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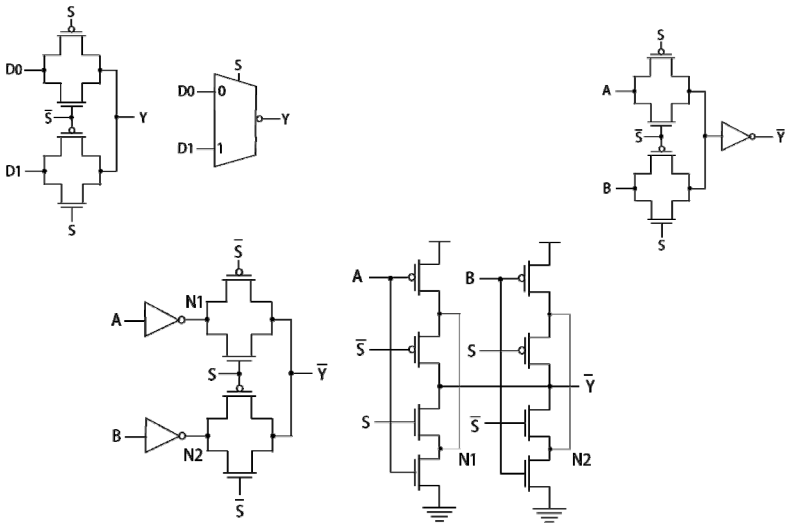
CMOS med transmisjonsporter



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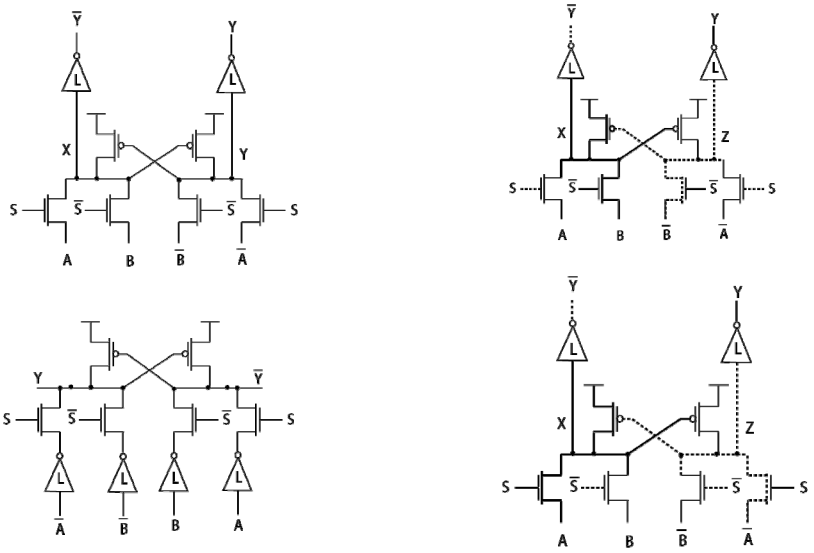
MES Mikroelektronikksystemer

Komplementær pass transistor logikk (CPL)



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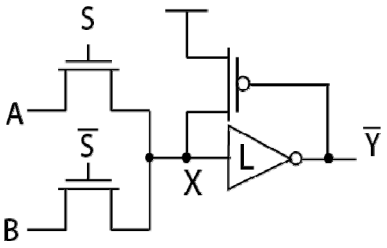
MES Mikroelektronikksystemer

LEAP



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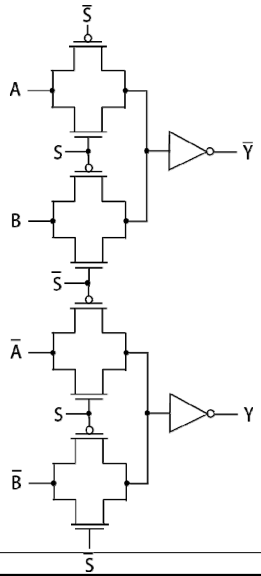
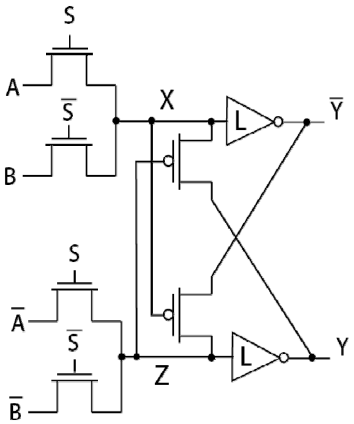
DPL og EEPL





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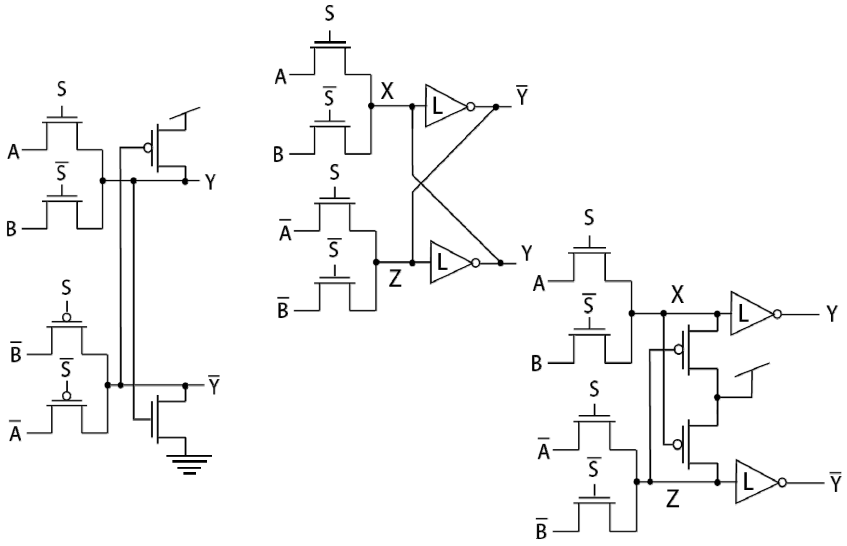
MES Mikroelektronikksystemer

PPL, SRPL og DCVSPG



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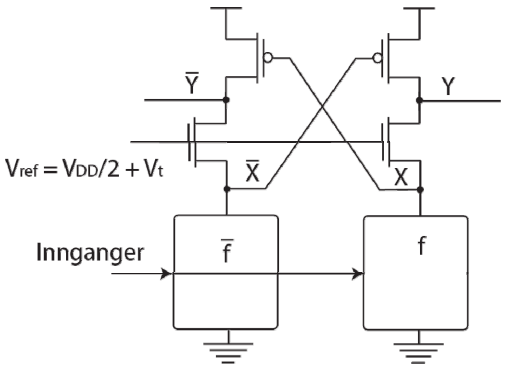
Differensielle kretser

Differensiell split-level:



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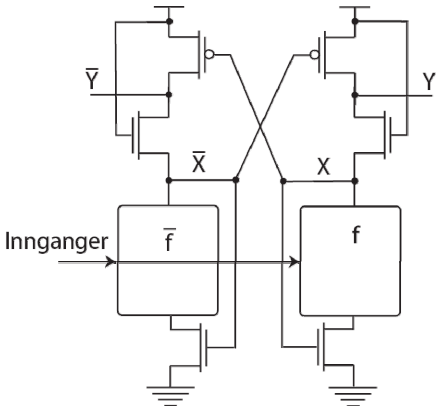
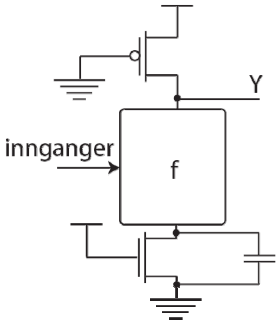
Kaskode nonthreshold logic:



Nonthreshold logic:



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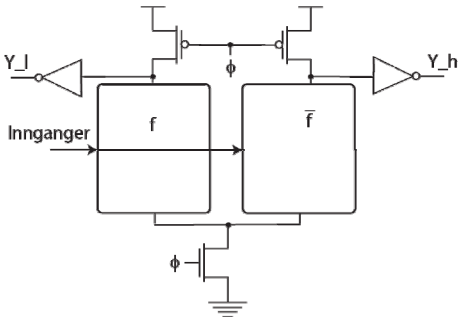
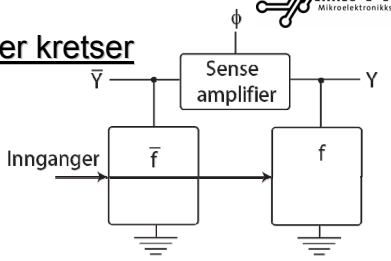
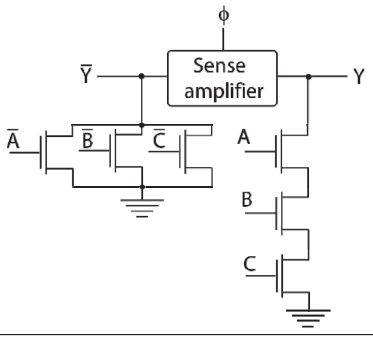
Sense-amplifier kretser

Dual rail domino logikk:







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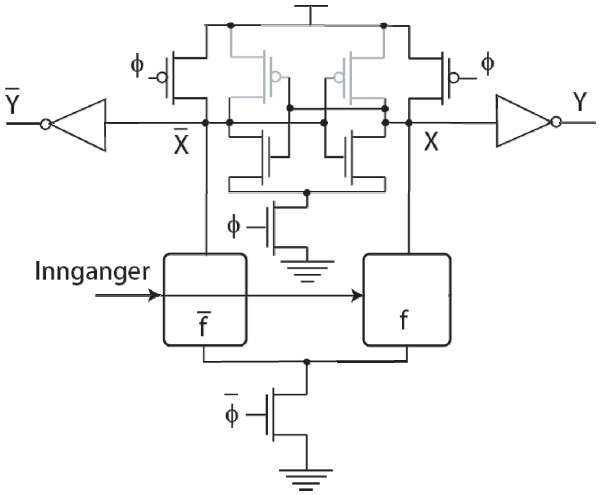
Sample set differensiell logikk



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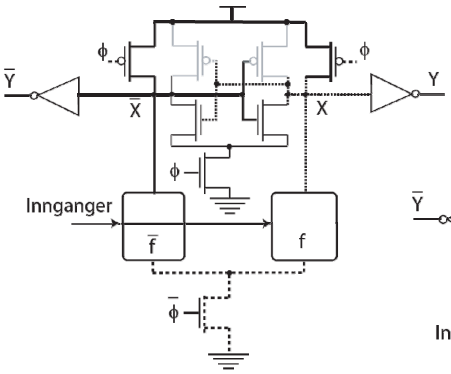
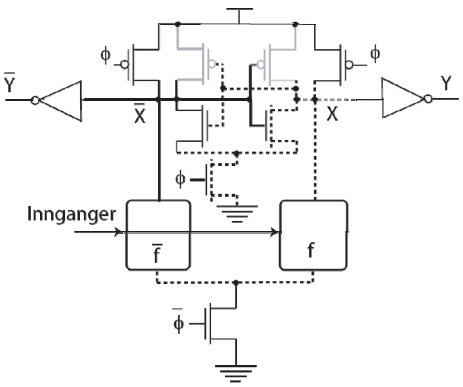
Sample:



Set:



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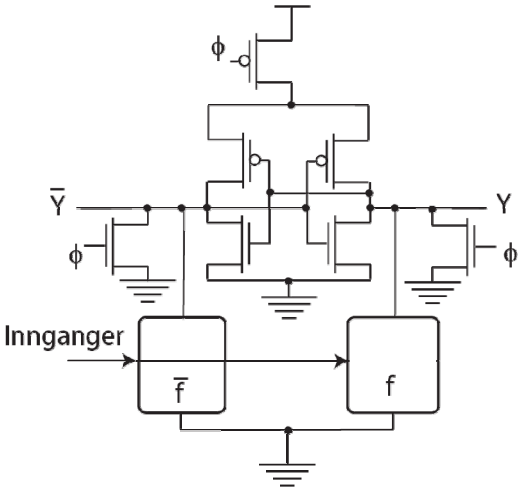
Enable/disable differensiell logikk



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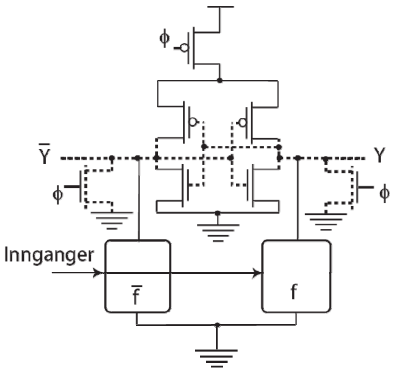
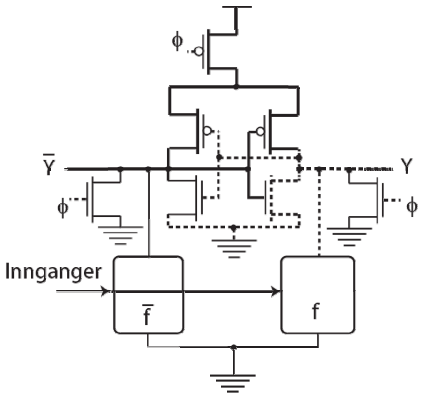
Disable:



Enable:



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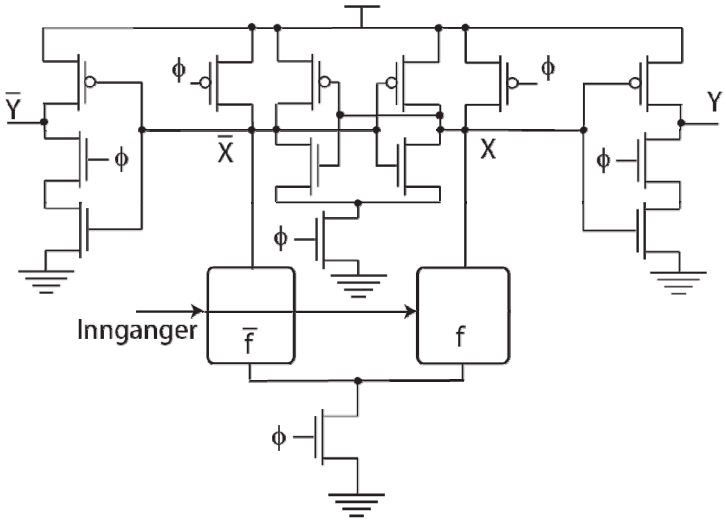
Latched differensiell logikk



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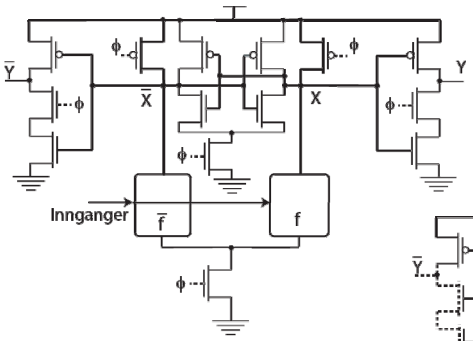
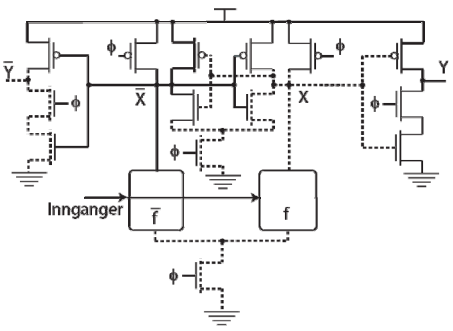
Precharge:



Evaluate:



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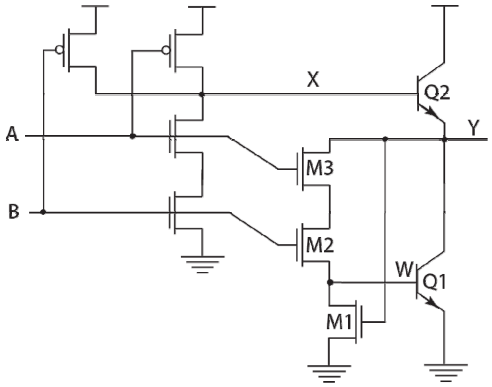
BiCMOS



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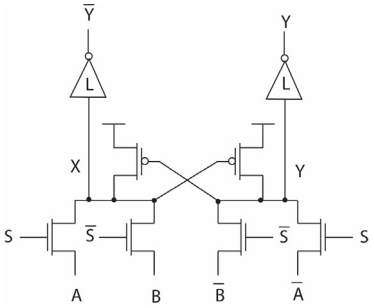
Oppgave A

Tegn sjematikk for en 4:1 multiplekser med innganger D0, D1, D2 og D3, og to selekt signaler S0 og S1, i følgende logikkstiler:

1. CPL.
2. LEAP.
3. DPL.
4. EEPL.
5. PPL.
6. SRPL.
7. DCVSPG.
8. Statisk CMOS

CPL



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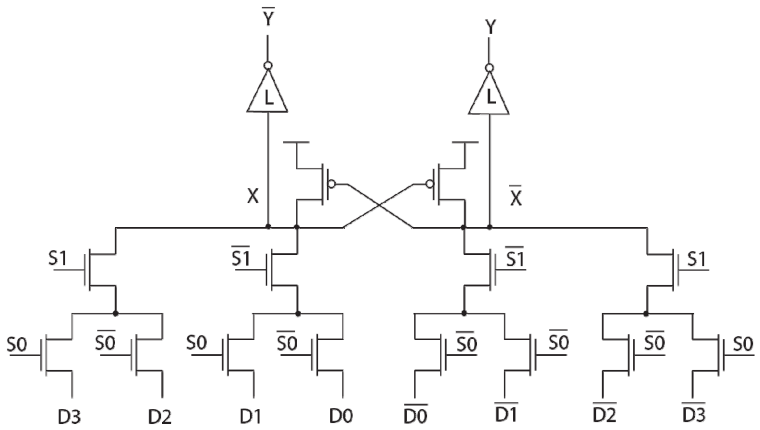
CPL



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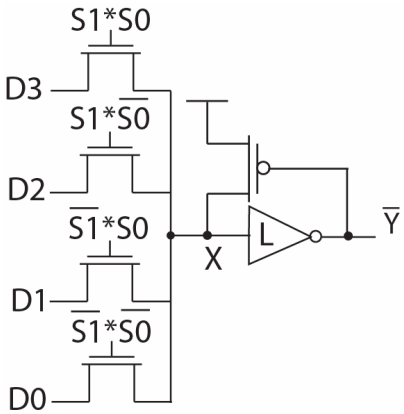
LEAP



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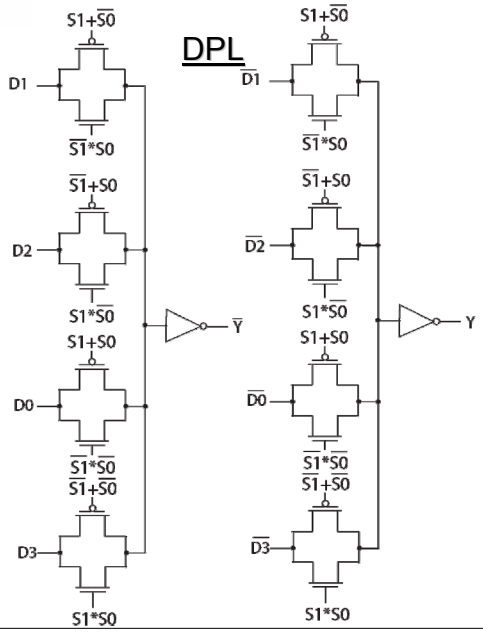
DPL



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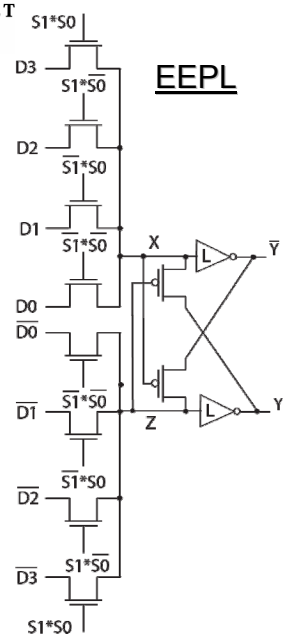
EEPL



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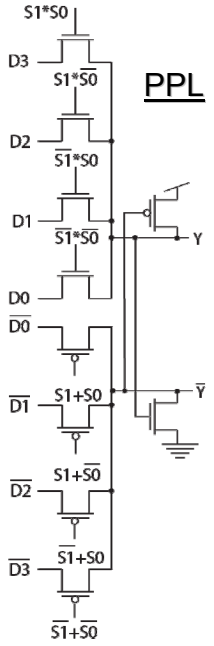
PPL



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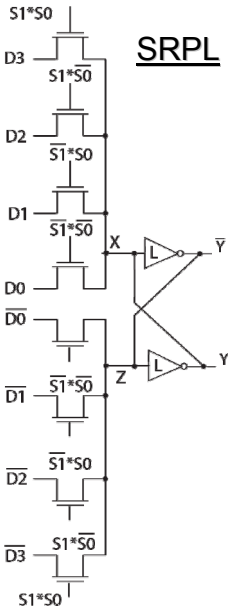
SRPL



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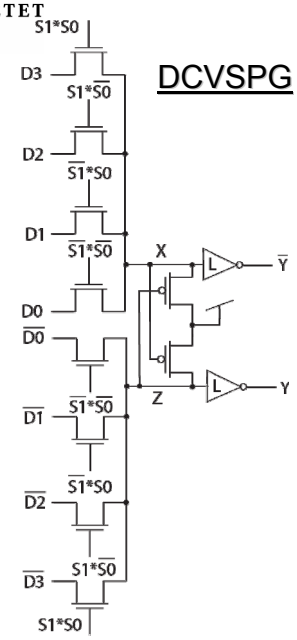
DCVSPG



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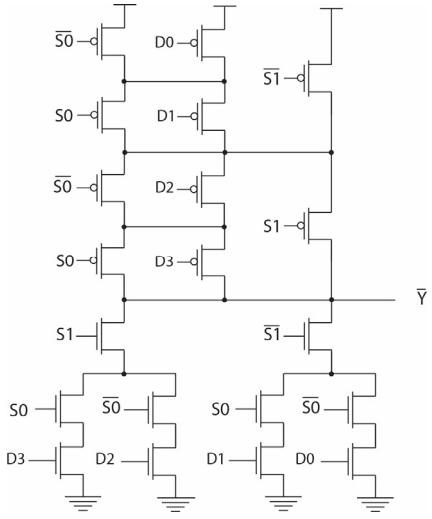
Statisk CMOS



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MES Mikroelektronikksystemer

Oppgave B

Tegn skjematikk for en 3inngangs NAND port i følgende logikkstiler:

1. SSDL.
2. ECDL.
3. LCDL.
4. DCSL.
5. BiCMOS.

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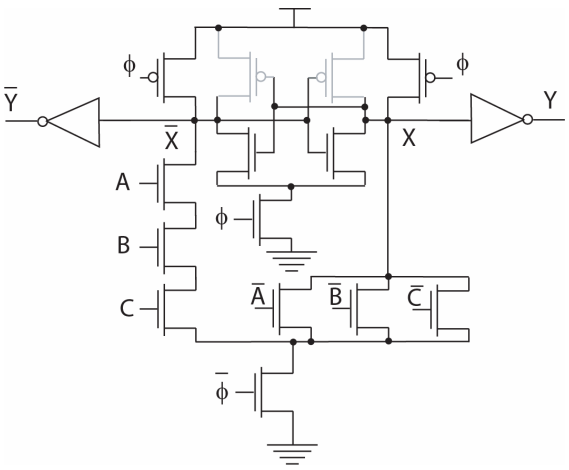
SSDL



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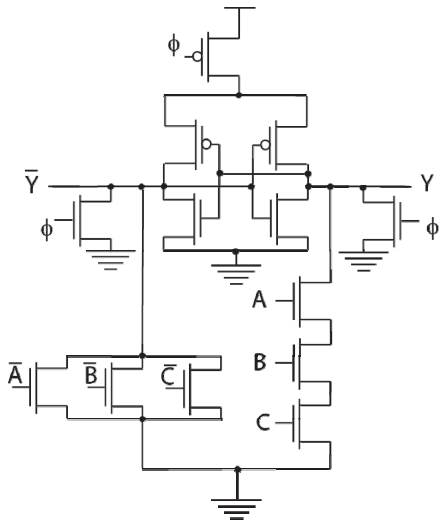
ECDL



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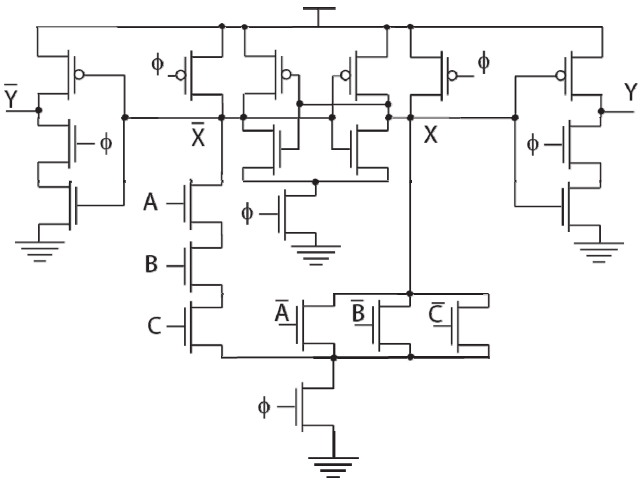
LCDL



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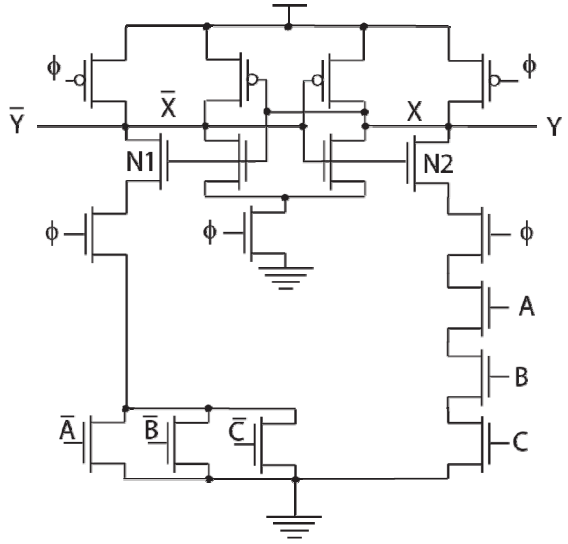
DCSL



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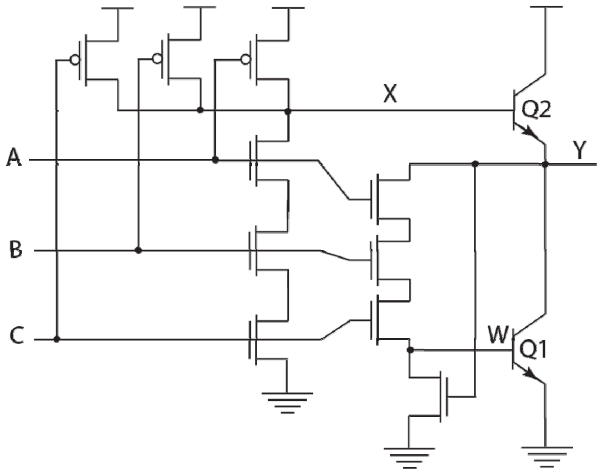
BiCMOS



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