INF3430

Introduksjon til VHDL

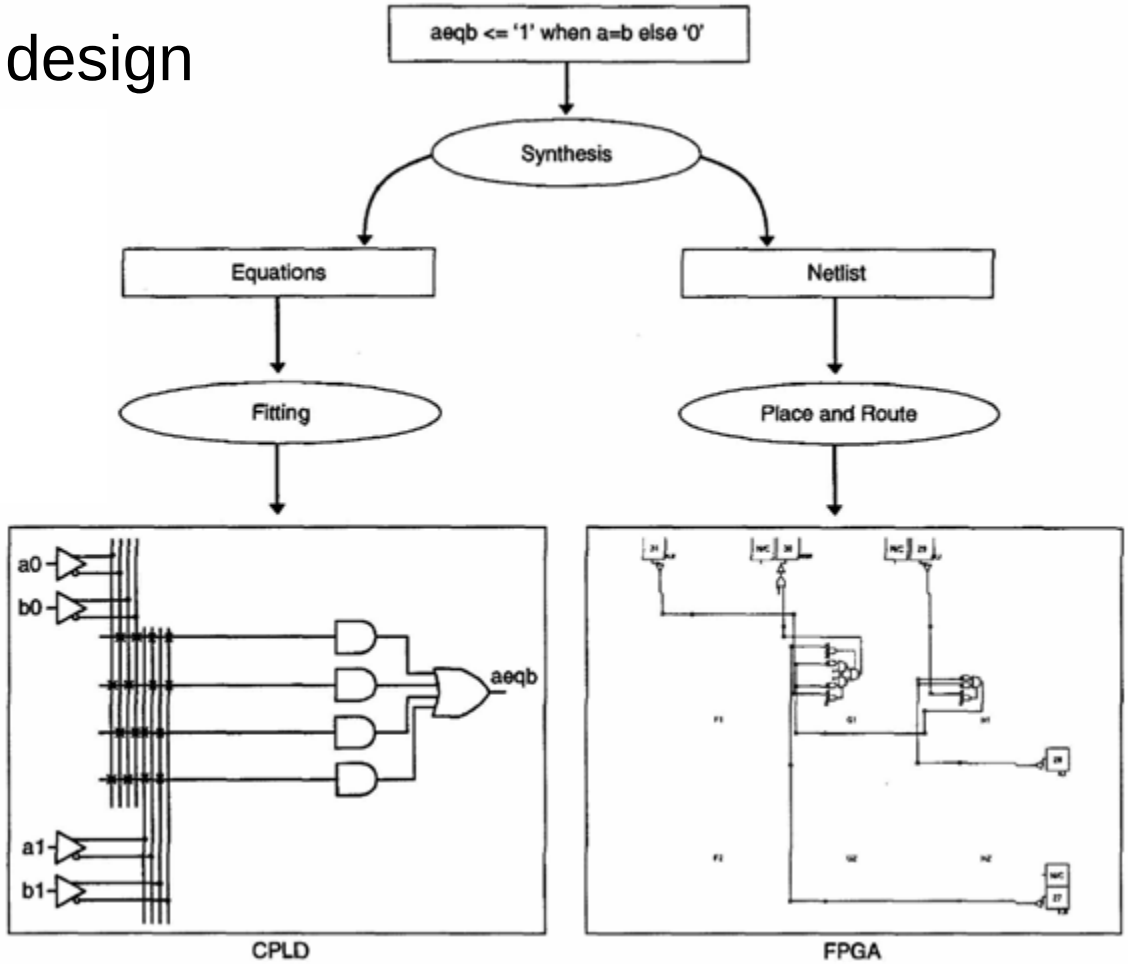
Spartan starterkit

Agenda

- Hva skal vi gjøre i INF3430?
  - VDHL simulering/syntese
  - Place & Route til FPGA
  - Prøve ut design i ekte hardware
- Hvorfor VHDL eller andre HDL (Hardware Description Language)?
- Gjennomgang av dokumentasjon for labkort
- Spartan-3 FPGA oppbygning

Hvorfor HDL?

- Syntese til design



Hvorfor HDL?

- Teknologiuavhengig kode
- Forskjellig abstrakssjonsnivå

Netlist:

```
U1: xor2 port map(a(0), b(0), x(0));
U2: xor2 port map(a(1), b(1), x(1));
U3: nor2 port map(x(0), x(1), aeqb);
```

Boolean equations:

```
aeqb <=      (a(0) xor b(0))
         nor (a(1) xor b(1));
```

Concurrents statements:

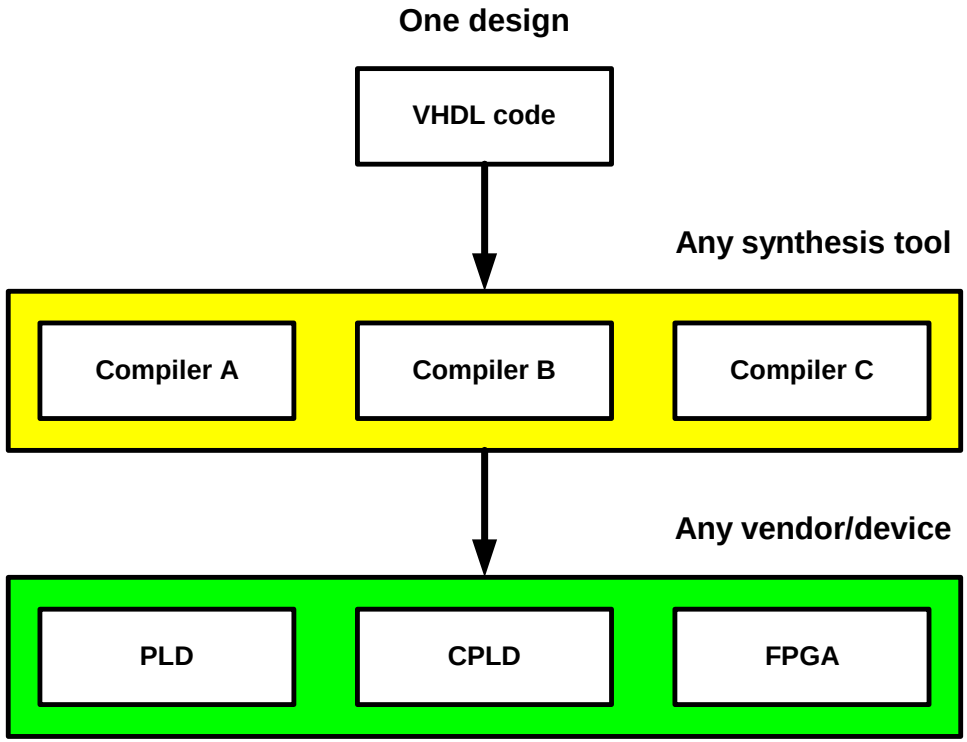
```
aeqb <= '1' when a=b else '0';
```

Sequential statements:

```
if a=b then
 aeqb <= '1';
    else
 aeqb <= '0';
  end if;
```

Hvorfor HDL?

- Portabilitet
- VHDL/Verilog er standardisert under IEEE (Institute of Electrical and Electronics Engineers)
  - VHDL - IEEE 1076
  - Verilog - IEEE 1364



Hvorfor HDL?

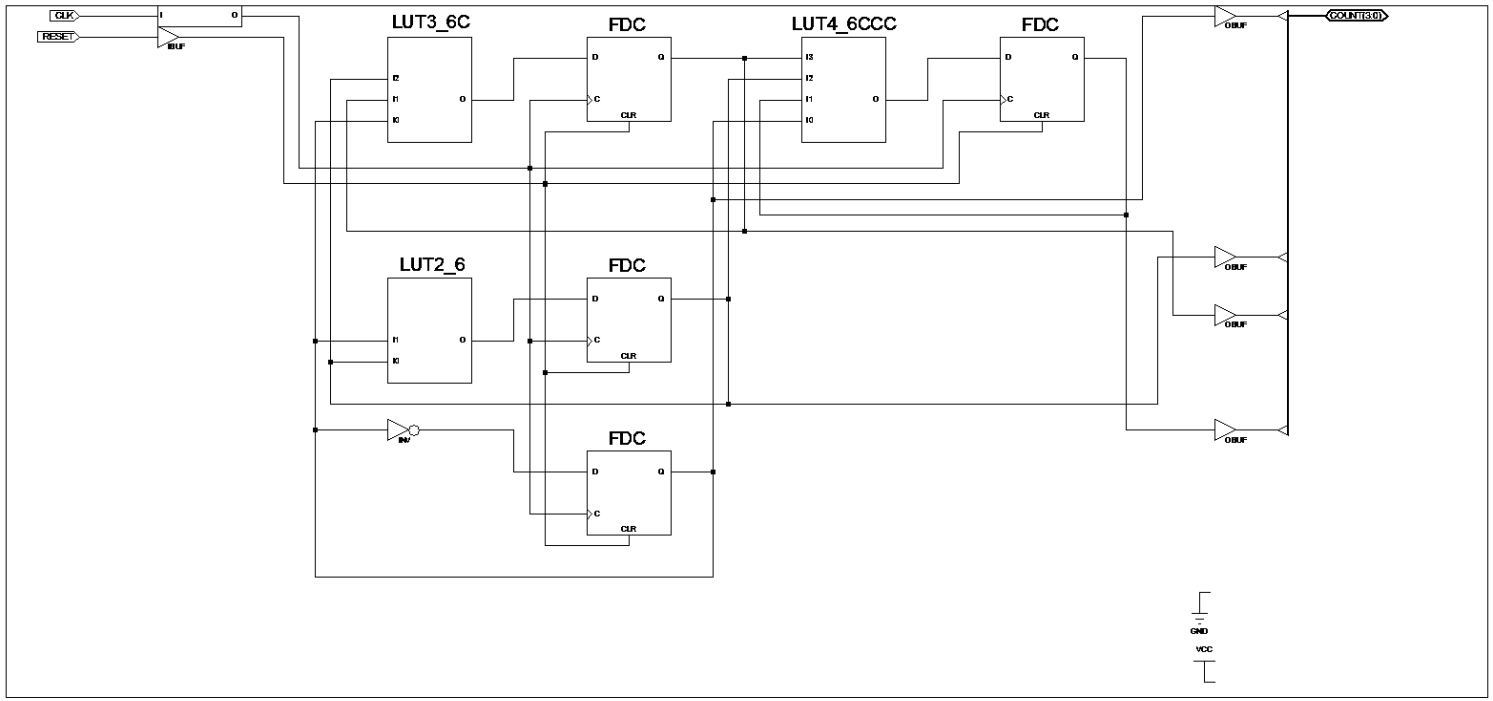
- Enkelt vedlikehold/utvidelse av design

```
COUNT      : inout std_logic_vector(3 downto 0); -- Telleverdi
---
COUNTER :
  process (RESET,CLK)
  begin
    if(RESET  = '1') then
      COUNT <= (others => '0');
    elsif rising_edge(CLK) then
      COUNT <= COUNT + 1;
    end if;
  end process COUNTER;
```

Hvorfor HDL?

- Enkelt vedlikehold/utvidelse av design

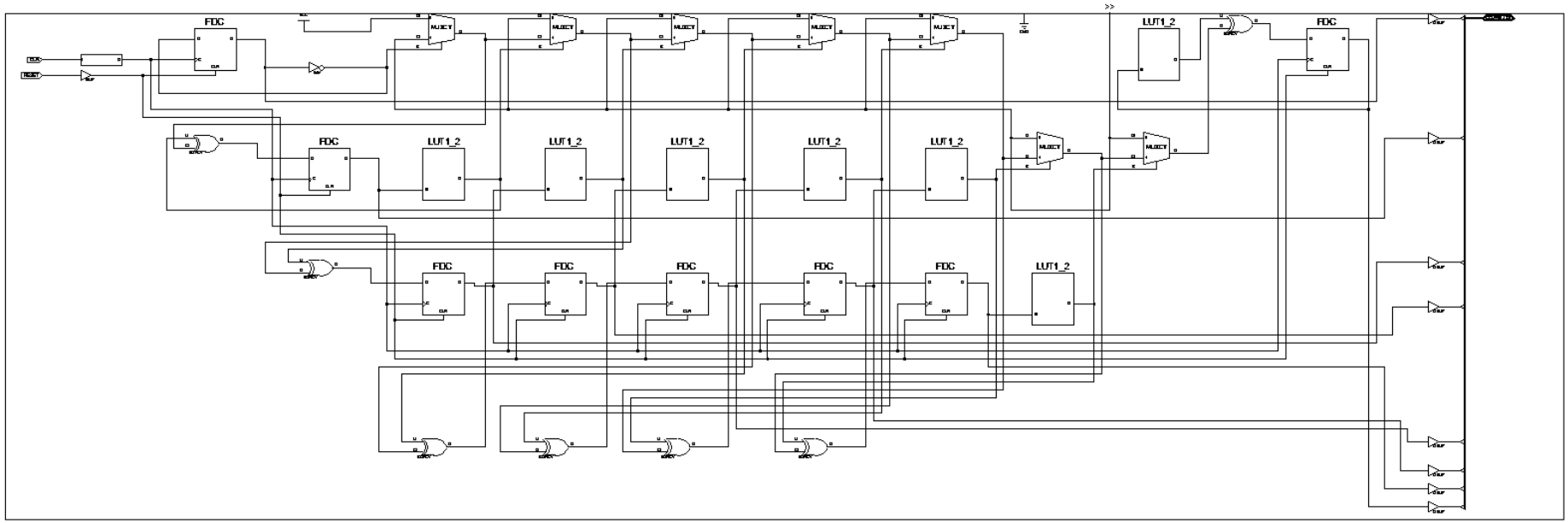
```
COUNT      : inout std_logic_vector(3 downto 0); -- Telleverdi
```



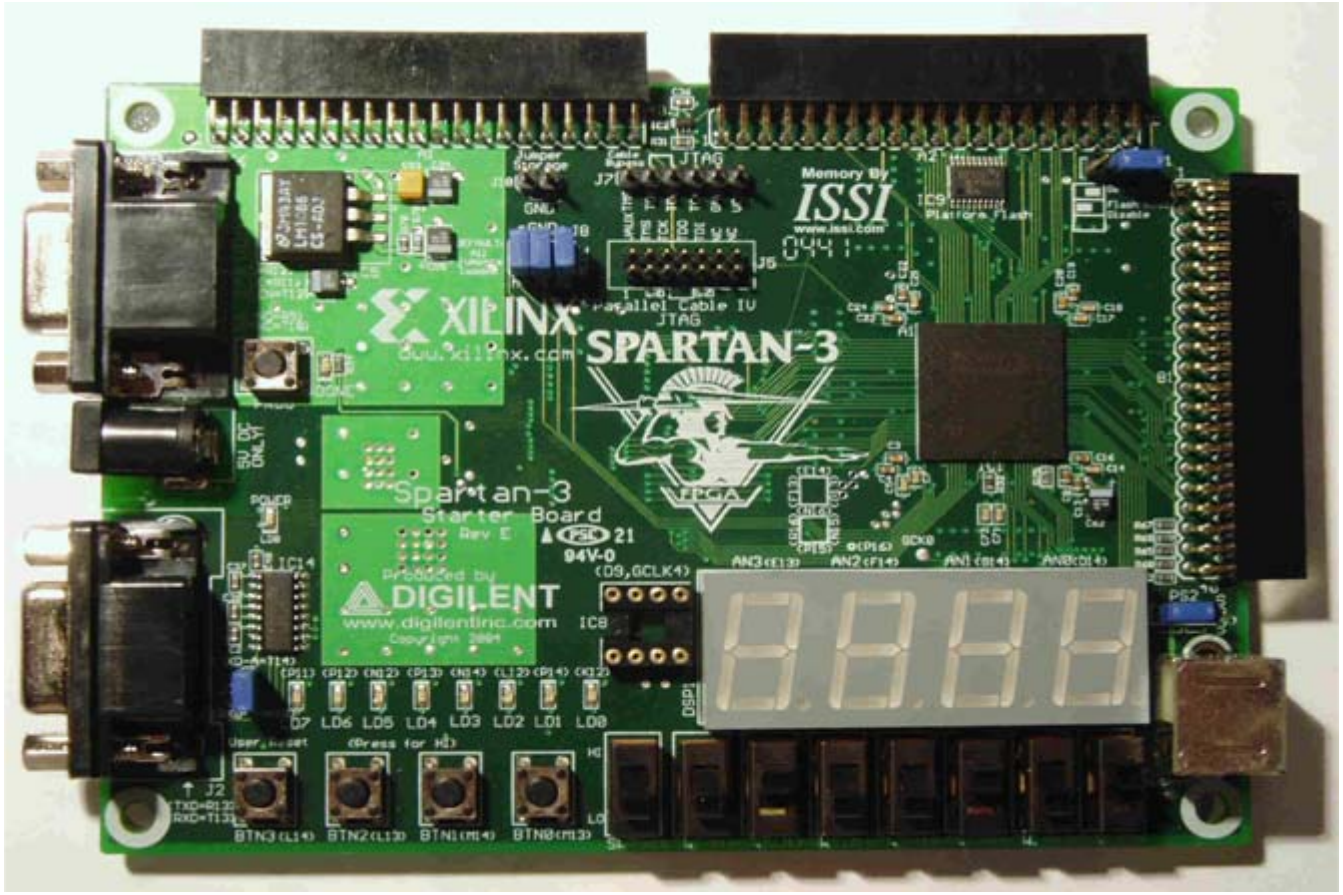
Hvorfor HDL?

- Enkelt vedlikehold/utvidelse av design

```
COUNT      : inout std_logic_vector(7 downto 0); -- Telleverdi
```

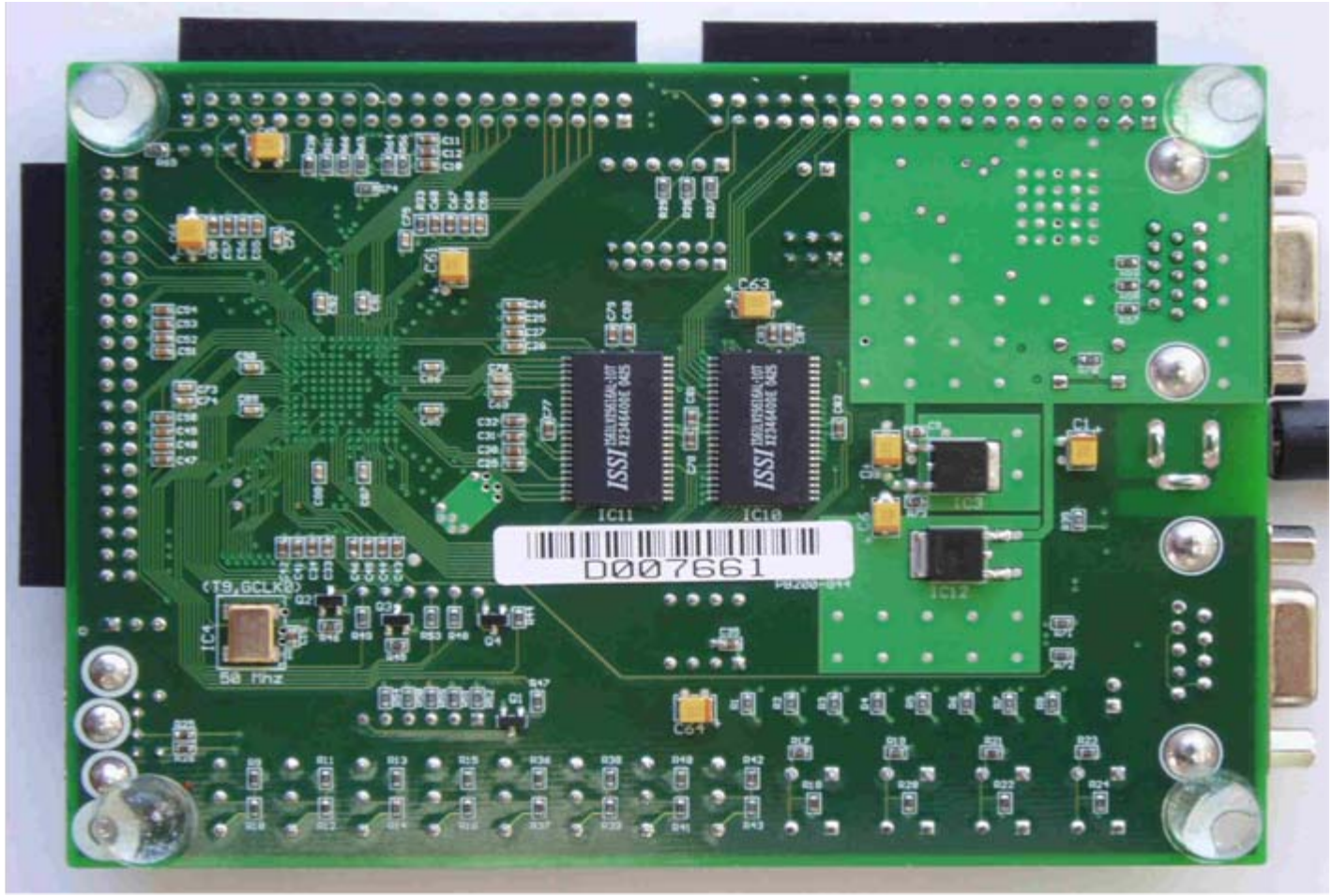


Spartan-3 labkort

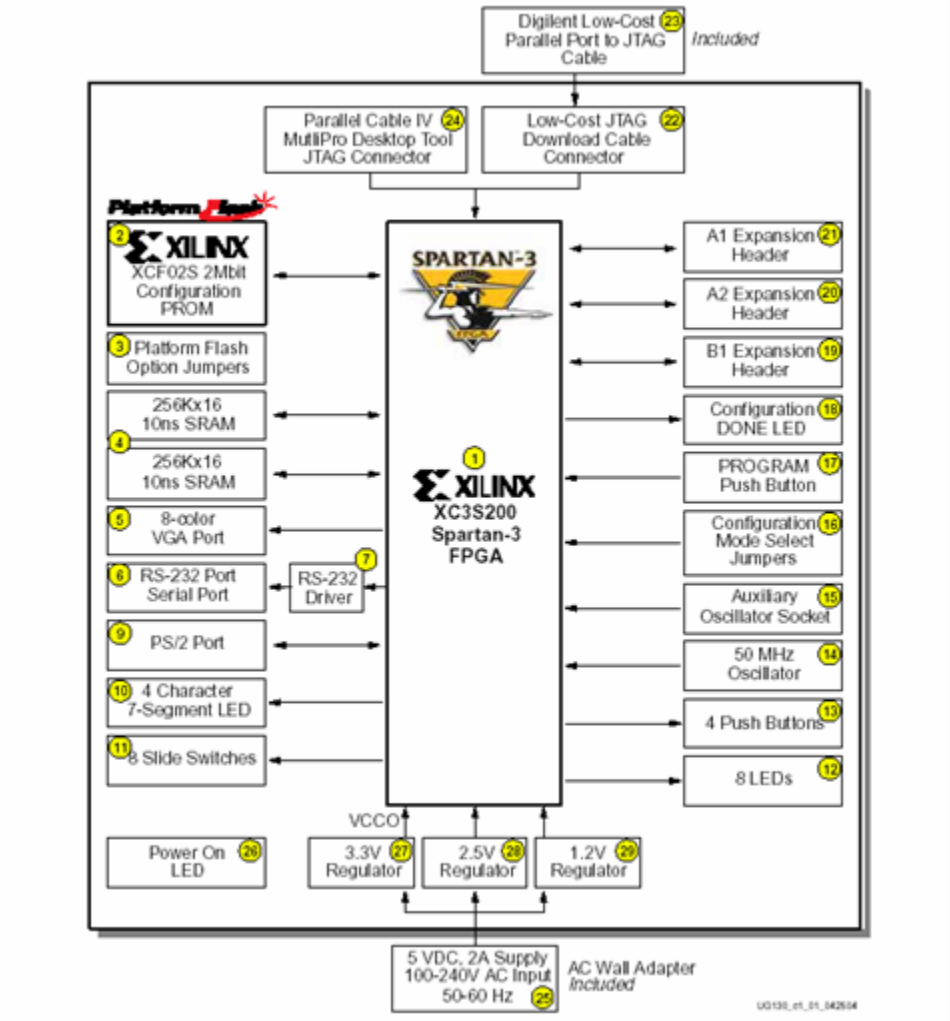


http://www.digilentinc.com/Products/Detail.cfm?Prod=S3BOARD&Nav1=Products&Nav2=Programmable

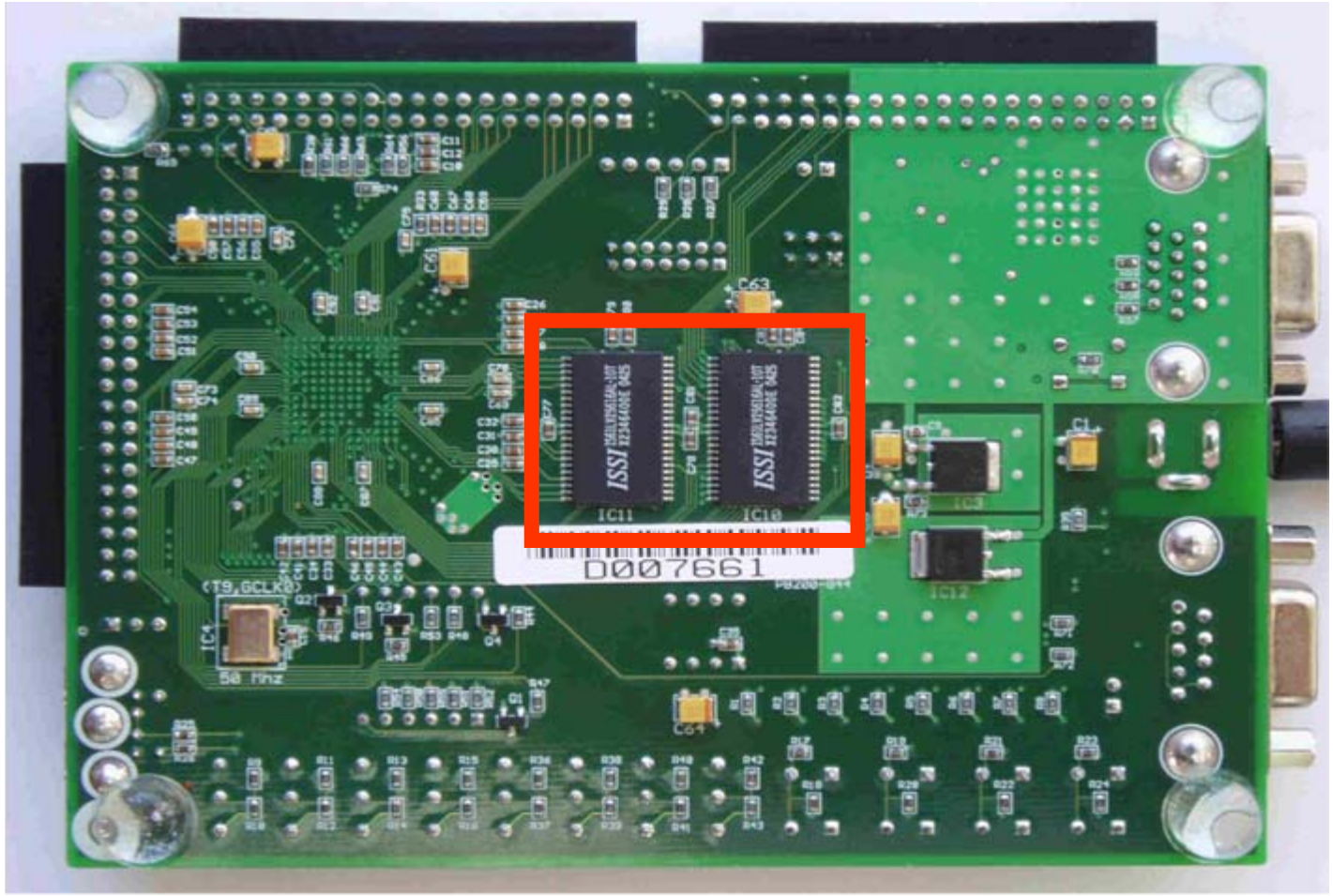
Spartan-3 labkort



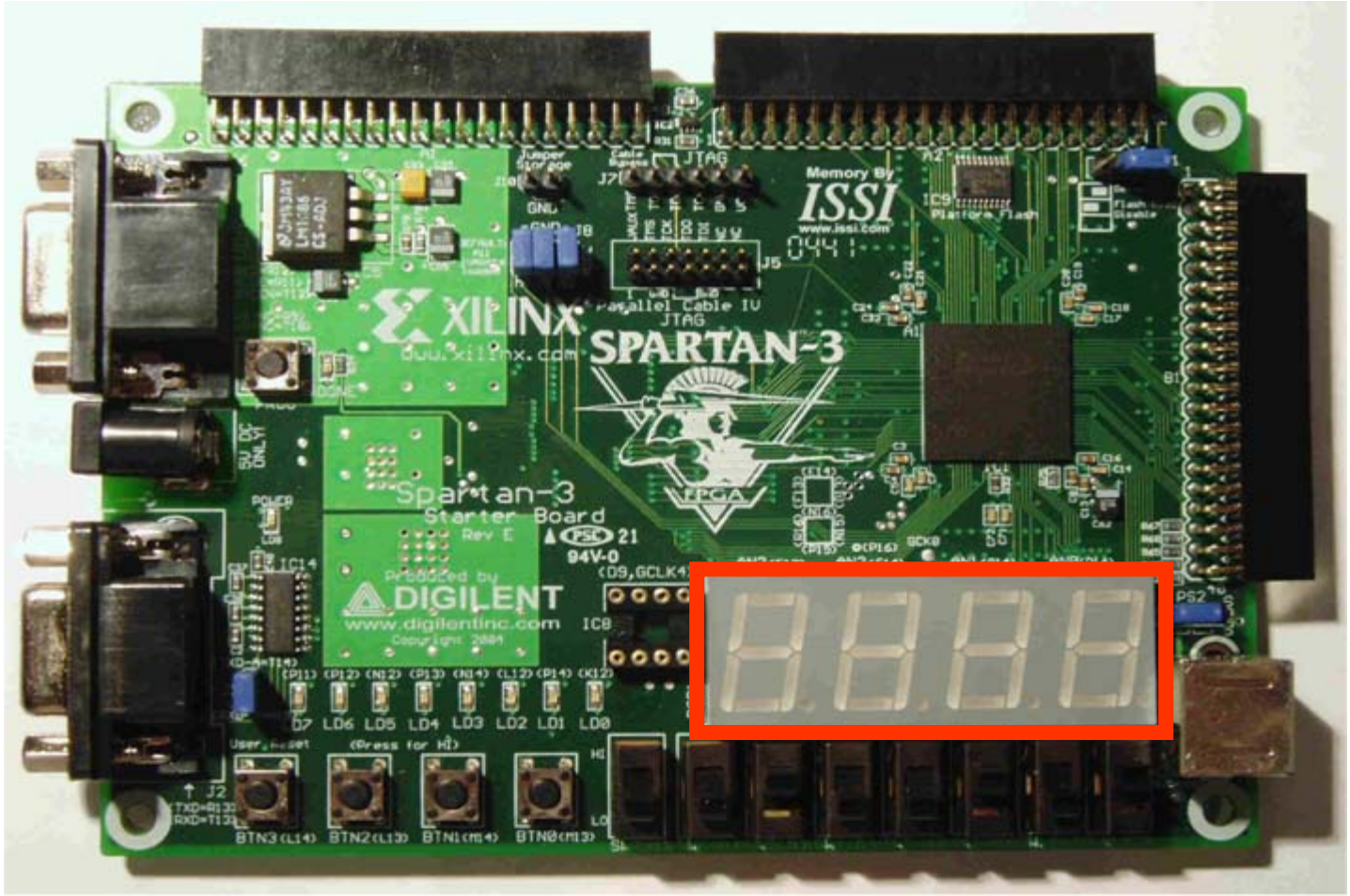
Spartan-3 labkort



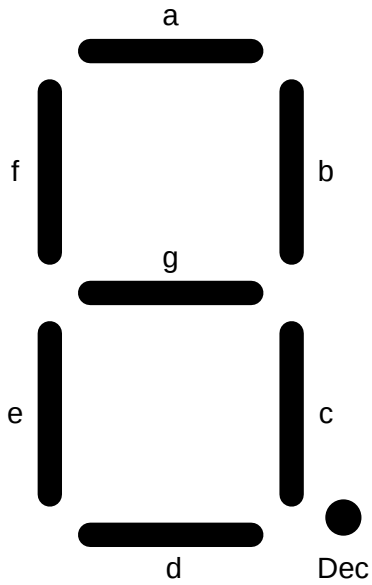
Spartan-3 labkort
SRAM

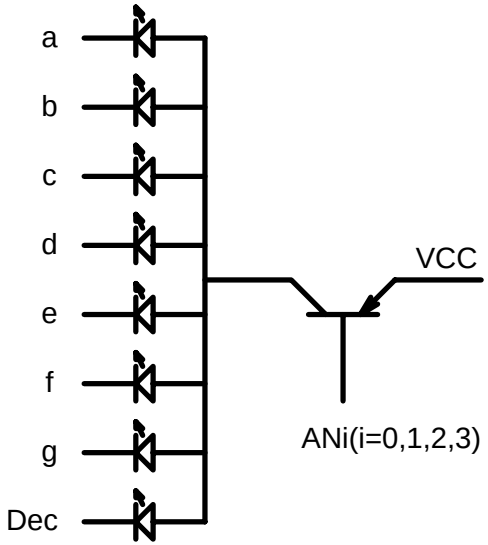


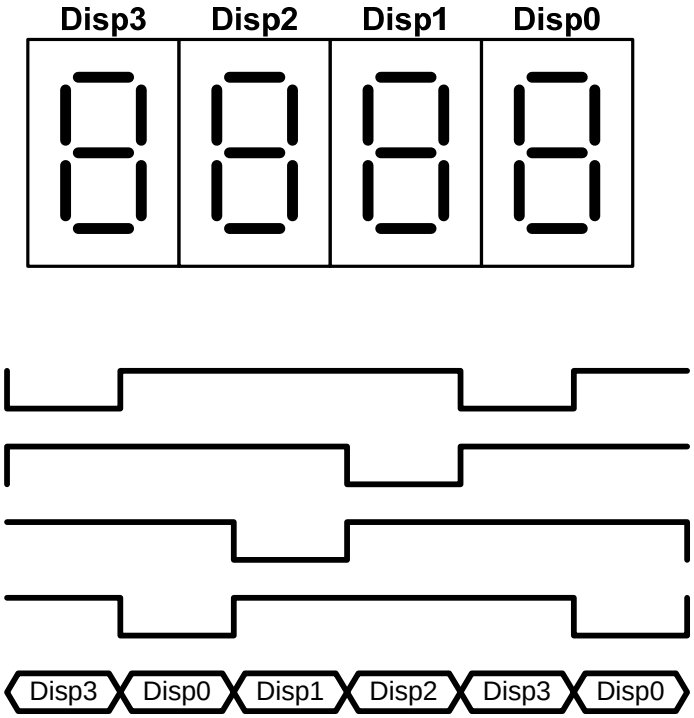
Spartan-3 labkort
Sjusegmenter



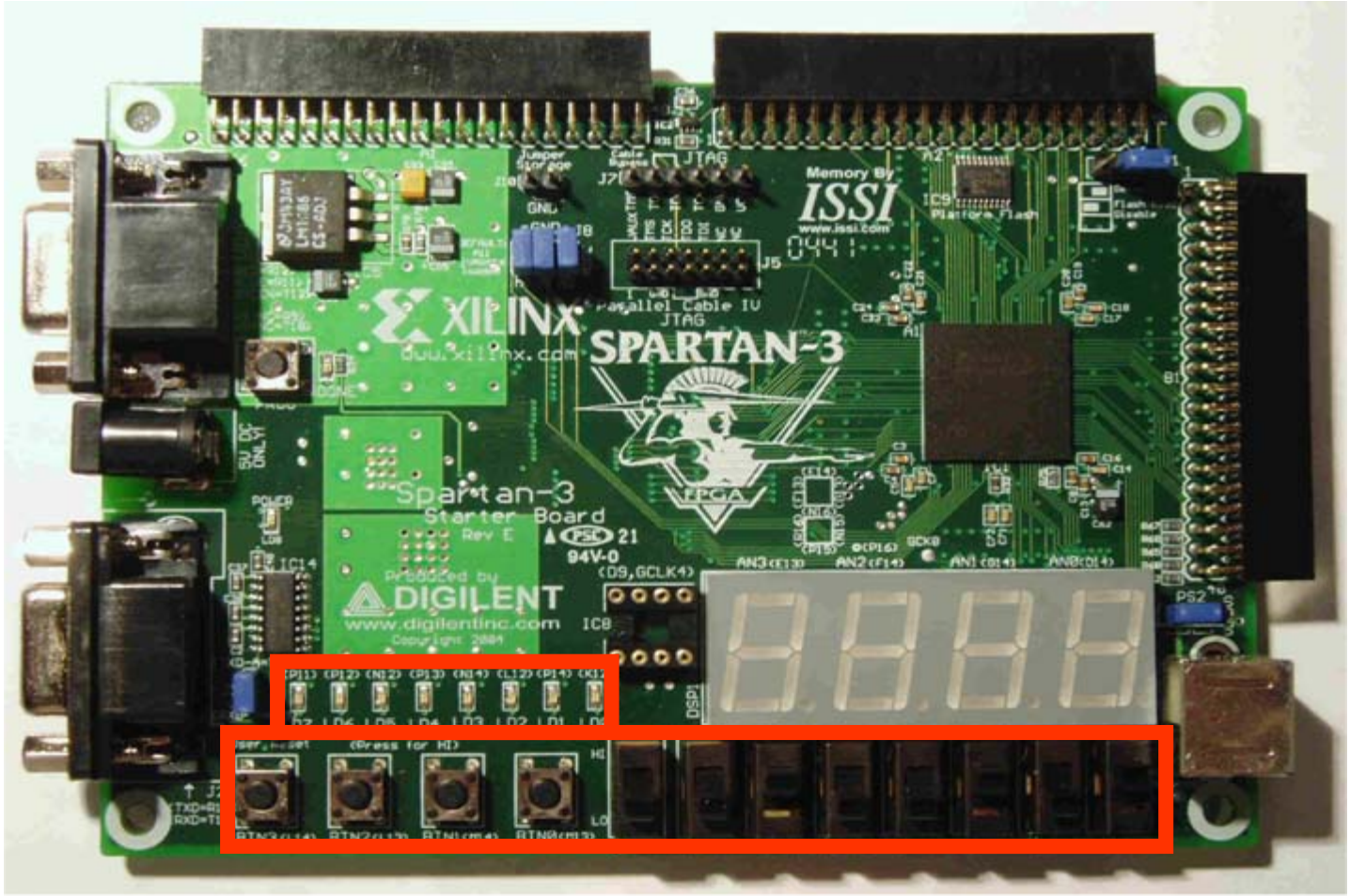
Styring av sjusegmentene



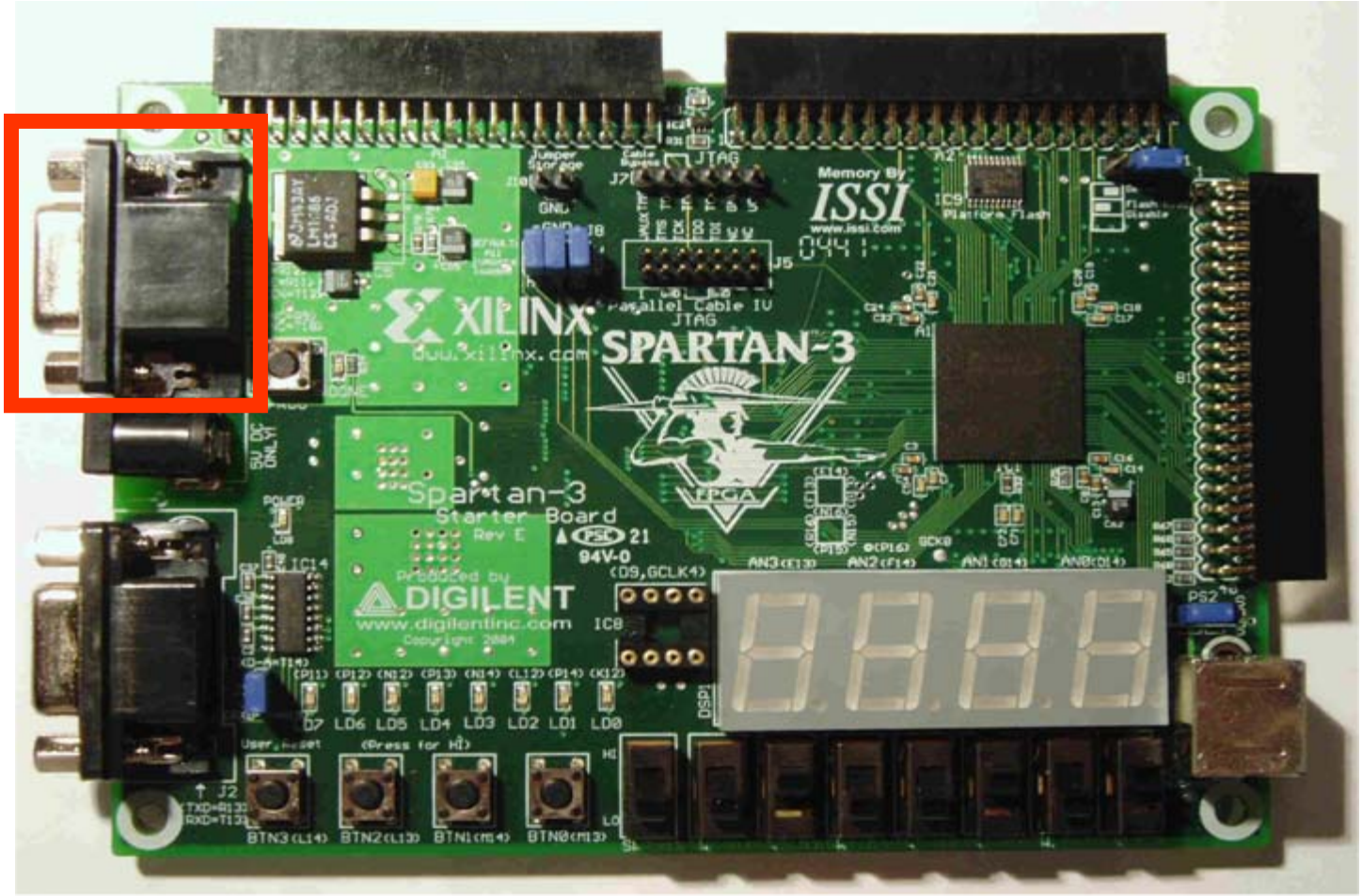




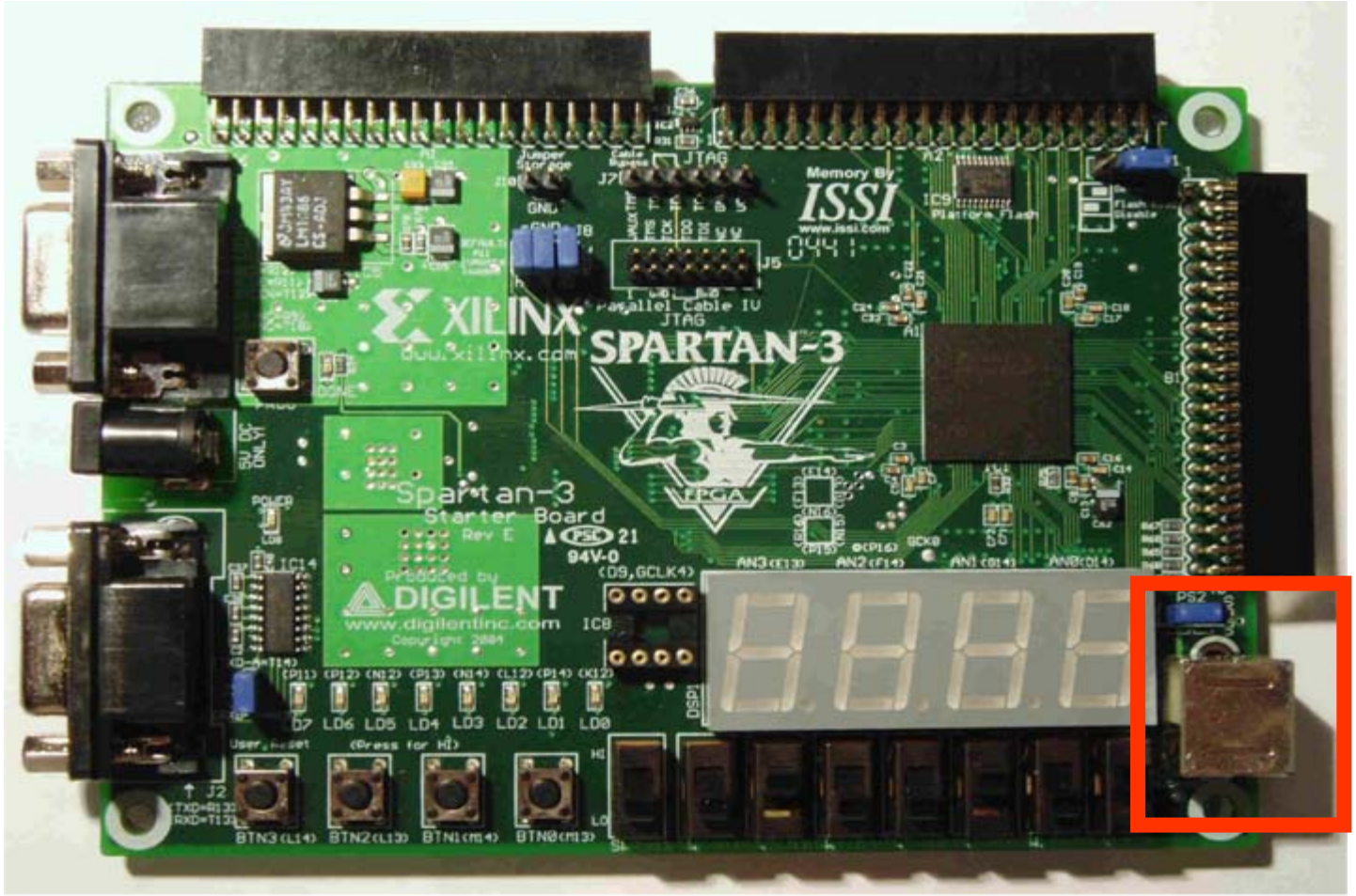
Spartan-3 labkort
Push buttons, Switches, LEDs



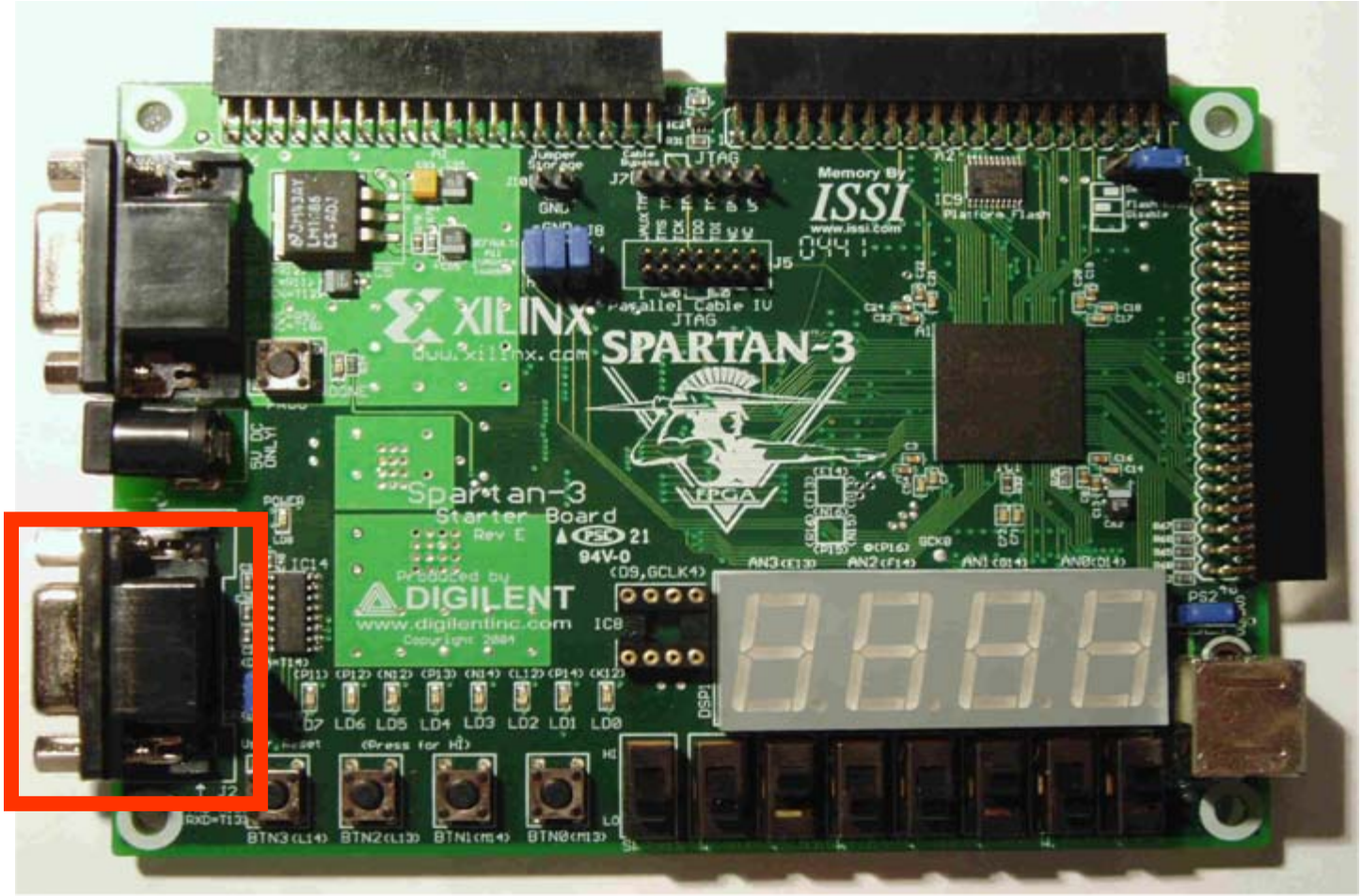
Spartan-3 labkort
VGA port



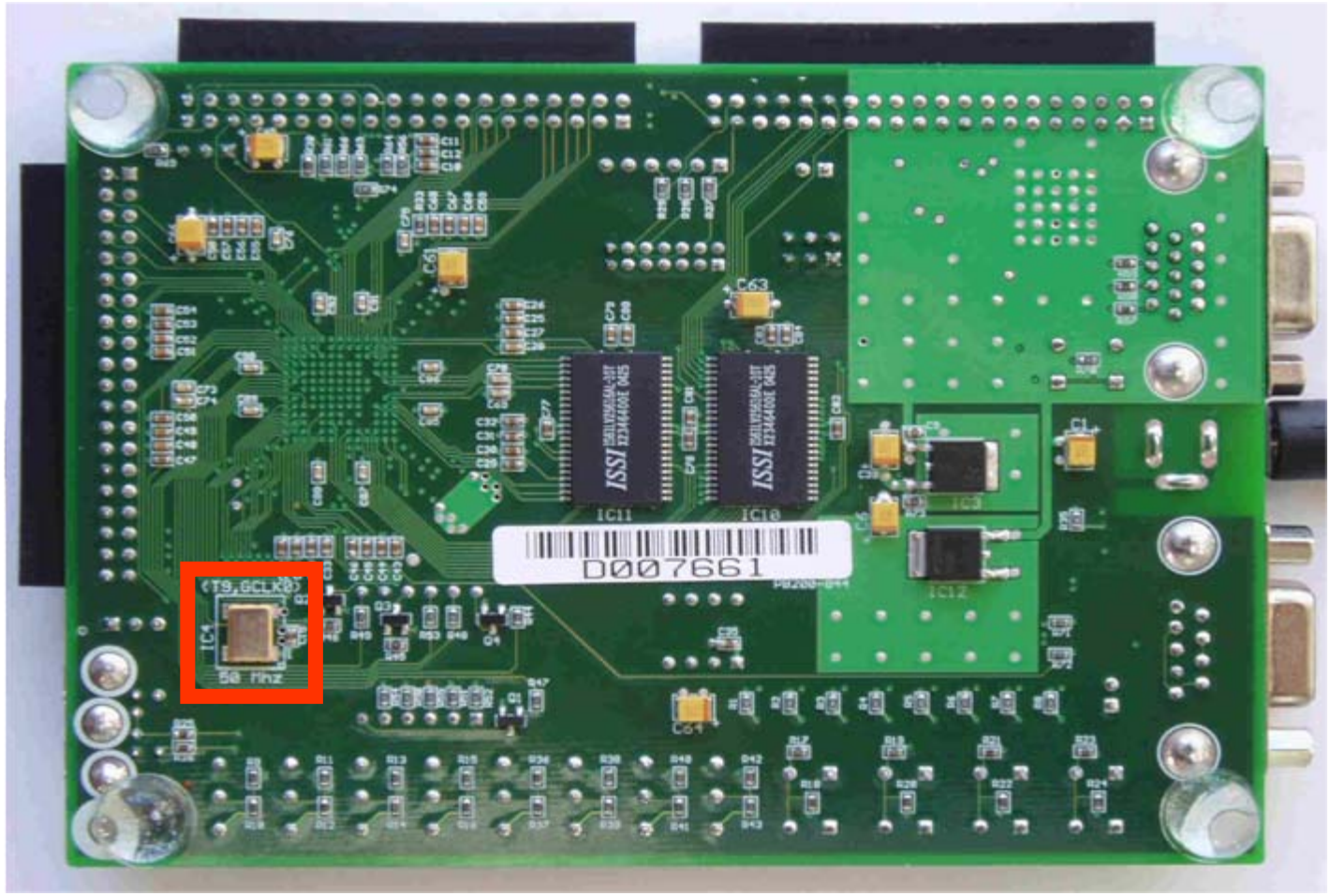
Spartan-3 labkort
PS2 port (tastatur/mus)



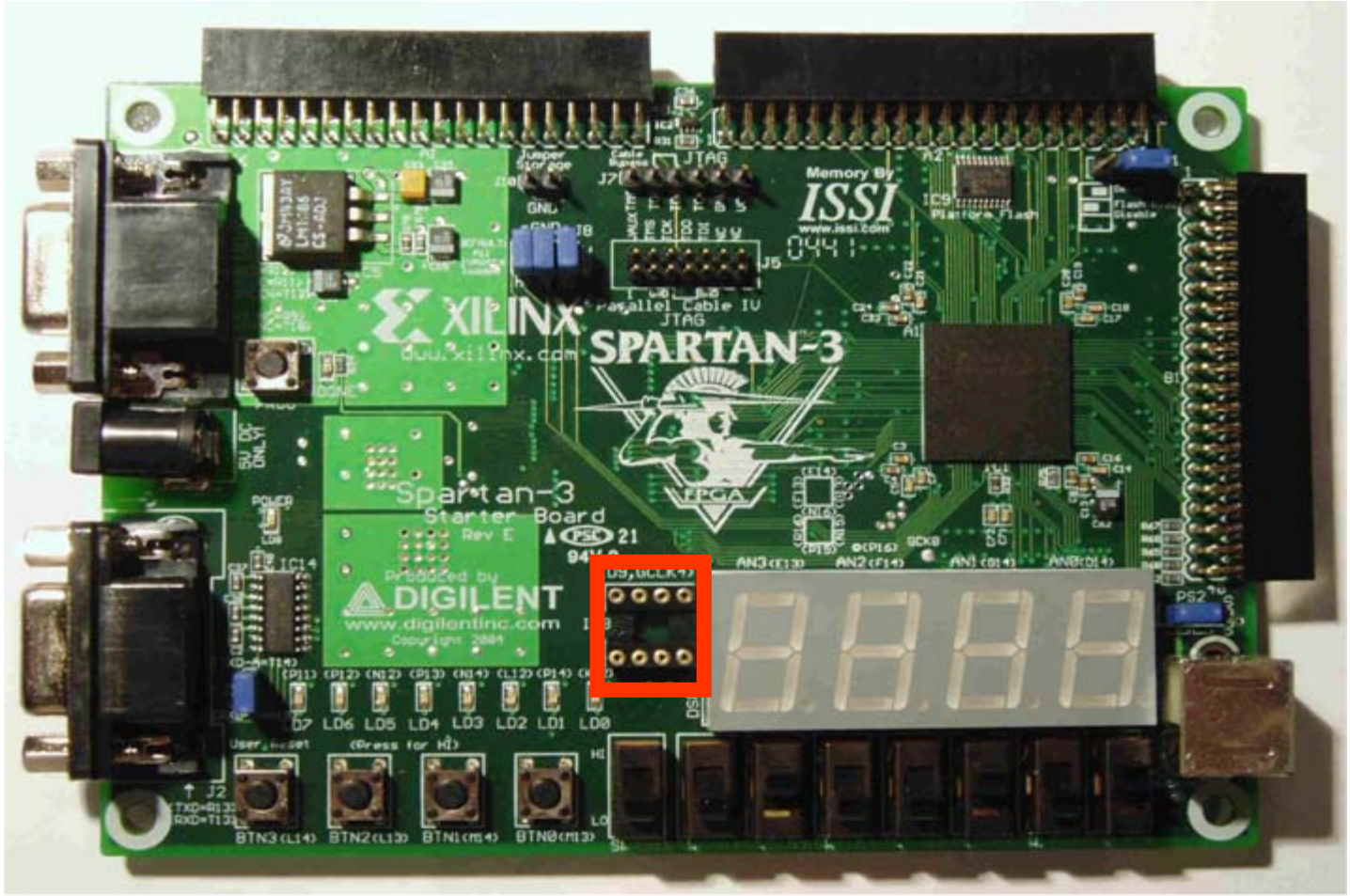
Spartan-3 labkort
RS-232 port (serie port)



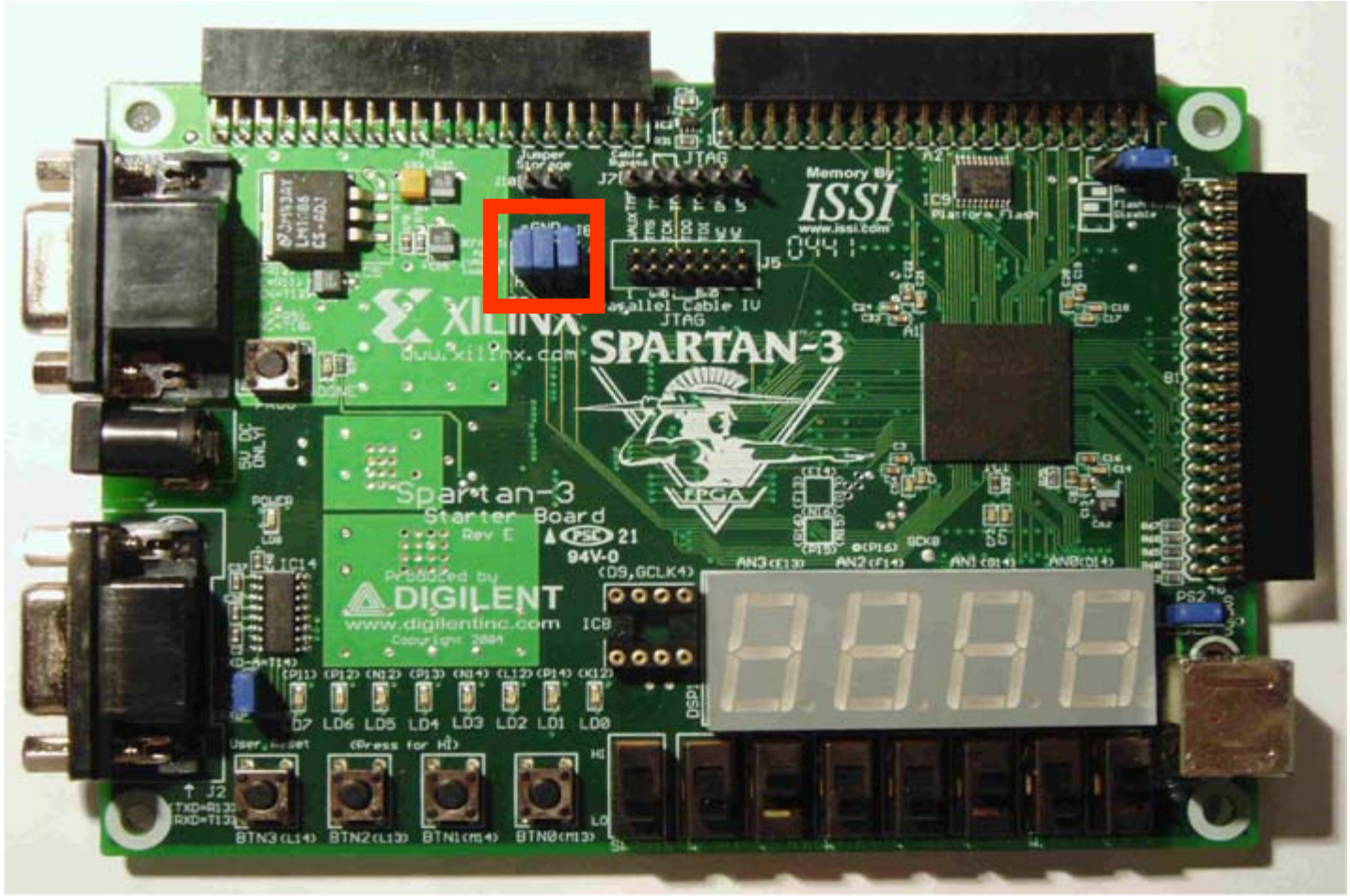
Spartan-3 labkort
50MHz klokke



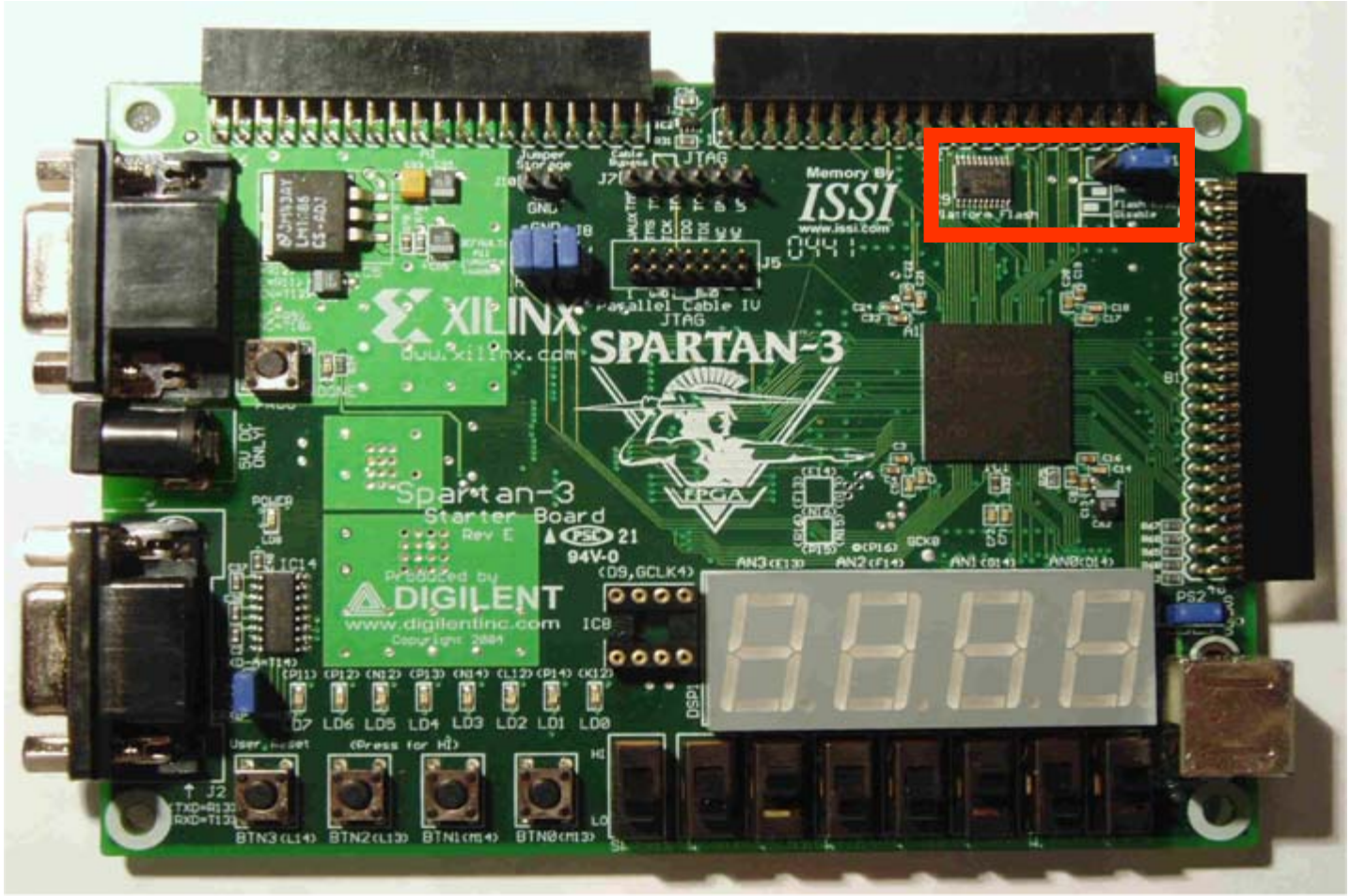
Spartan-3 labkort.
Ekstra klokke



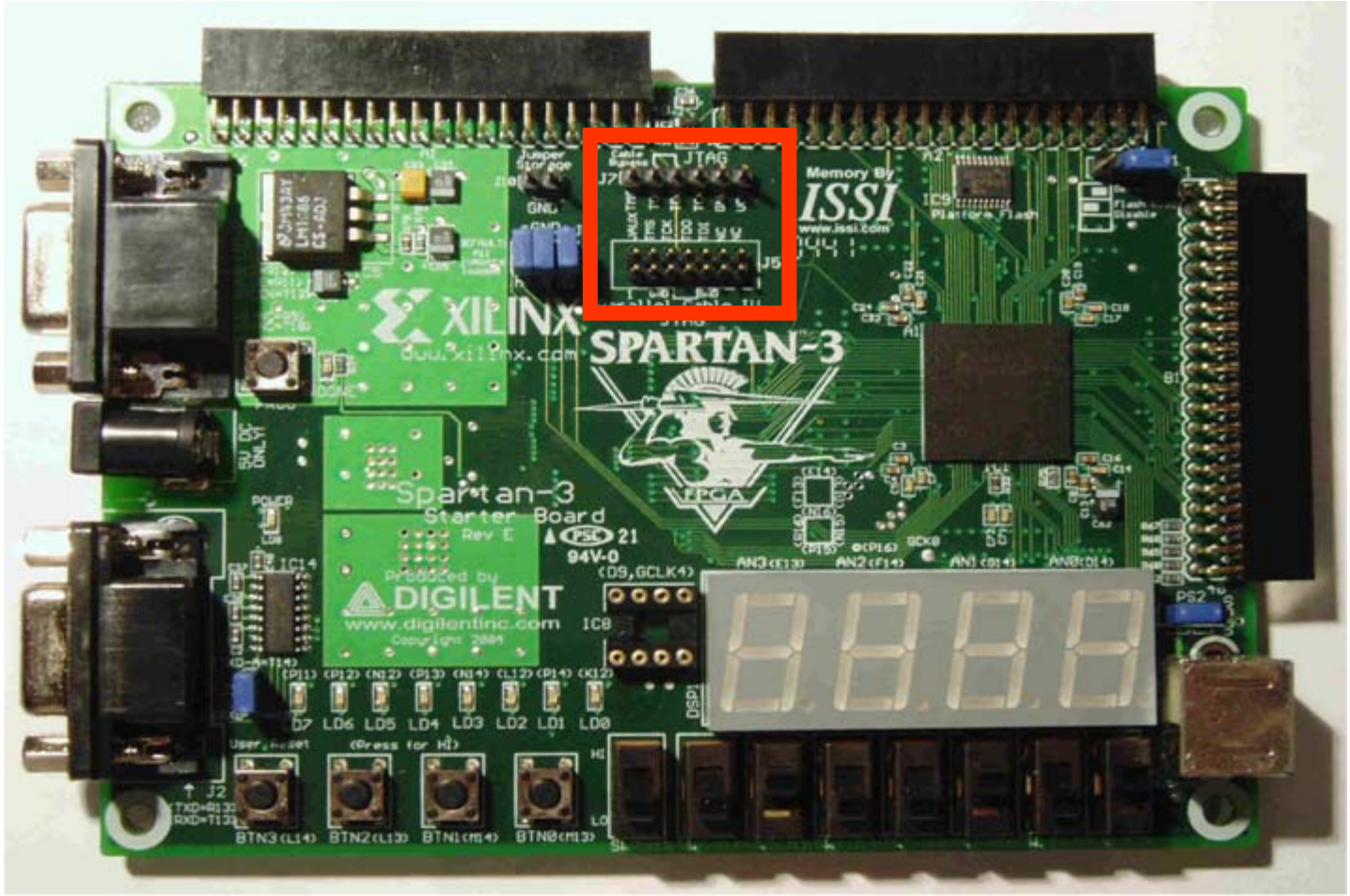
Spartan-3 labkort.
Konfigurasjonsmode jumpere



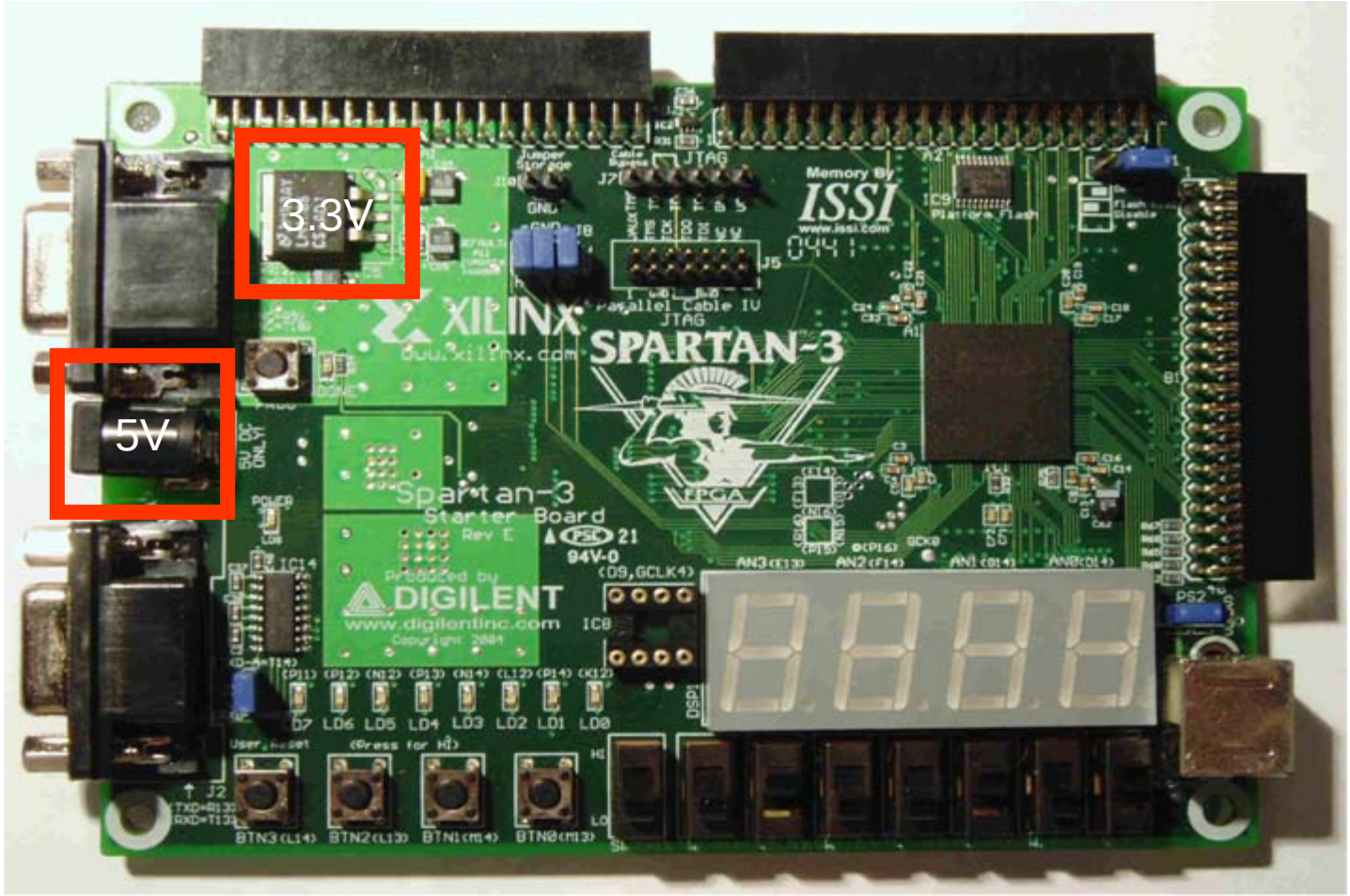
Spartan-3 labkort.
Platform Flash minne



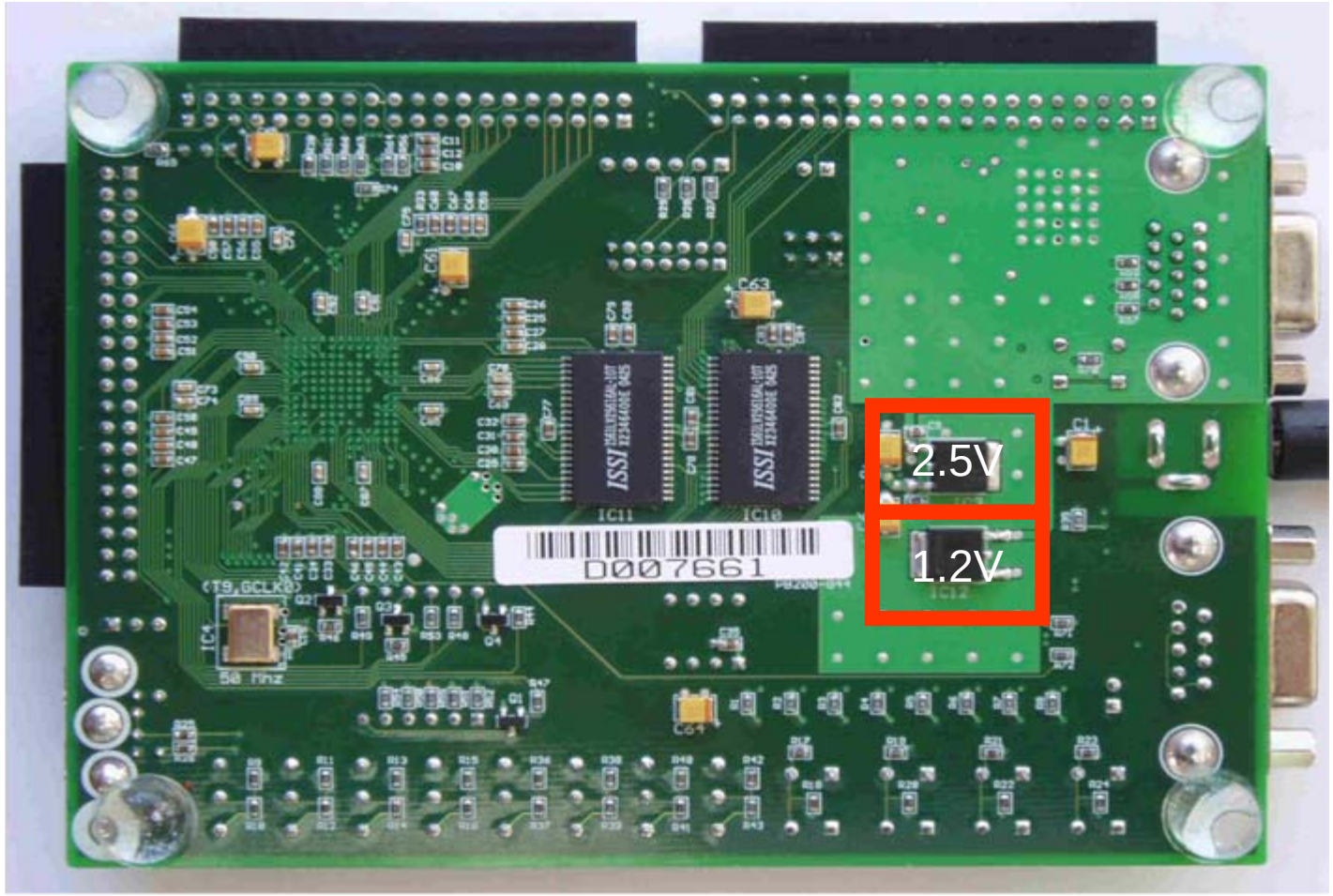
Spartan-3 labkort.
JTAG programming/debug ports



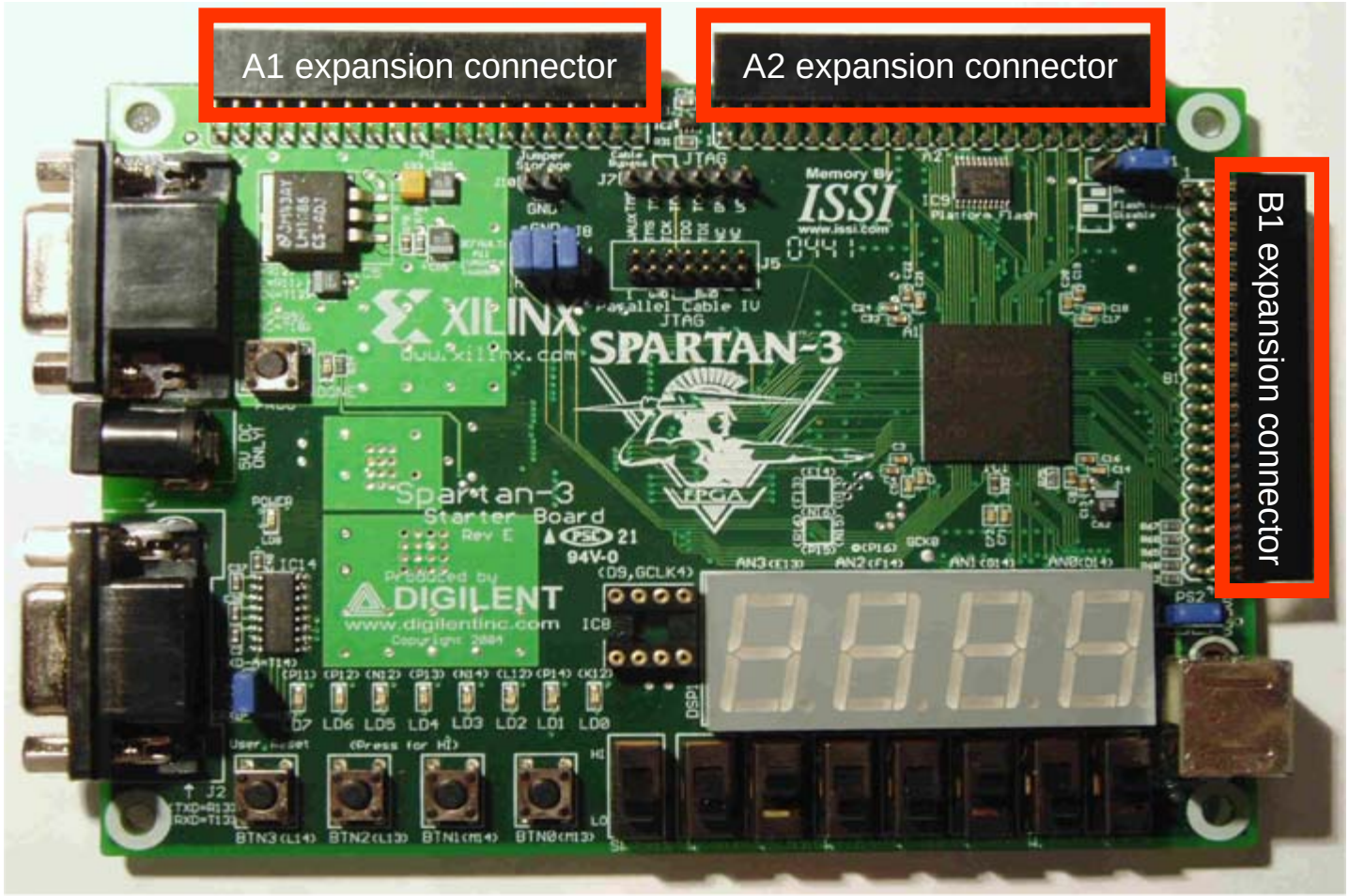
Spartan-3 labkort.
Power supplies (5V og 3.3V)



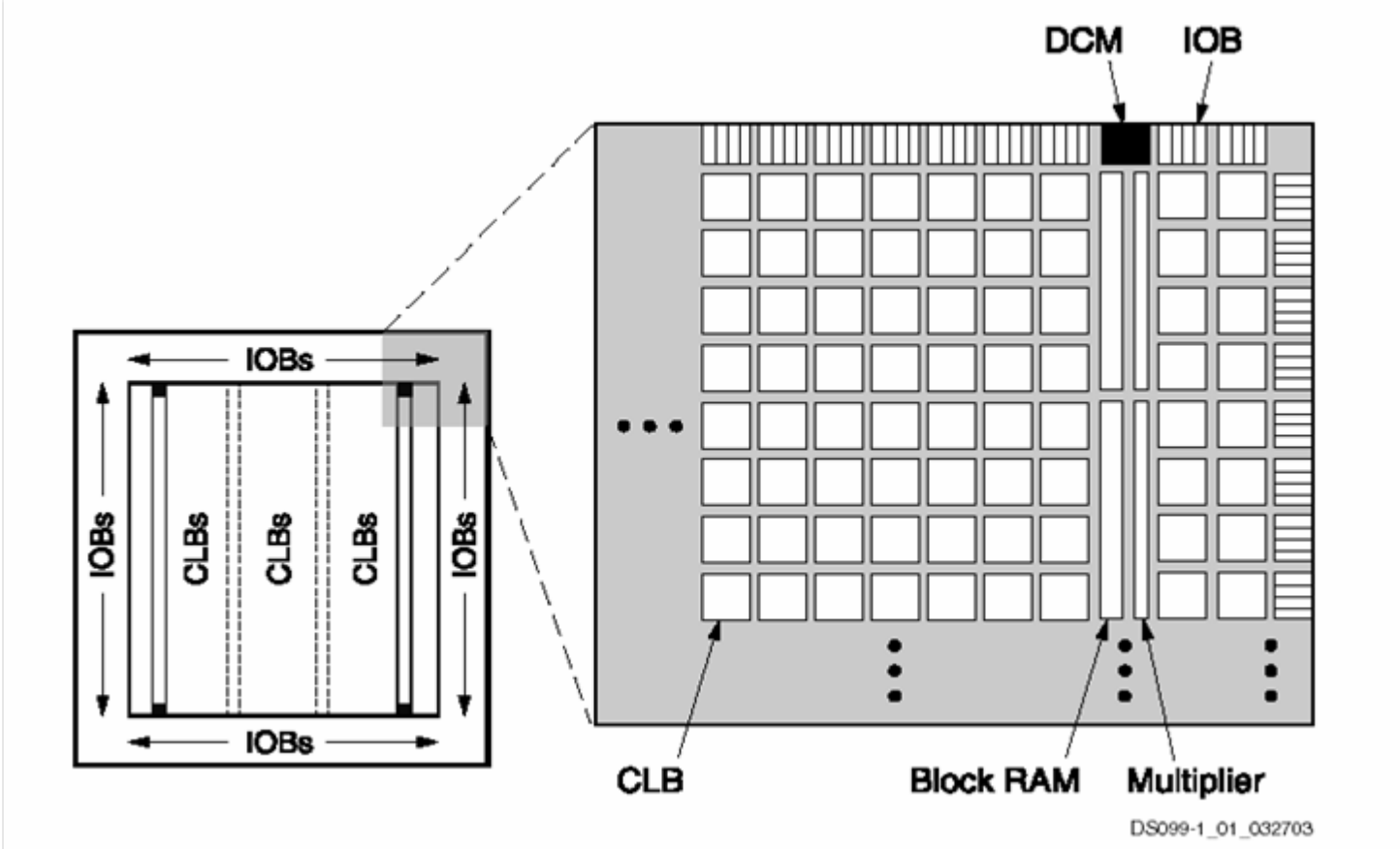
Spartan-3 labkort
Power supplies (2.5V og 1.2V)



Spartan-3 labkort.
Expansion connectors



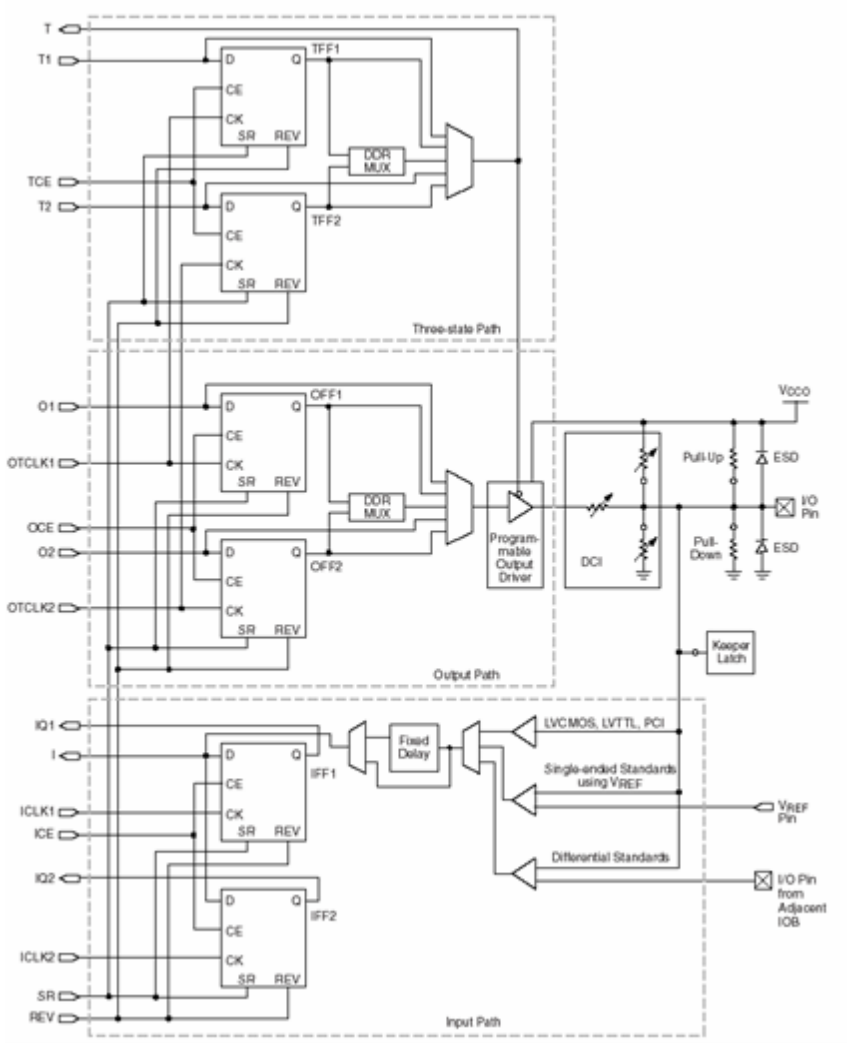
Spartan3-Arkitektur



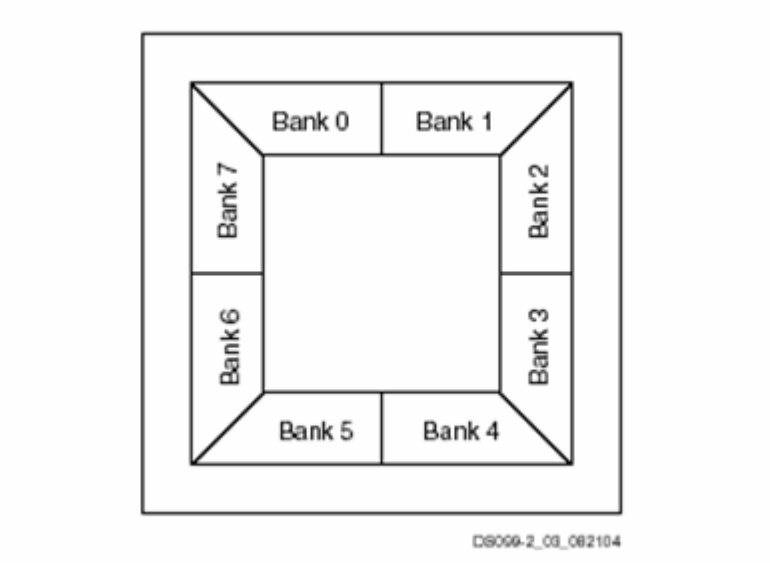
Spartan3-Arkitektur

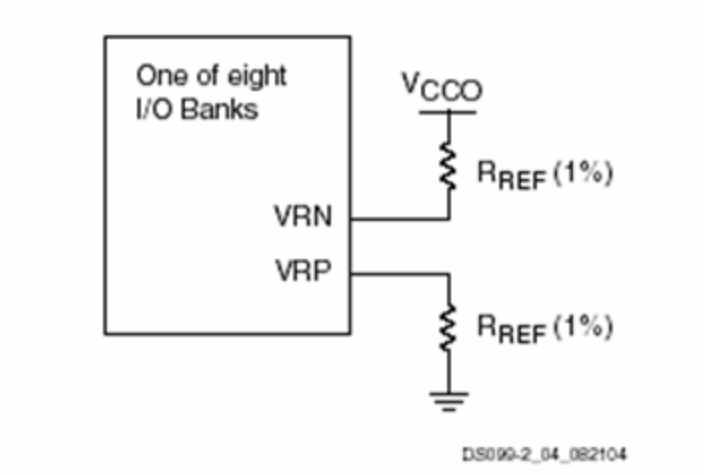
- Input/Output-block
  - Opptil 24 I/O standarder
  - 7 high performance differensial
- CLB-Configurable Logic Blocks
  - SRAM basert LUT (Look-up table)
- Block RAM
  - Dual-port 18kbit i hver
- Hardware multipliers
  - Beregner produkt av to 18bits inputs
  - Viktig for DSP anvendelser
- DCM-Digital clock manager
  - Faseforskyvning, klokkemultiplikasjon/divisjon

Spartan-3 I/O-block



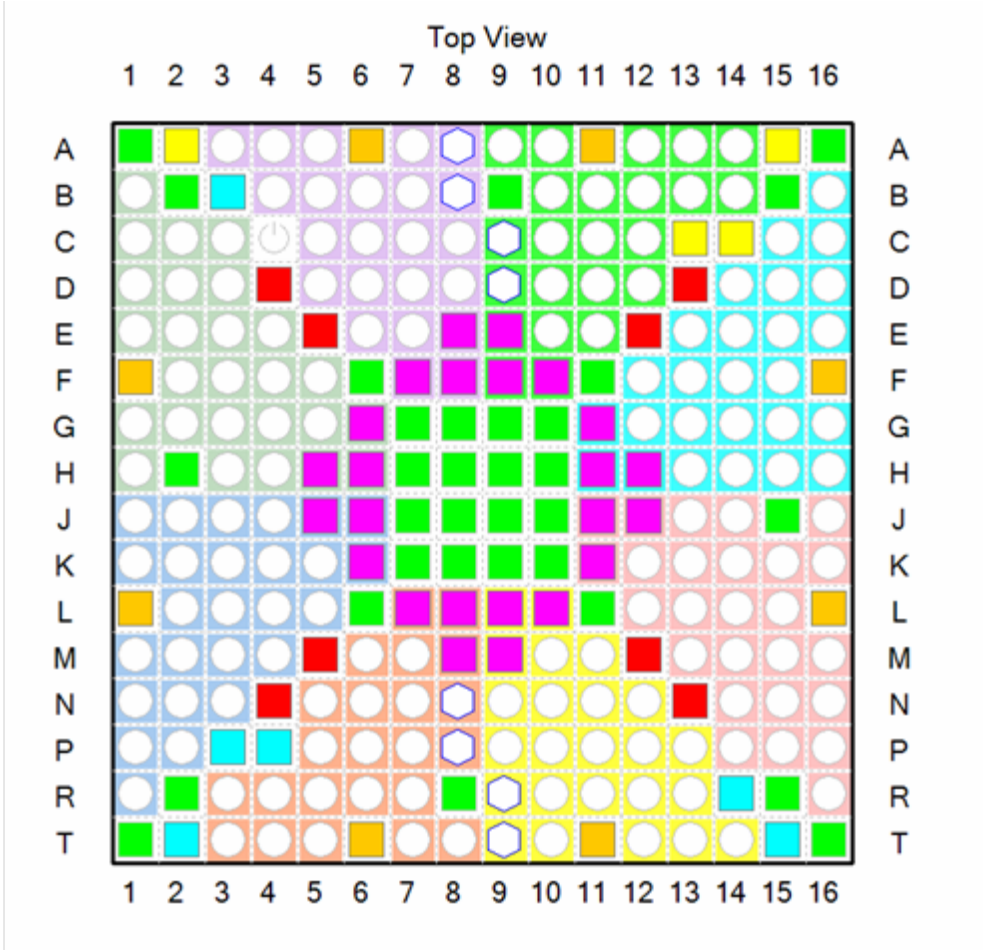
Spartan-3 I/O banker



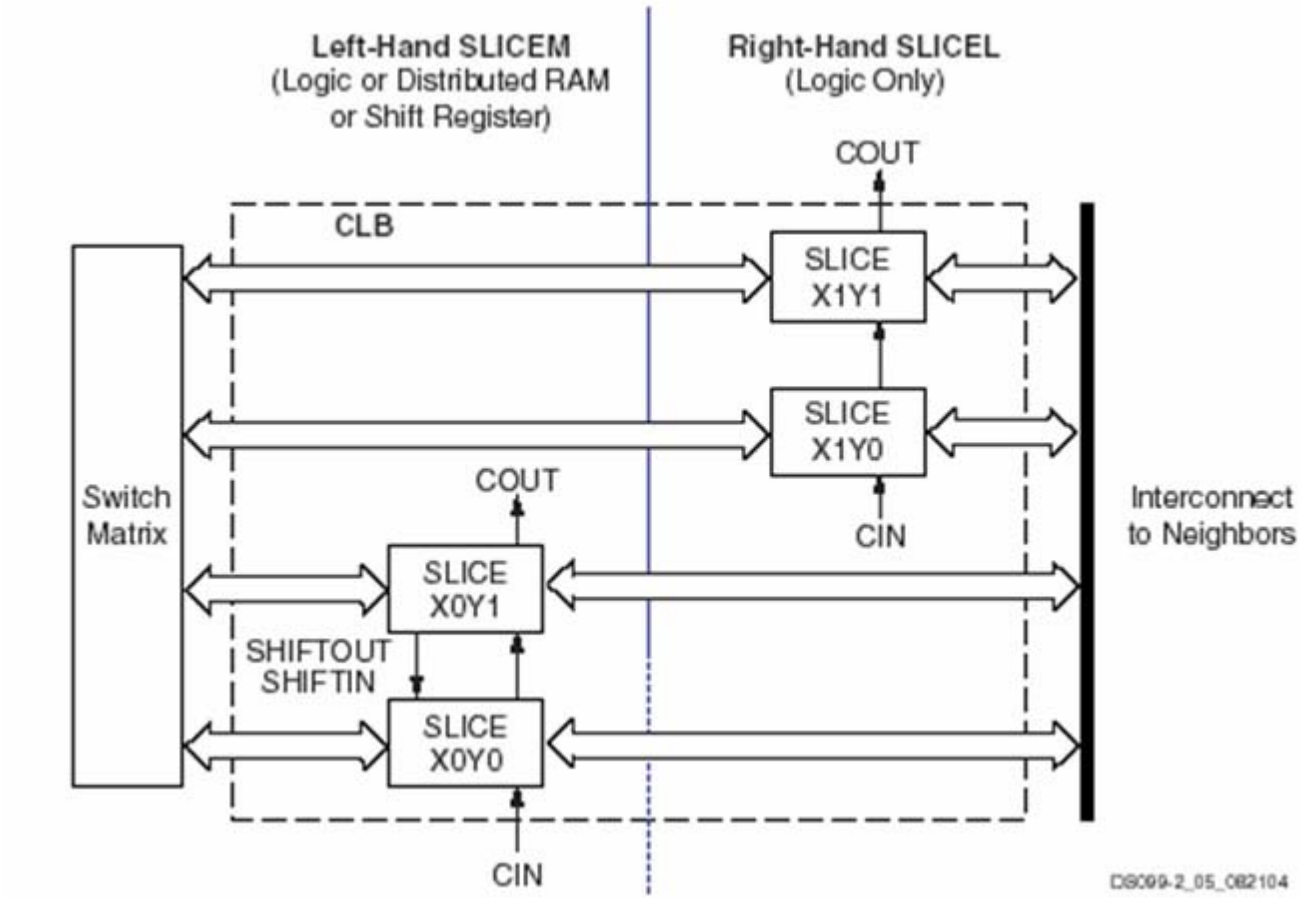


- Samme I/O standard innenfor samme bank
- Viktig å være obs på bank-grenser ved blanding av I/O standarder

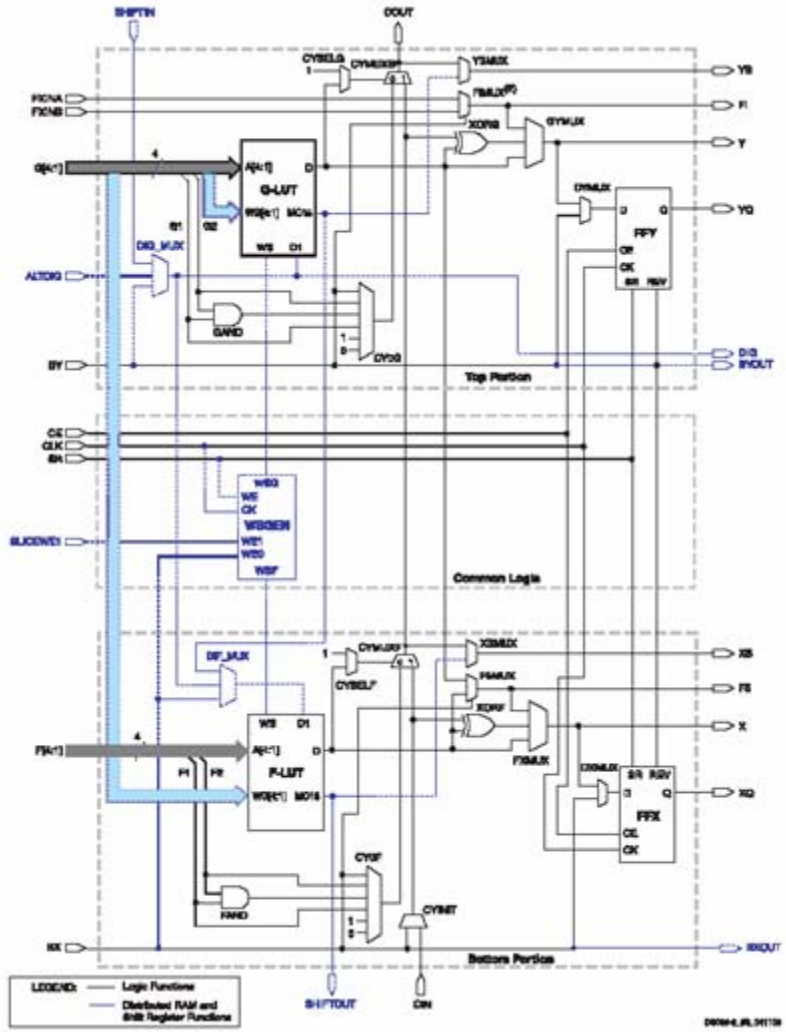
Spartan-3 Pinneplassering ft256



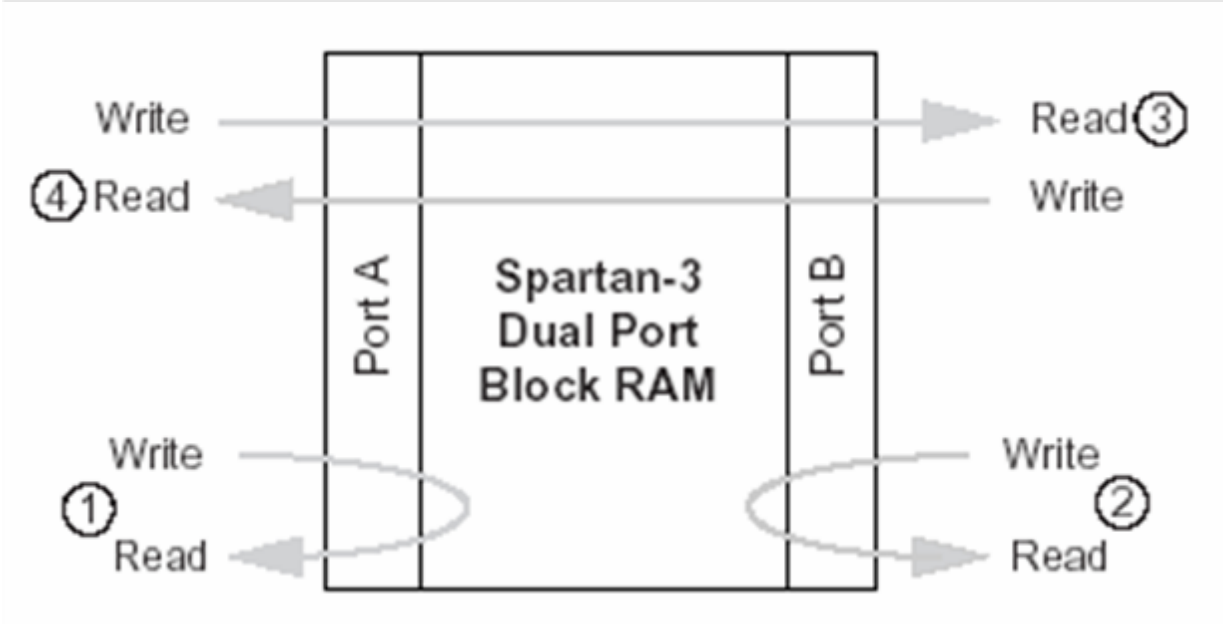
Spartan-3 CLB



Spartan-3 CLB



Spartan-3 Block RAM



Spartan-3 Block RAM

- Anvendelser
  - FIFO First In-First Out buffere
    - Viktig i datakommunikasjon for å lage køer
  - Tilpasning av forskjellige bussbredder
  - Tilpasning av forskjellige klokkedomener
  - Kan brukes som programminne for innebygde prosessorer (jfr. Microblaze)
  - Mellomlager mot eksternt lager (SDRAM)

Spartan-3 Block RAM

Table 10: **Port Aspect Ratios for Port A or B**

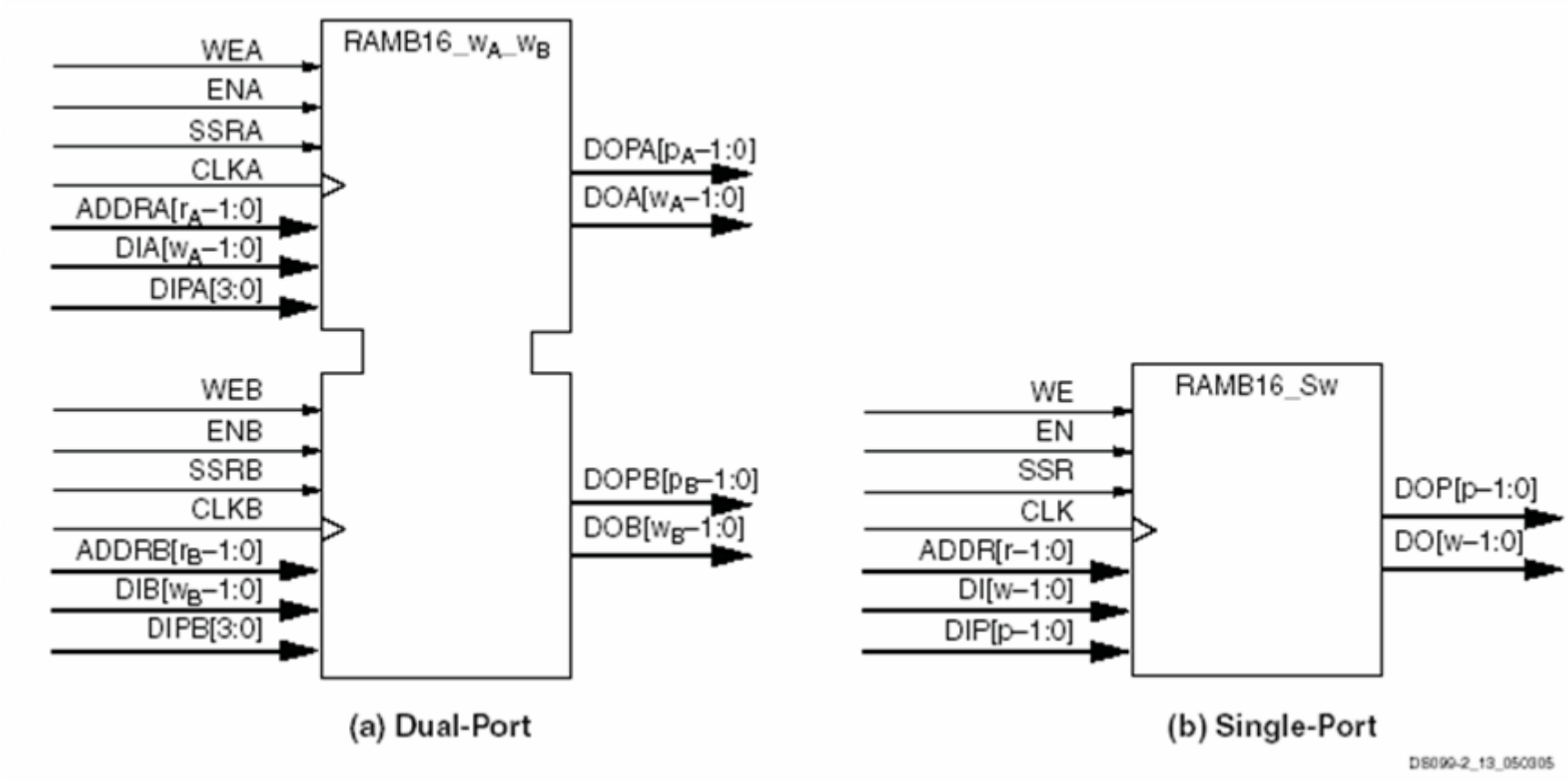
DI/DO Bus Width (w – p bits)	DIP/DOP Bus Width (p bits)	Total Data Path Width (w bits)	ADDR Bus Width (r bits)	No. of Addressable Locations (n)	Block RAM Capacity (bits)
1	0	1	14	16,384	16,384
2	0	2	13	8,192	16,384
4	0	4	12	4,096	16,384
8	1	9	11	2,048	18,432
16	2	18	10	1,024	18,432
32	4	36	9	512	18,432

Spartan-3 Block RAM

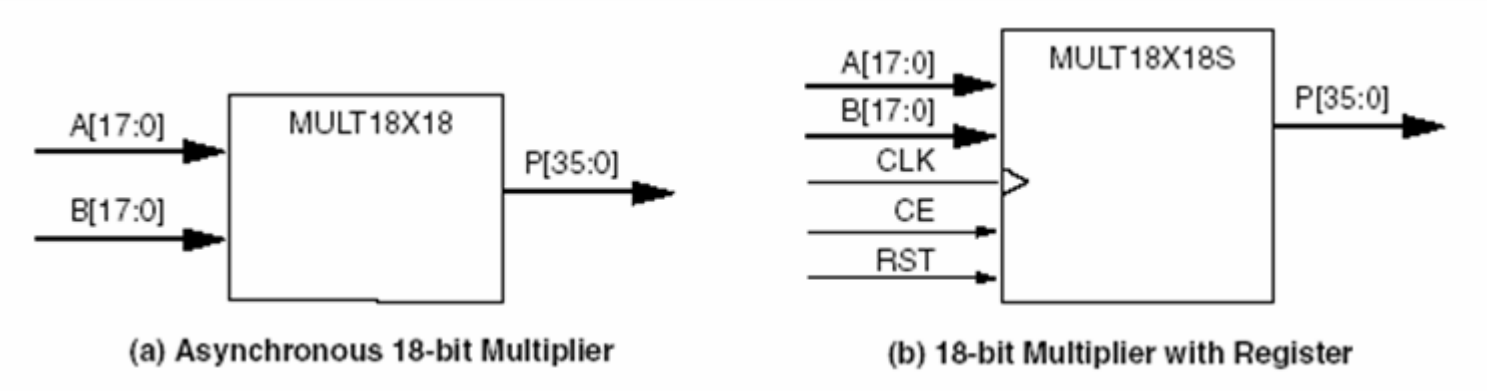
Table 8: **Number of RAM Blocks by Device**

Device	Total Number of RAM Blocks	Total Addressable Locations (bits)	Number of Columns
XC3S50	4	73,728	1
XC3S200	12	221,184	2
XC3S400	16	294,912	2
XC3S1000	24	442,368	2
XC3S1500	32	589,824	2
XC3S2000	40	737,280	2
XC3S4000	96	1,769,472	4
XC3S5000	104	1,916,928	4

Spartan-3 Block RAM



Spartan-3 Multiplikatorer



Spartan-3 DCM

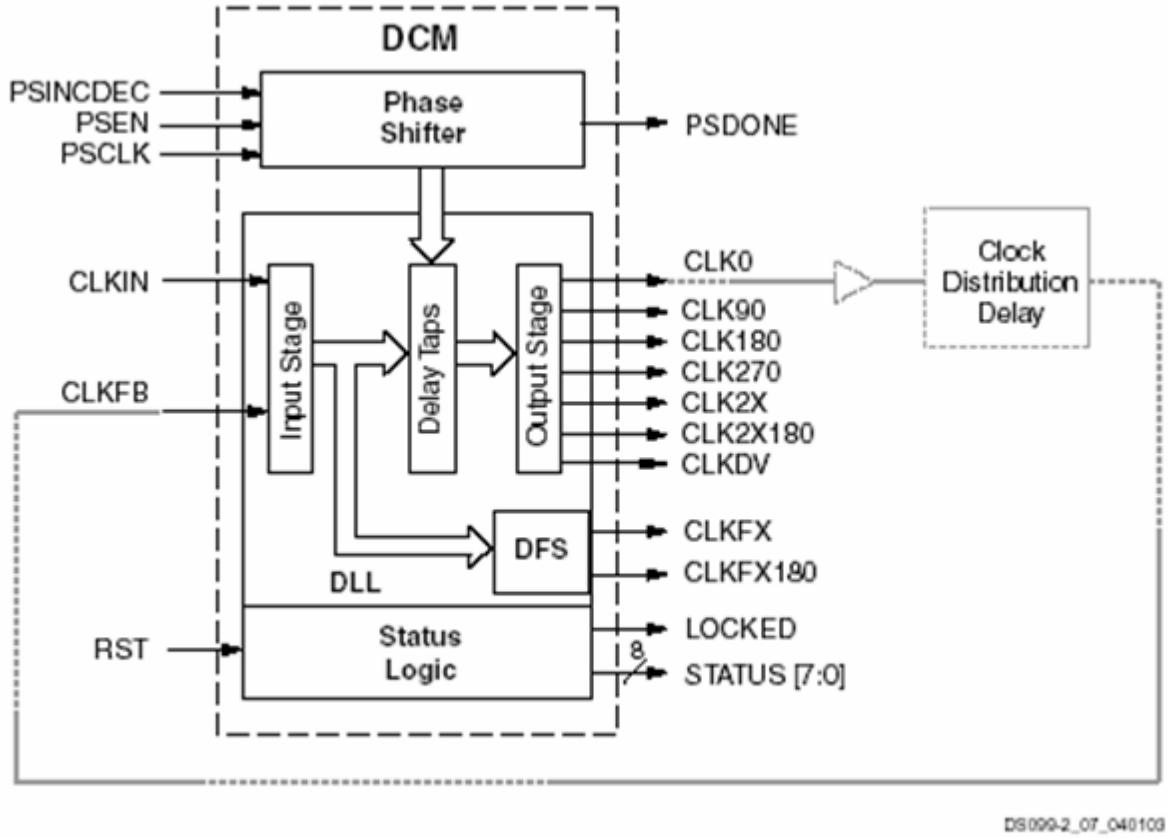


Figure 13: **DCM Functional Blocks and Associated Signals**

Spartan-3 DCM

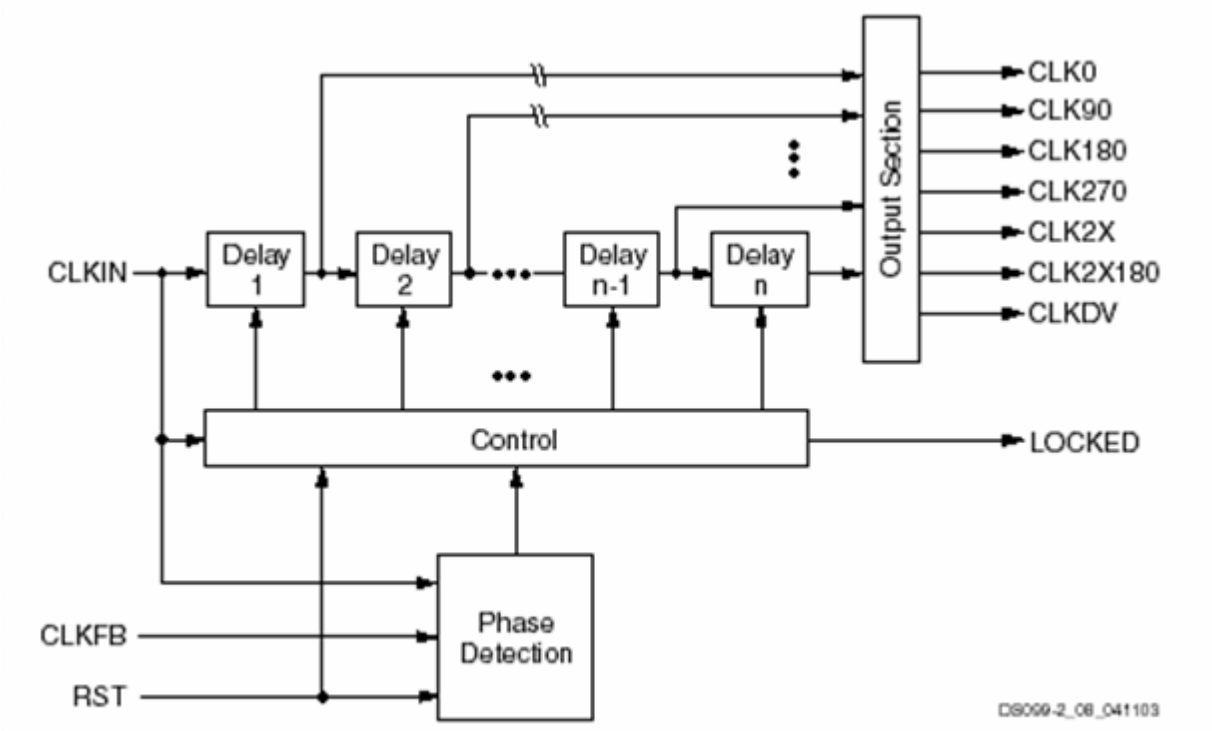


Figure 14: **Simplified Functional Diagram of DLL**