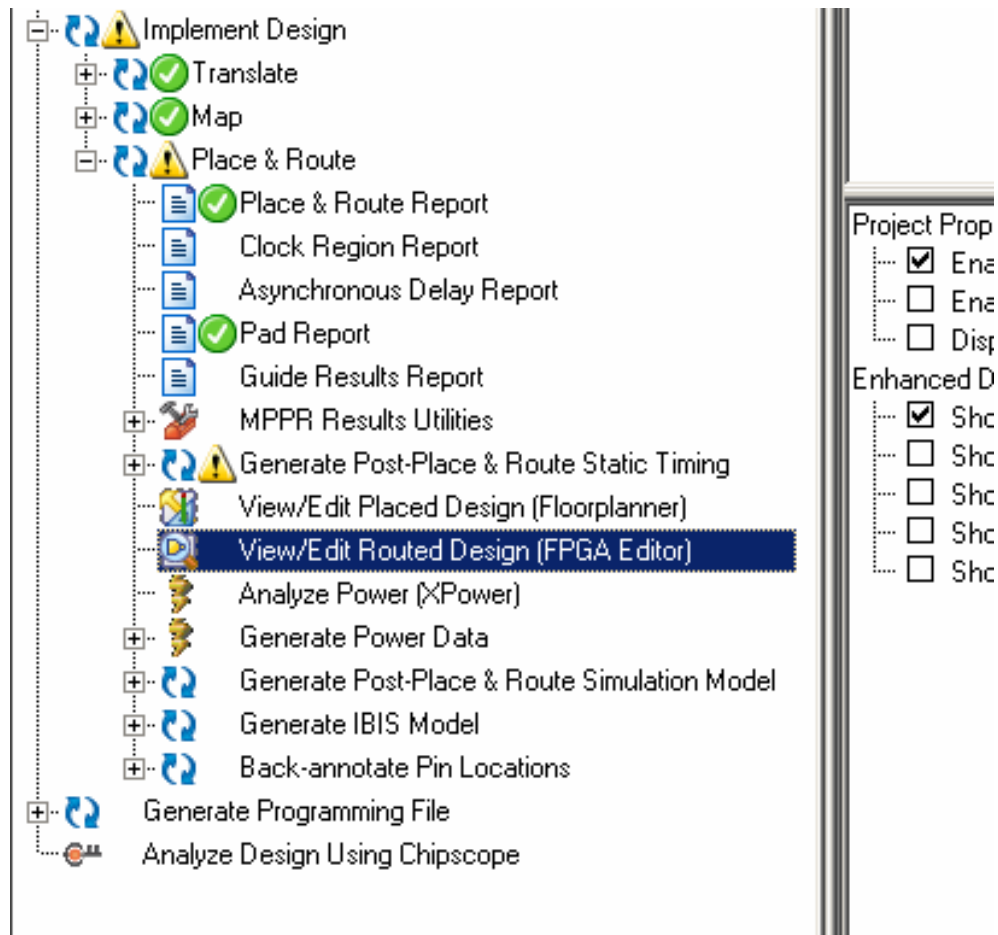
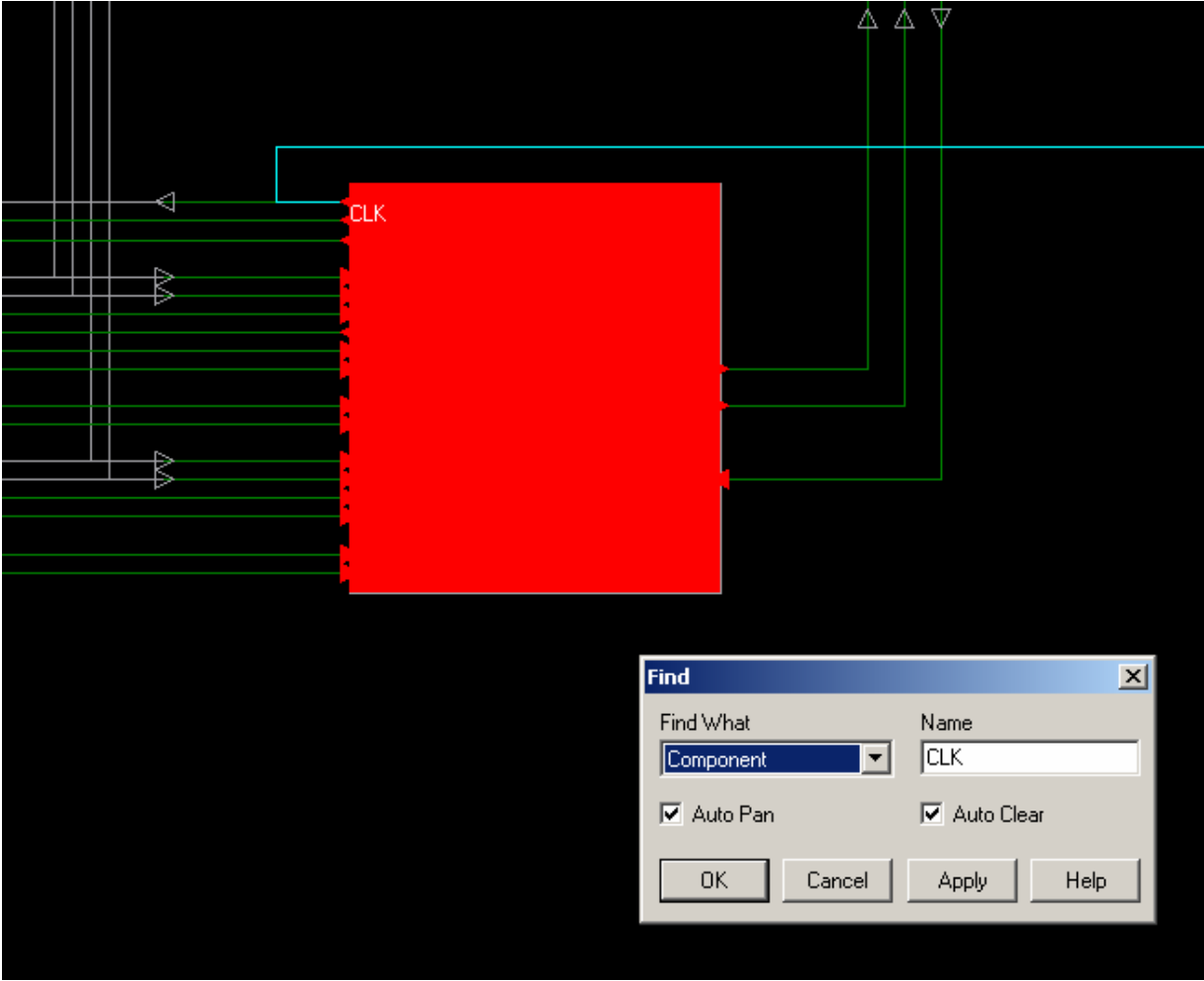


FPGA editor



Clock pad



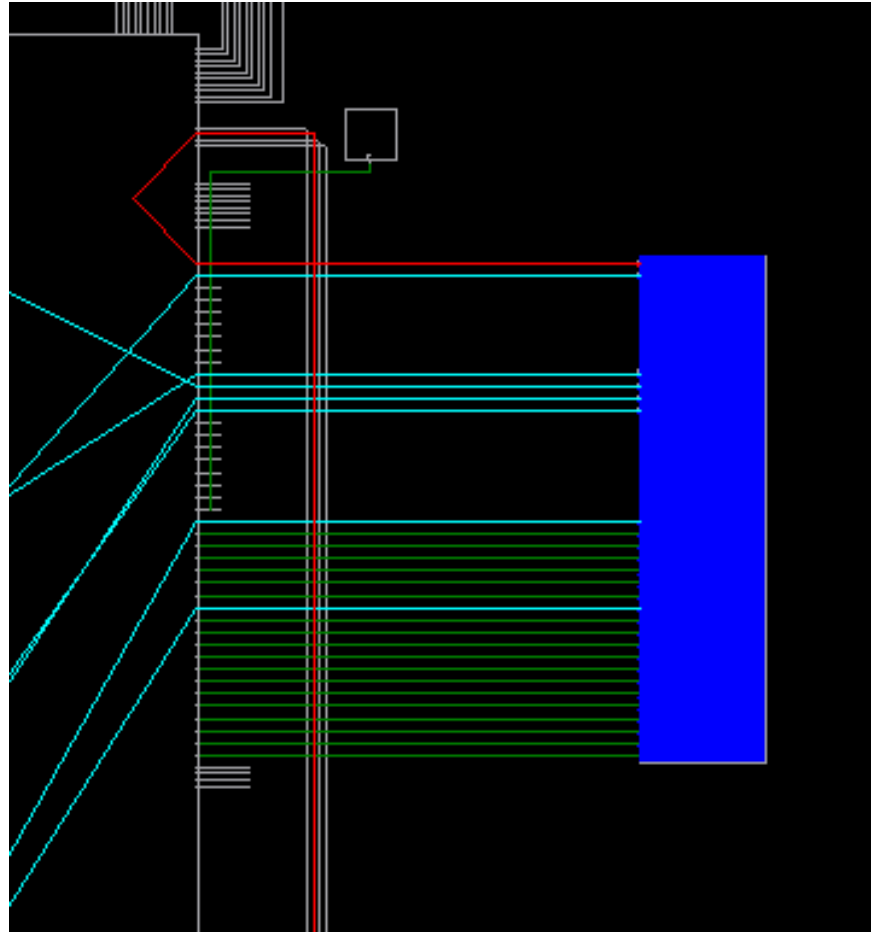
Pad output

The screenshot shows a logic simulator interface. A central circuit diagram features a blue rectangular component with a red arrow labeled 'CLK' pointing to its top-left corner. Multiple green lines represent signal paths connecting the component to various parts of the circuit. A 'Find' dialog box is open in the foreground, with 'Component' selected in the 'Find What' dropdown and 'CLK' entered in the 'Name' field. The 'Auto Pan' and 'Auto Clear' checkboxes are checked. Below the circuit, a component list table is visible, and a 'World1' window shows a blue rectangular area on a black background. At the bottom left, a text label reads 'net "CLK_IBUFG"'. The status bar at the bottom center contains the text 'INF3430 - H08'.

3	ABCDEF	H14	IOB	1
4	ABCDEF	H15	IOB	1
5	ABCDEF	N12	IOB	1
6	ABCDEF	E11	IOB	1
7	ABCDEF	C11	IOB	1
8	ABCDEF	SLICE_X	SLICEL	10
9	ABCDEF	SLICE_X	SLICEL	10
10	ABCDEF	SLICE_X	SLICEL	10
11	ABCDEF	SLICE_X	SLICEL	10
12	ABCDEF	SLICE_X	SLICEL	10
13	ABCDEF	SLICE_X	SLICEL	10
14	ABCDEF	SLICE_X	SLICEL	10
15	AN<0>	P5	IOB	1
16	AN<1>	M10	IOB	1
17	AN<2>	N10	IOB	1
18	AN<3>	C10	IOB	1

net "CLK_IBUFG"

DCM module



INF3430 - H08

Clock0

The diagram shows a routing path for the signal 'Clock0'. On the left, a vertical bus of signals is shown, with a red line indicating the selected signal. This signal is routed through a series of vertical and horizontal lines to a blue rectangular logic block on the right. The routing is highlighted in red and cyan.

	Name	Src	Type	Wires
1	ABCDEF	H16	IOB	1
2	ABCDEF	H13	IOB	1
3	ABCDEF	H14	IOB	1
4	ABCDEF	H15	IOB	1
5	ABCDEF	N12	IOB	1
6	ABCDEF	E11	IOB	1
7	ABCDEF	C11	IOB	1
8	ABCDEF	SLICE_X	SLICEL	10
9	ABCDEF	SLICE_X	SLICEL	10
10	ABCDEF	SLICE_X	SLICEL	10
11	ABCDEF	SLICE_X	SLICEL	10
12	ABCDEF	SLICE_X	SLICEL	10
13	ABCDEF	SLICE_X	SLICEL	10
14	ABCDEF	SLICE_X	SLICEL	10
15	AN<0>	P5	IOB	1
16	AN<1>	M10	IOB	1
17	AN<2>	N10	IOB	1
18	AN<3>	C10	IOB	1

World1

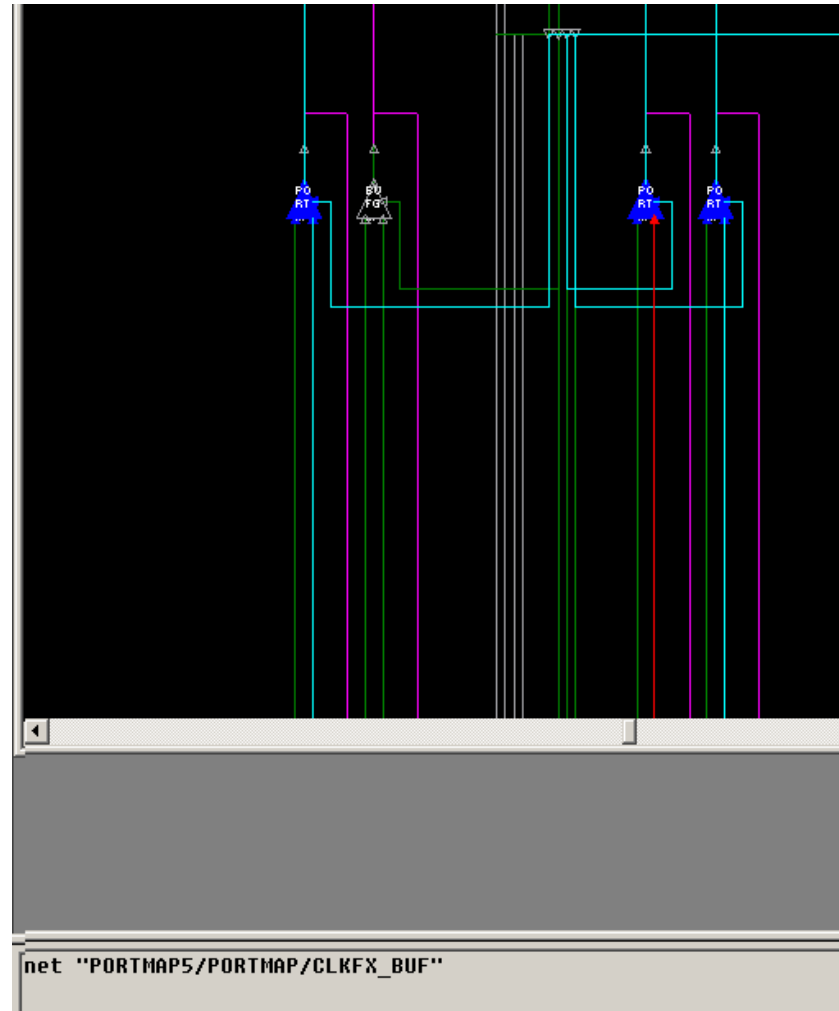
```
net "PORTMAP5/PORTMAP/CLK0_OUT"
```

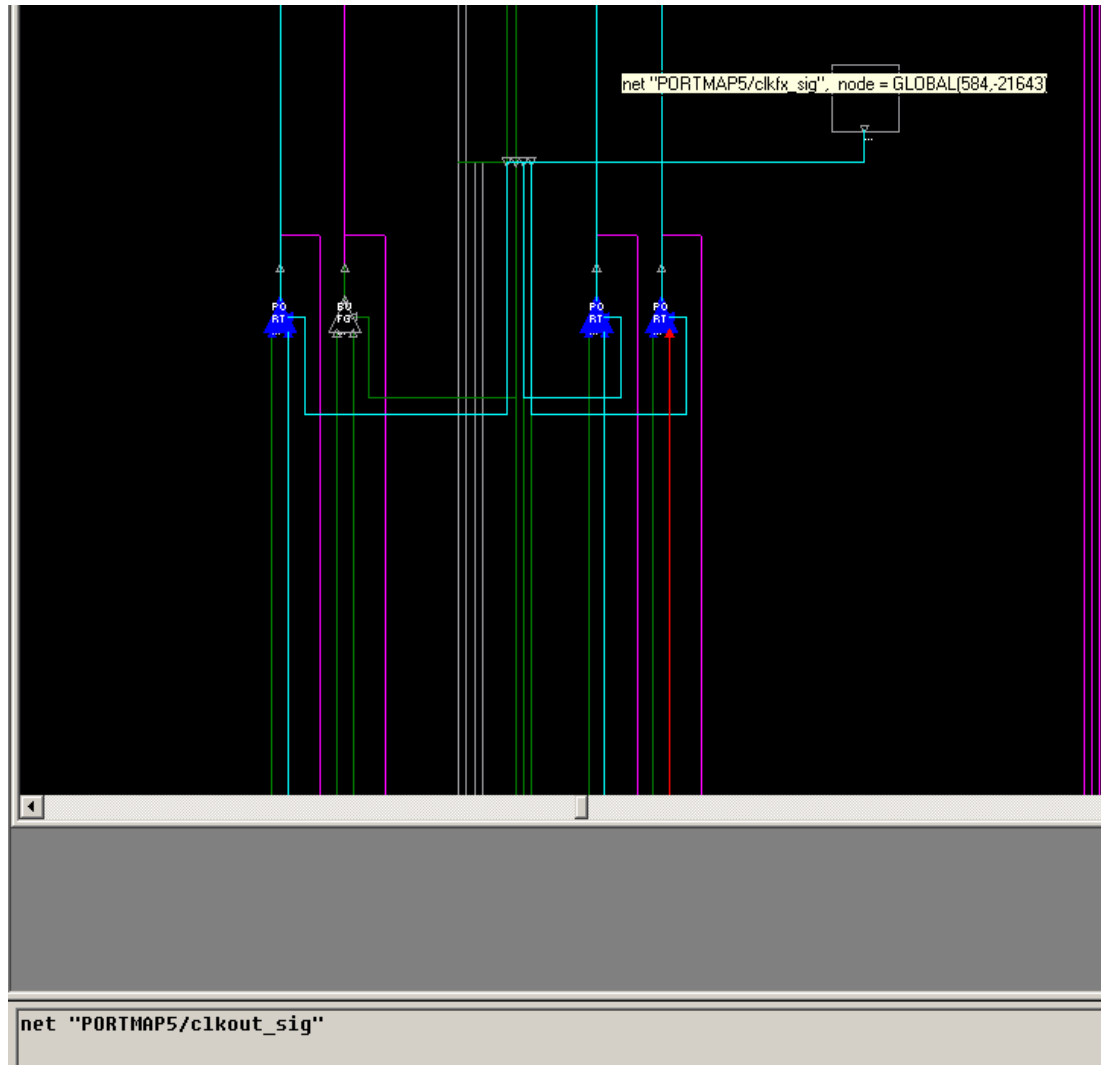
CLKFX net

	Name	Site	Type	#Pins
1	ABCDEF	H16	IOB	1
2	ABCDEF	H13	IOB	1
3	ABCDEF	H14	IOB	1
4	ABCDEF	H15	IOB	1
5	ABCDEF	N12	IOB	1
6	ABCDEF	E11	IOB	1
7	ABCDEF	C11	IOB	1
8	ABCDEF	SLICE_X	SLICEL	10
9	ABCDEF	SLICE_X	SLICEL	10
10	ABCDEF	SLICE_X	SLICEL	10
11	ABCDEF	SLICE_X	SLICEL	10
12	ABCDEF	SLICE_X	SLICEL	10
13	ABCDEF	SLICE_X	SLICEL	10
14	ABCDEF	SLICE_X	SLICEL	10
15	AN<0>	P5	IOB	1
16	AN<1>	M10	IOB	1
17	AN<2>	N10	IOB	1
18	AN<3>	C10	IOB	1

net "PORTMAP5/PORTMAP/CLKFX_BUF"

BUFG





Statisk timing analyse setup

The screenshot displays a static timing analysis setup in a CAD tool. The main window shows a circuit diagram with various components and connections. A table on the right lists constraints for various signals and components. A small inset window shows a top-level view of the design.

1	ABCDEF	H16	IOB	1
2	ABCDEF	H13	IOB	1
3	ABCDEF	H14	IOB	1
4	ABCDEF	H15	IOB	1
5	ABCDEF	N12	IOB	1
6	ABCDEF	E11	IOB	1
7	ABCDEF	C11	IOB	1
8	ABCDEF	SLICE_X	SLICEL	10
9	ABCDEF	SLICE_X	SLICEL	10
10	ABCDEF	SLICE_X	SLICEL	10
11	ABCDEF	SLICE_X	SLICEL	10
12	ABCDEF	SLICE_X	SLICEL	10
13	ABCDEF	SLICE_X	SLICEL	10
14	ABCDEF	SLICE_X	SLICEL	10
15	AN<0>	P5	IOB	1
16	AN<1>	M10	IOB	1
17	AN<2>	N10	IOB	1
18	AN<3>	C10	IOB	1

World1

net "CLK_div"

UCF file

```
NET "CLK" TNM_NET = "CLK_GRP";  
TIMESPEC "TS_CLK" = PERIOD "CLK_GRP" 20 ns HIGH 50 %;  
  
NET "PORTMAP5/PORTMAP/CLKFX_BUF" TNM = "CLKFX_BUF_GRP";  
NET "PORTMAP5/clkout_sig" TNM = "clk_div_grp";  
  
TIMESPEC "TS_clk_div" = PERIOD "clk_div_grp" 330 ns HIGH 50%;  
TIMESPEC "TS_CLKFX_BUF_GRP_2_clk_div_grp" = FROM "CLKFX_BUF_GRP" TO "clk_div_grp" 20.0 ns;  
  
TIMESPEC "TS_P2P" = FROM "PADS" TO "PADS" 40 ns;  
TIMESPEC "TS_P2FFS" = FROM "PADS" TO "FFS" 10 ns;  
TIMESPEC "TS_FFS2P" = FROM "FFS" TO "PADS" 10 ns;
```