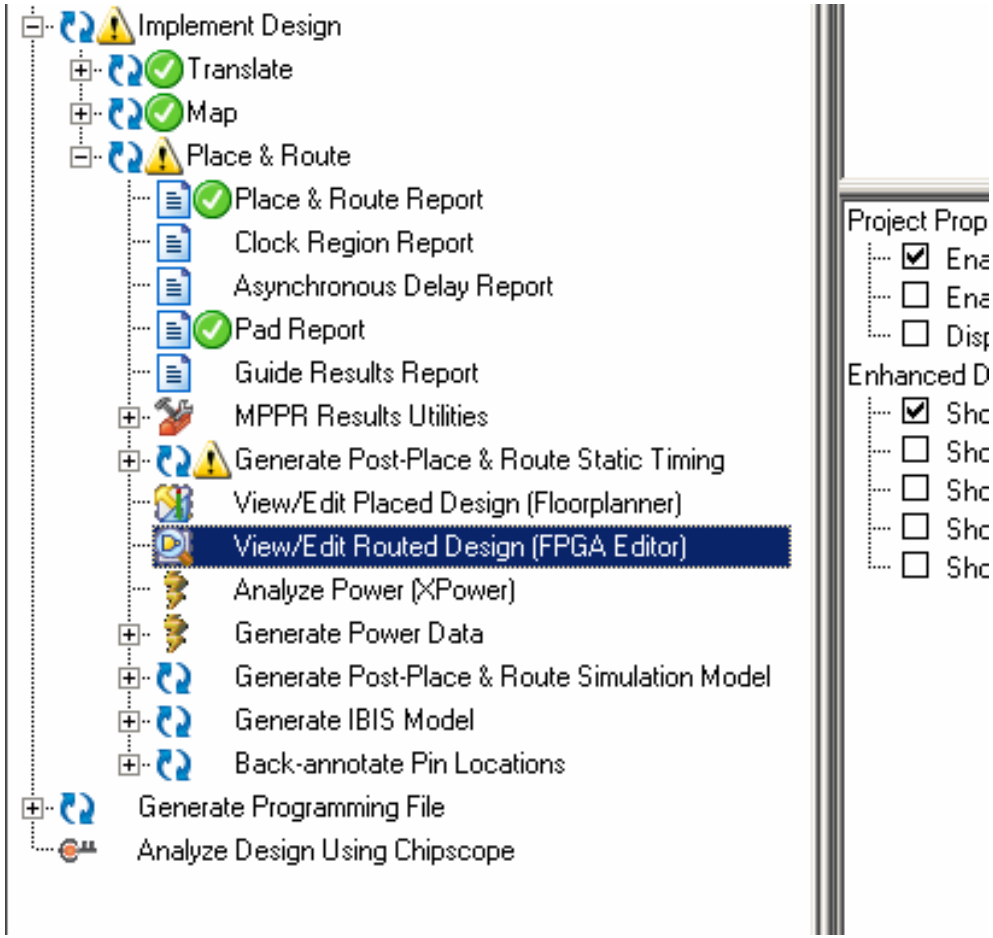
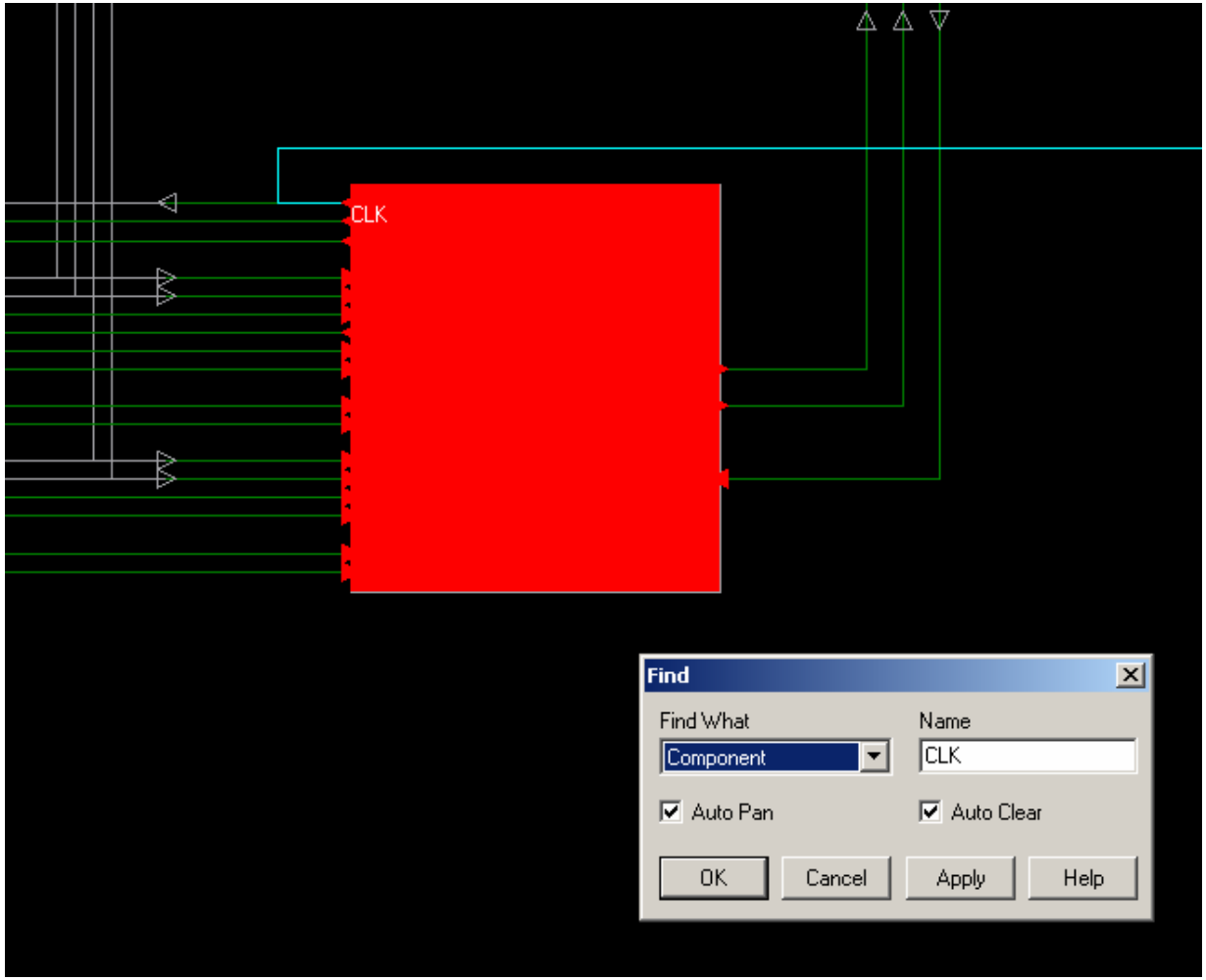
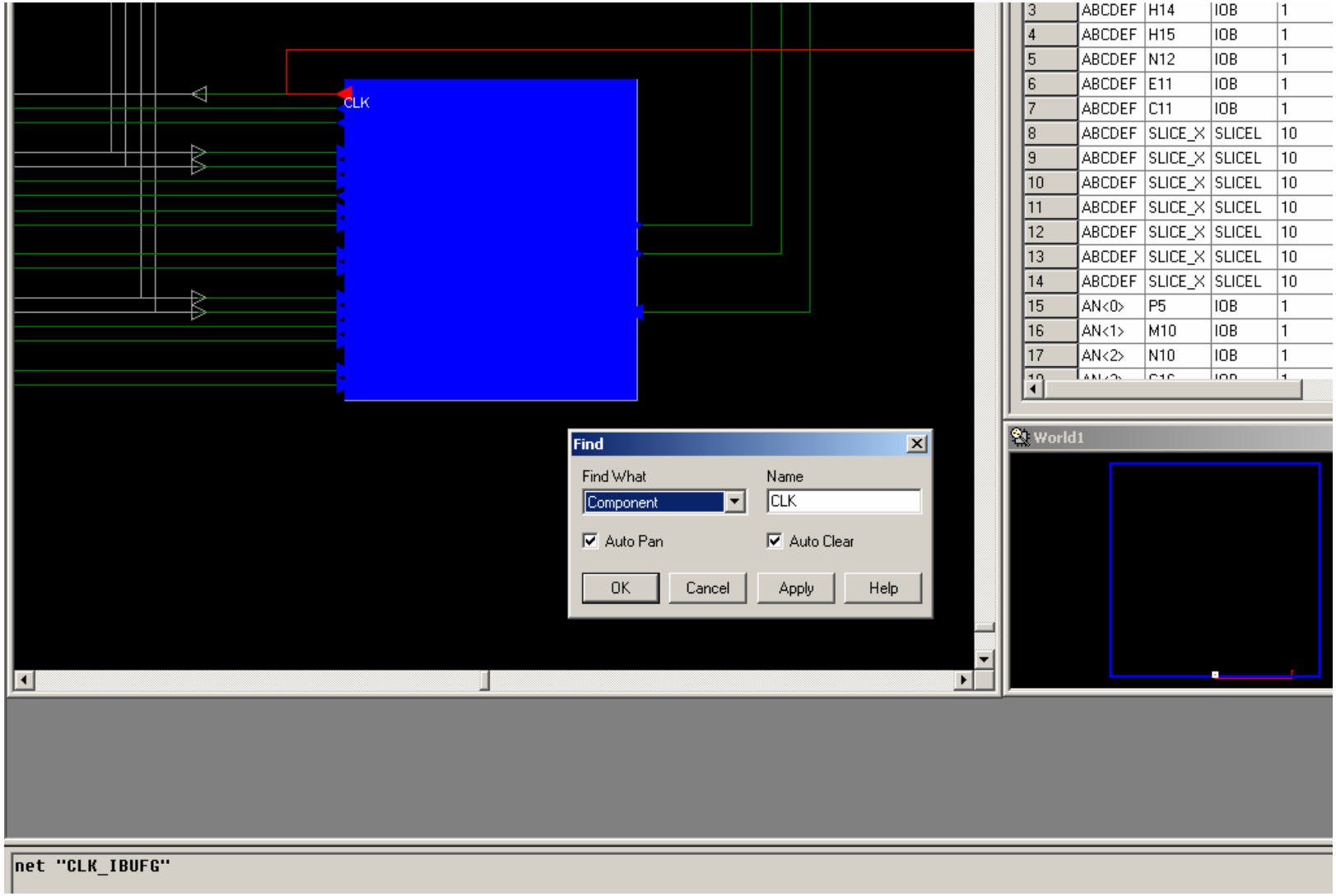
FPGA editor


Implement Design
Translate
Map
Place & Route
Place & Route Report
Clock Region Report
Asynchronous Delay Report
Pad Report
Guide Results Report
MPPR Results Utilities
Generate Post-Place & Route Static Timing
View/Edit Placed Design (Floorplanner)
View/Edit Routed Design (FPGA Editor)
Analyze Power (XPower)
Generate Power Data
Generate Post-Place & Route Simulation Model
Generate IBIS Model
Back-annotate Pin Locations
Generate Programming File
Analyze Design Using Chipscope
Project Prop
Enhanced D

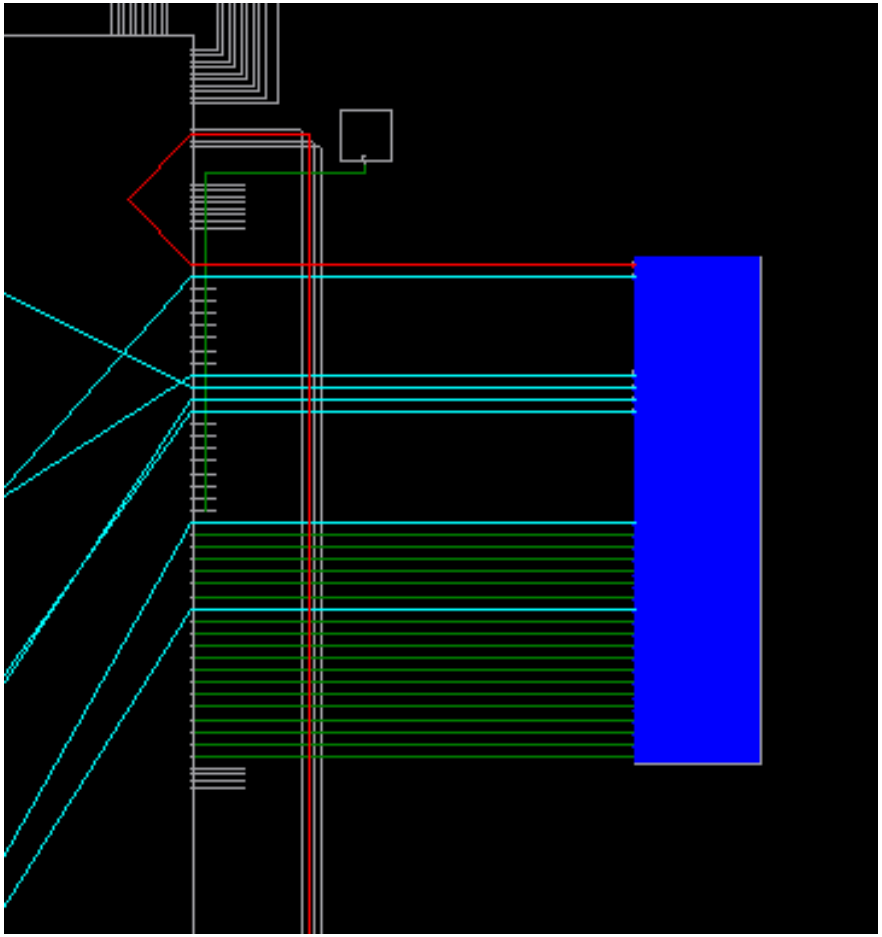
Clock pad


CLK
Find
Find What
Component
Name
CLK
Auto Pan
Auto Clear
OK
Cancel
Apply
Help

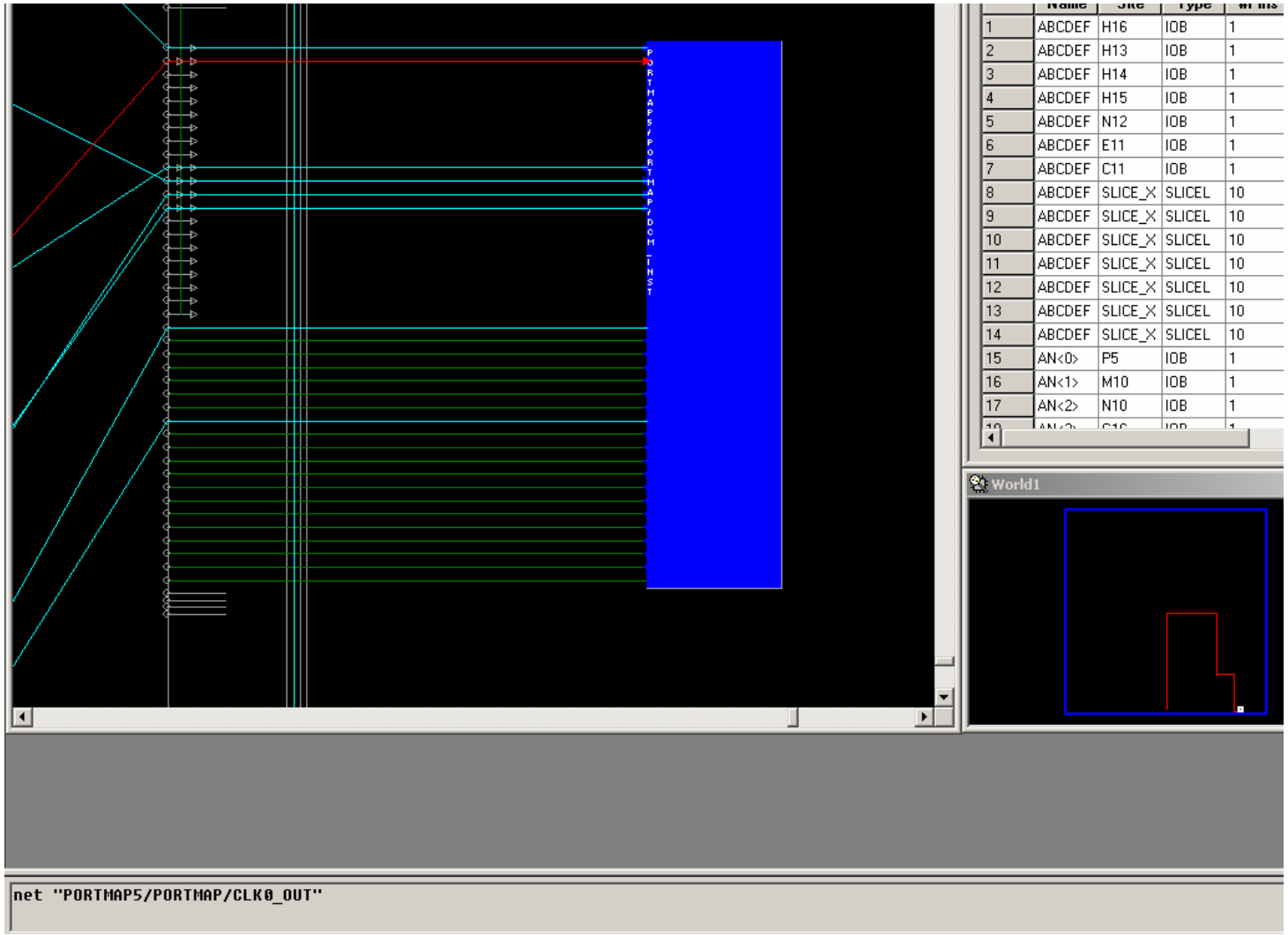
Pad output


CLK
Find
Find What
Component
Name
CLK
Auto Pan
Auto Clear
OK
Cancel
Apply
Help
World1
3 ABCDEF H14 IOB 1
4 ABCDEF H15 IOB 1
5 ABCDEF N12 IOB 1
6 ABCDEF E11 IOB 1
7 ABCDEF C11 IOB 1
8 ABCDEF SLICE_X SLICEL 10
9 ABCDEF SLICE_X SLICEL 10
10 ABCDEF SLICE_X SLICEL 10
11 ABCDEF SLICE_X SLICEL 10
12 ABCDEF SLICE_X SLICEL 10
13 ABCDEF SLICE_X SLICEL 10
14 ABCDEF SLICE_X SLICEL 10
15 AN<0> P5 IOB 1
16 AN<1> M10 IOB 1
17 AN<2> N10 IOB 1
net "CLK_IBUFG"

DCM module

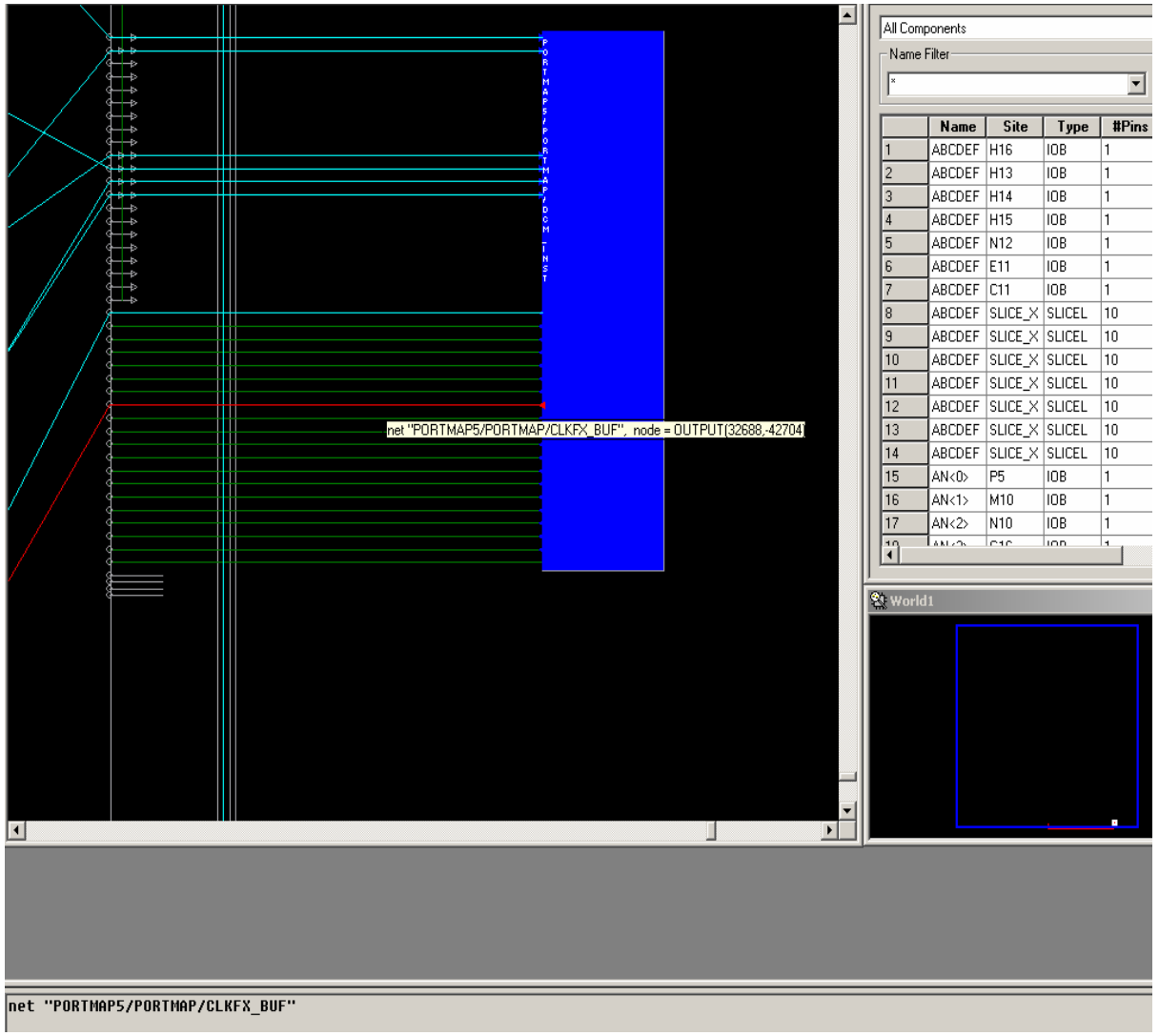


Clock0

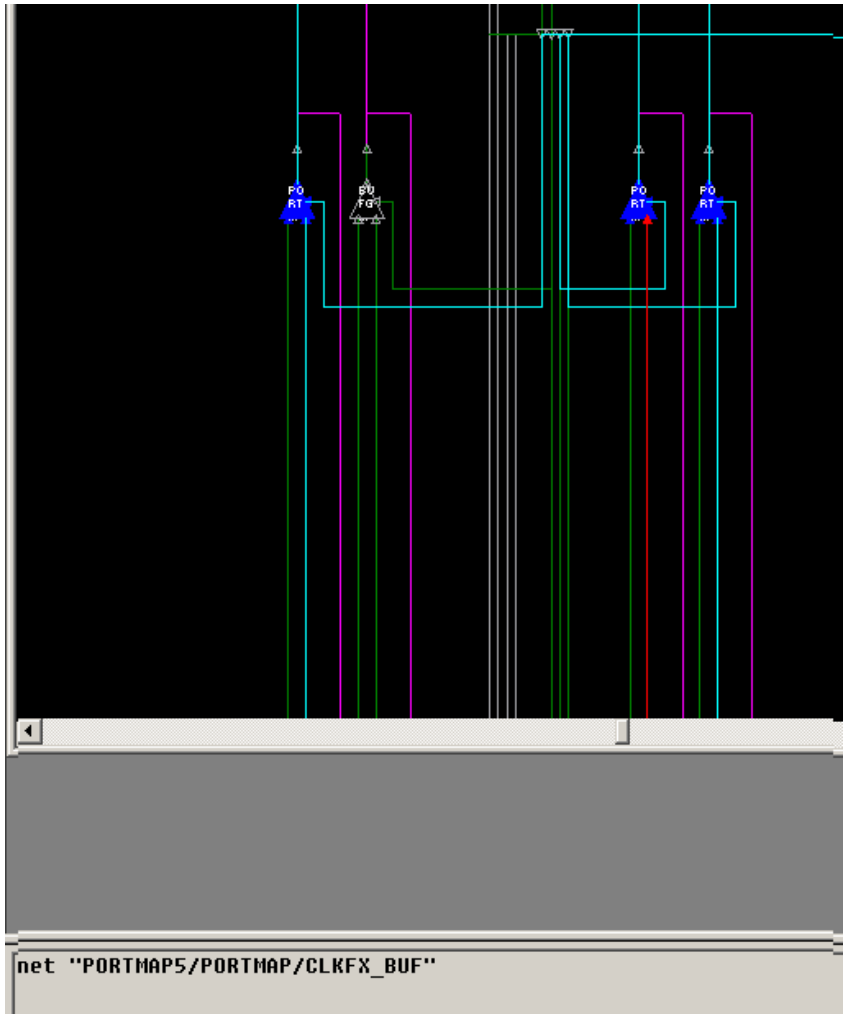


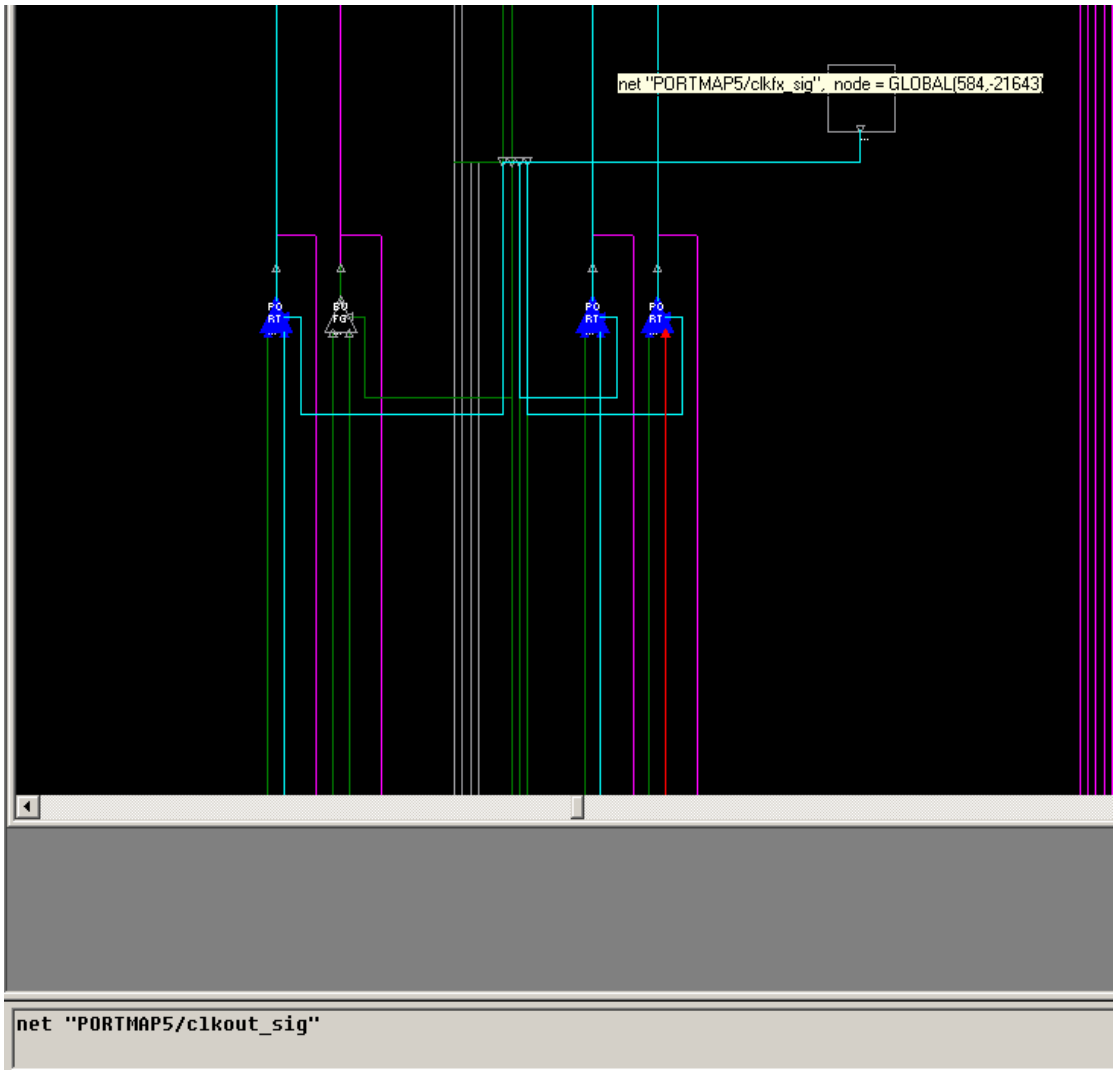
	Name	Site	Type	#Pins
1	ABCDEF	H16	IOB	1
2	ABCDEF	H13	IOB	1
3	ABCDEF	H14	IOB	1
4	ABCDEF	H15	IOB	1
5	ABCDEF	N12	IOB	1
6	ABCDEF	E11	IOB	1
7	ABCDEF	C11	IOB	1
8	ABCDEF	SLICE_X	SLICEL	10
9	ABCDEF	SLICE_X	SLICEL	10
10	ABCDEF	SLICE_X	SLICEL	10
11	ABCDEF	SLICE_X	SLICEL	10
12	ABCDEF	SLICE_X	SLICEL	10
13	ABCDEF	SLICE_X	SLICEL	10
14	ABCDEF	SLICE_X	SLICEL	10
15	AN<0>	P5	IOB	1
16	AN<1>	M10	IOB	1
17	AN<2>	N10	IOB	1

CLKFX net

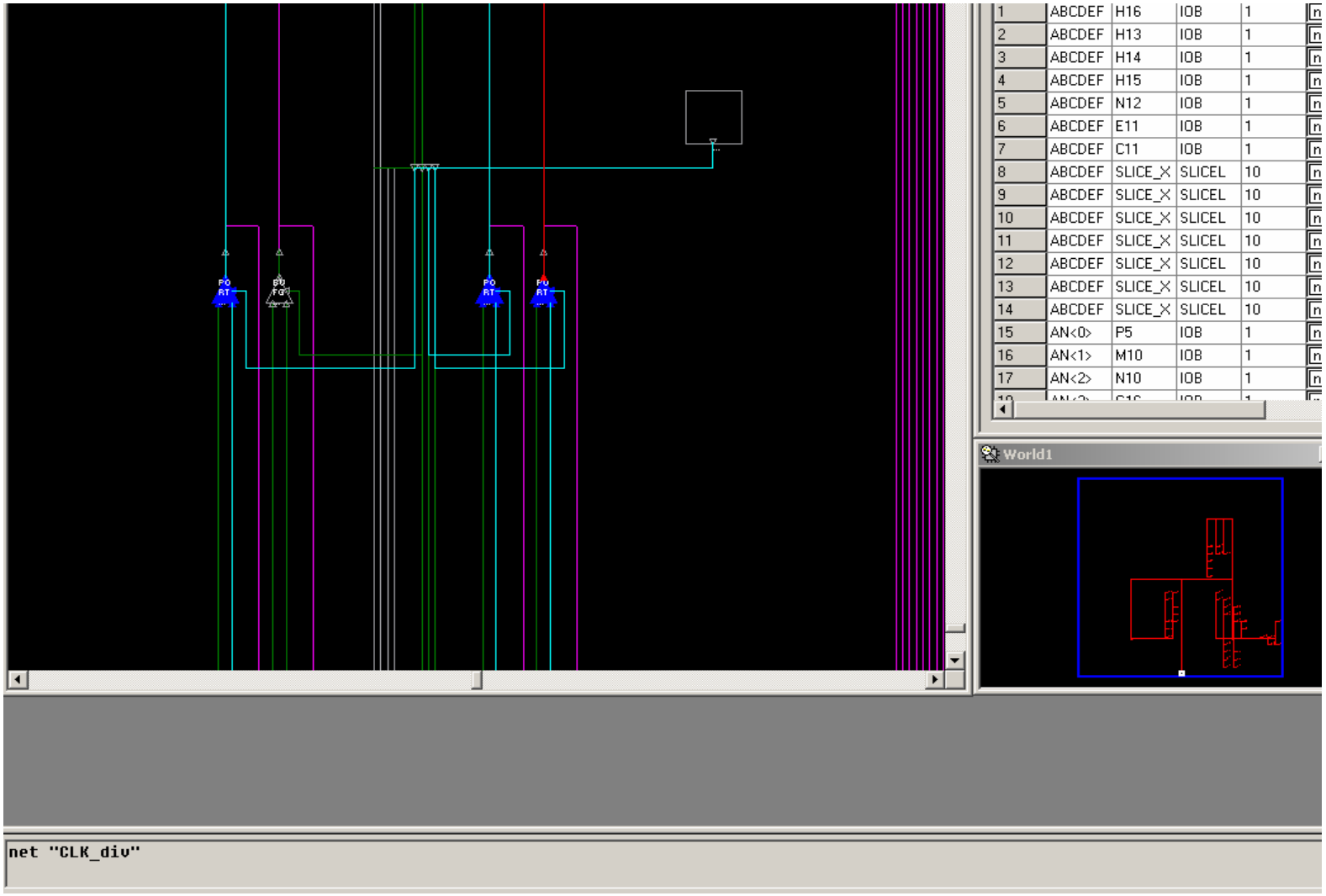

net "PORTMAP5/PORTMAP/CLKFX_BUF", node = OUTPUT(32688,-42704
All Components
Name Filter
Name Site Type #Pins
1 ABCDEF H16 IOB 1
2 ABCDEF H13 IOB 1
3 ABCDEF H14 IOB 1
4 ABCDEF H15 IOB 1
5 ABCDEF N12 IOB 1
6 ABCDEF E11 IOB 1
7 ABCDEF C11 IOB 1
8 ABCDEF SLICE_X SLICEL 10
9 ABCDEF SLICE_X SLICEL 10
10 ABCDEF SLICE_X SLICEL 10
11 ABCDEF SLICE_X SLICEL 10
12 ABCDEF SLICE_X SLICEL 10
13 ABCDEF SLICE_X SLICEL 10
14 ABCDEF SLICE_X SLICEL 10
15 AN<0> P5 IOB 1
16 AN<1> M10 IOB 1
17 AN<2> N10 IOB 1
World1
net "PORTMAP5/PORTMAP/CLKFX_BUF"

BUFG




net "PORTMAP5/clkfx_sig", node = GLOBAL(584,-21643)
net "PORTMAP5/clkout_sig"

Statisk timing analyse setup



UCF filen

```
NET "CLK" TNM_NET = "CLK_GRP";
TIMESPEC "TS_CLK" = PERIOD "CLK_GRP" 20 ns HIGH 50 %;

NET "PORTMAP5/PORTMAP/CLKFX_BUF" TNM = "CLKFX_BUF_GRP";
NET "PORTMAP5/clkout_sig" TNM = "clk_div_grp";

TIMESPEC "TS_clk_div" = PERIOD "clk_div_grp" 330 ns HIGH 50%;
TIMESPEC "TS_CLKFX_BUF_GRP_2_clk_div_grp" = FROM "CLKFX_BUF_GRP" TO "clk_div_grp" 20.0 ns;

TIMESPEC "TS_P2P"   = FROM "PADS" TO "PADS" 40 ns;
TIMESPEC "TS_P2FFS" = FROM "PADS" TO "FFS" 10 ns;
TIMESPEC "TS_FFS2P" = FROM "FFS" TO "PADS" 10 ns;
```