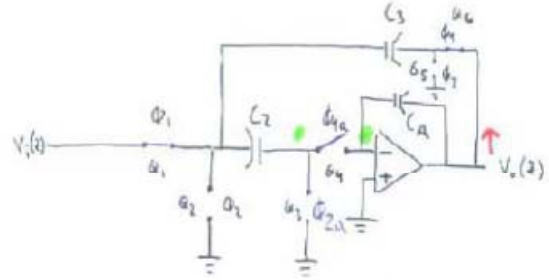
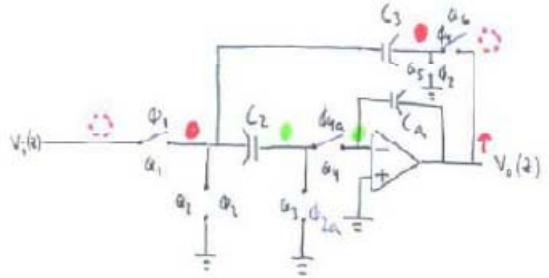
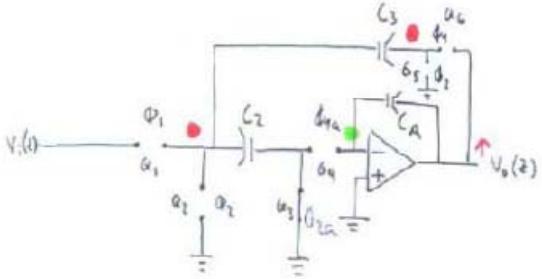
Charge Injection

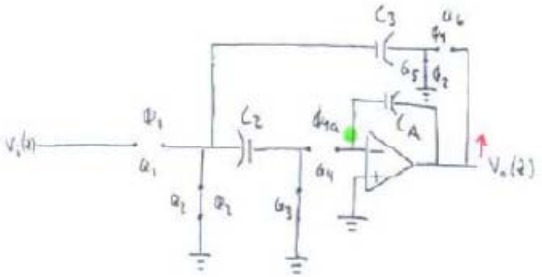
5/3

Just throw the older version..









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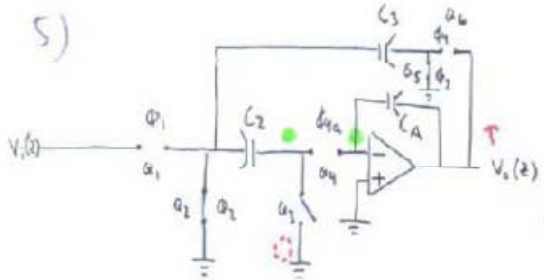

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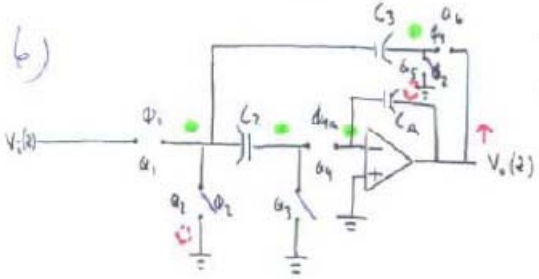

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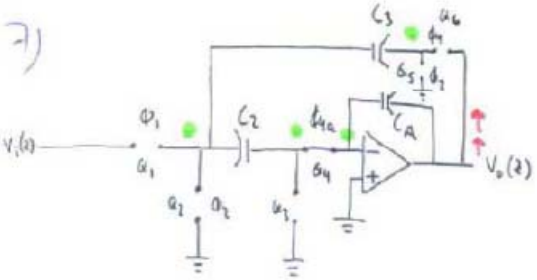

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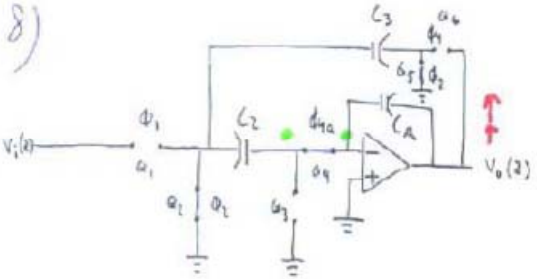
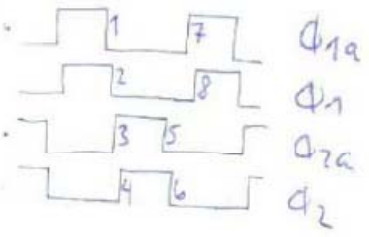


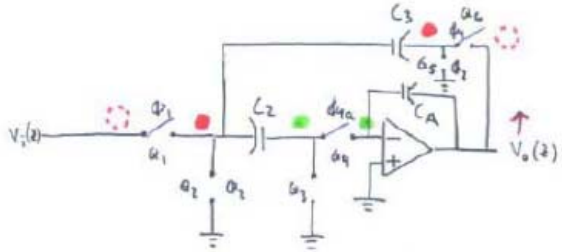


● not signal dependent charge

● signal depend.

◌ signal dep. but quickly absorbed by input or outp. (or uss)

1)



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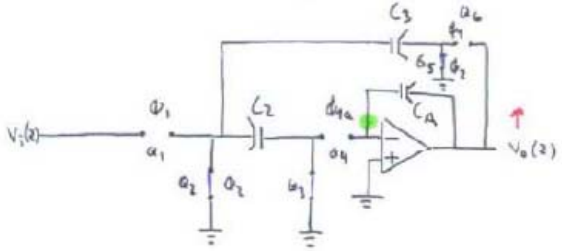

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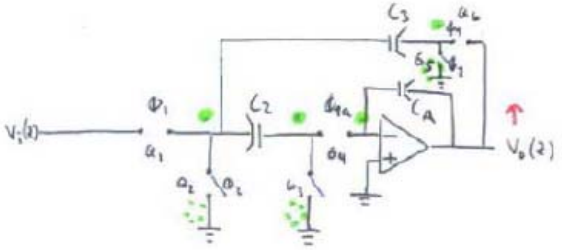

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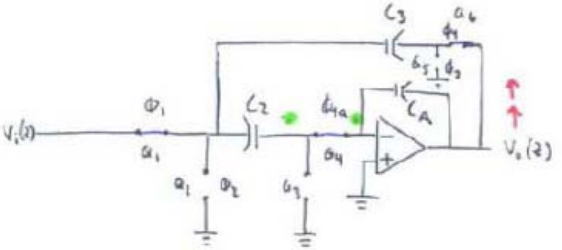

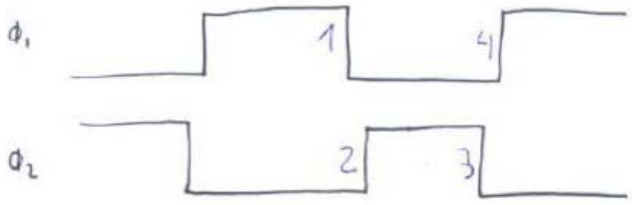

- Signal dependent charge inj.
- ——— " ——— but quickly absorbed by node
- Signal independent charge inj.
- Signal indep. charge quickly absorbed

Short explanation

- It’s assumed that the clock signals are so steep that half the charge injected by a switch is dumped on each side of the switch itself. The charge injected by Q1 (Fig. 10.26 pp 424 in ”J & M”) For the simplest clocking scheme (with clock events 1),2),3) and 4)), Q1, Q4 and Q6 open when Phi1 goes low. The input signal dependent charge injection due to Q1 produce a current that may go via C2, Q4 and CA. This produces a corresponding input signal dependent offset voltage at the output.
- This is enough to produce a input signal dependent voltage on the output (though Q6 may also contribute). No similar case exists for the clocking scheme with advanced clocks. CA is for example isolated from signal dependent charge injection in the 2nd among the 8 ”clock events” in the 1st slide.