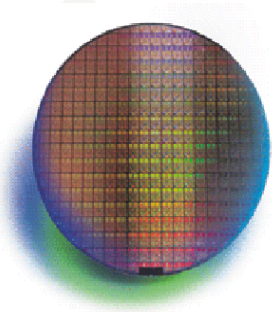
INF4420 – V2010:

- sa@luke ~ $ ng sinf4420
- fridtjha
- rise
- majacs
- hansoei
- haraldsf
- ragulant
- eivinsam
- natalkov
- nikolahl
- kritr
- sindrso
- mshaugla
- geiraby
- anderhf
- toreivib
- mortenhr
- moradi
- anhtv
- michaol
- kklee

- Lærere:
- Amir Hasanbegovic
- Snorre Aunet

Outline – Tuesday 20th of January

- Practical issues
- Learning goals
- Design project, tools and methods
- Syllabus
- Very brief introduction to various circuit building blocks (sample-and-holds, bandgap references, switched capacitor circuits, Nyquist- and oversampling data converters, phase-locked loops)



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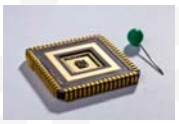
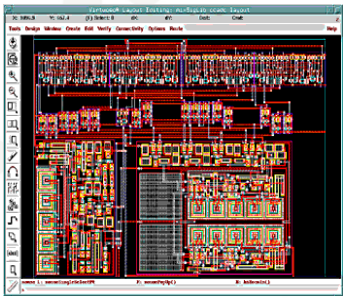
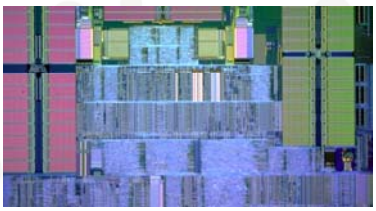
CMOS Integrated Circuits?

- Digital circuits exploit mainly transistors and interconnect
- Mixed-Signal (Digital AND Analog) also use resistors, capacitors and inductors
- Work-horse of modern Information Technology







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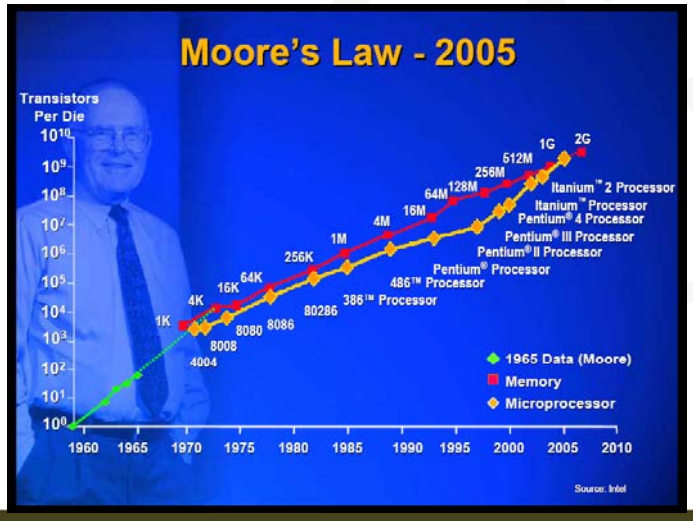
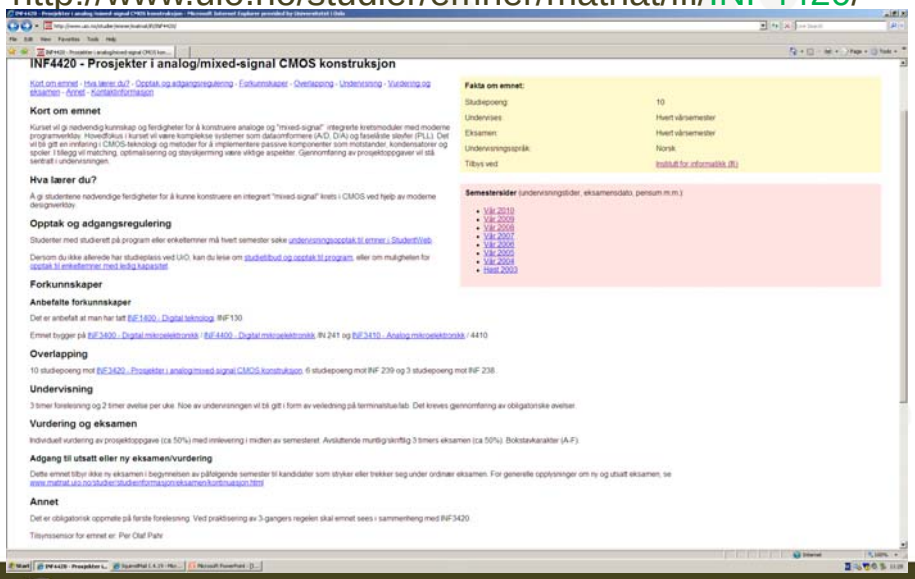
Moore's law: exponential increase in components per area



http://www.uio.no/studier/emner/matnat/ifi/INF4420/



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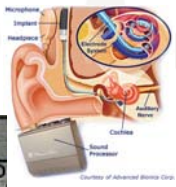
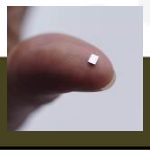
Why ASICs (Application Specific Integrated Circuits) ??

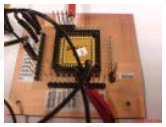
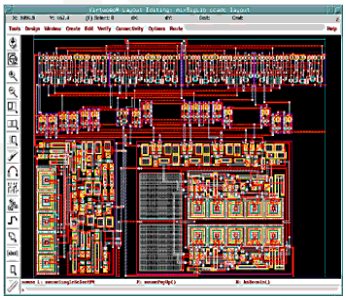
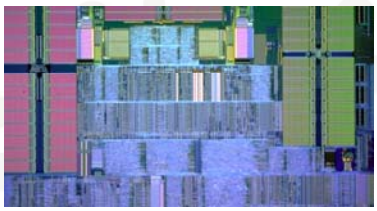
- Advantages:
  - Reduced size
  - Improved performance and functionality
  - Easier to hide ”company secrets”
  - Reduced cost
  - Reduced power consumption
  - Less radiated noise
- Disadvantages:
  - Increased start-up cost
  - High power density - Heat
  - Hard to find top competence
  - Time consuming development and production
  - Time-to-market

What is an integrated circuit?

- Transistors
  - Several options
- Capacitors
  - How to implement
  - Linearity
- Resistors
  - How to implement
  - Area
- Inductors
  - How to implement
  - Quality factor
- Parasitic components
  - Calculate
  - Minimize

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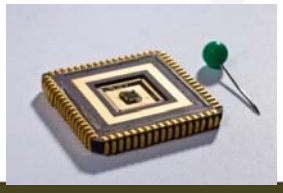
Design methods; digital from HDL, full custom analog

- Digital systems:
  - Automatic synthesis
    - VHDL
    - Schematic
- Analog systems:
  - Module based
  - Full-custom



Low Power..

KISEL ELLER MJUKVARA

Och till slut – är pendeln på väg att svänga från mjukvara till hårdvara? Idag handlar allt om energiförbrukning och i valet mellan programmerbara system och "hårda" ASIC-lösningar är det ingen större tvekan om vad som är energieffektivast. Och det blir samtidigt allt lättare att konstruera med hjälp av färdiga IP-block.

Om det här hade jag ett långt och intressant samtal med Kathryn Kranen, vd för EDA-företaget Jasper. Kathryn Kranen hävdar med bestämdhet att hon ser allt fler halvledarkonstruktioner, inte färre. Till och med företag som inte tidigare gjort egna kretsar tar nu steget till kisel för att klara sina krav.

Det här är något som vi snart kommer att återkomma till. Ännu så länge saknas hårda data, men de exploderande mjukvarukostnaderna gör att hårdvara inte nödvändigtvis är dyrare än mjukvara. Hårdvarukonstruktörernas disciplin och effektiva verifiering kanske gör att det till slut lönar sig med hårdvara.

Men det återstår att se.

Göte Fagerfjäll

Mandatory design project

- Design and implement mixed-mode circuit:
  - Example: ADC, SC-filter, PLL, DAC (2008)
  - System for automatic removal of mismatch (2009)
  - Milestones during the process
  - Teaching assistant, Amir Hasanbegovic, will follow up
- Write a project report
  - LaTeX or similar
- Submission: Early/Mid May
- Counts 40 % in the final grading (exam 60%)

Challenge in 2008: Digital-to-Analog Converter (”DAC”)

INF 4420 - Prosjektoppgave: Digital til Analog Omformer - 2008

1 Introduksjon

Det skal lages en data konverter av typen "Two stage balanced current DAC", illustrert i figur lengre ned.

- DAC'en skal ha en oppløsning tilsvarende minimum 6 bit.
- Anta i utgangspunktet at maksimalt et en spenningsreferanse og en strømkilde er tilgjengelig, og dermed ikke trenger konstrueres.
- Digitalt ord inn (unipolart) skal være på følgende form, forutsatt 6 bit oppløsning: 00...0, 00...1, ..., 11...1.
- Utgangssignalet skal være nedad begrenset til 0.3 V og oppad begrenset til 0.7 V.
- Positiv forsyninsspenning ("Vdd") er 1.0 V. Negativ forsyningsspenning ("Vss") er 0 V.
- Maksimal DNL: +/- 1 LSB
- Kretsen slik den er i kretsskjema mangler buffer, for eksempel i form av en spenningsfølger, som gjør den i stand til å drive en kapasitiv last i form av I/O-celle ("pad"). Det er frivillig evt å lage et slikt buffer, ikke påkrevd.
- Søk en best mulig konstruksjon ut fra effektforbruk og areal.

2 Milepæler

For å sikre gjennomføring innenfor tidsrammen settes det delmål med oppgitte frister. Studentene har ansvaret for å få disse delmålene godkjent av gruppelærer.

11/3-08 Det skal leveres inn et dokument på inntil 2 sider som beskriver hvordan dere har forstått oppgaven, og skisserer hvordan dere har tenkt å løse den.

25/3-08 Testbenk for systemet skal være ferdig.

6/5 08 Design og simuleringsarbeidet for hele kretsen skal være ferdig for både skjema og utlegg, og LVS inkludert. Gruppelærer skal eventuelt godkjenne at kretsen fungerer tilfredsstillende på bakgrunn av demonstrasjon.

3 Krav til prosjektgjennomføring

Målsetningen er å lage en digital-til-analog omformer ("DAC") med minimum 6 bit nøyaktighet. Gruppens medlemmer må i fellesskap gå gjennom oppgaven og fordele arbeidsoppgaver, men samtlige skal kunne stå inne for, og redegjøre for konstruksjonen. Arbeidsfordelingen mellom deltakere i prosjektet skal rapporteres. Under følger noen tilleggsopplysninger og nærmere spesifisering.

3.1 Praktisk arbeid

1. Komplette skjema, ned til transistornivå, skal tegnes. Det skal lages symboler for de ulike byggeblokkene som inngår i det komplette systemet som utgjør dataomformeren.
2. Benytt statistiske ("Monte-Carlo") simuleringer for å verifisere funksjonalitet under prosessvariasjoner.
3. Når simuleringsresultatene er tilfredsstillende skal det tegnes fysisk utlegg ("layout") for hver av byggeblokkene, som til slutt settes sammen til den komplette kretsen.
4. Det er en del spesielle utfordringer i forbindelse med design av systemer som inneholder mixed-signal (analoge og digitale) byggeblokker. Identifiser slike utfordringer og foreta tiltak for å løse disse.
5. Benytt Layout Versus Schematic ("LVS") for delkretser og totalsystem, for å verifisere samsvar mellom kretsskjema og tilsvarende utlegg, og lette konstruksjonen. Resultatene fra LVS skal vedlegges prosjektrapporten.

4. Krav til rapport.

Sentralt i bedømmingen av arbeidet vektlegges rapportens kvalitet. Skriv den i LaTeX eller tilsvarende program. De ulike fasene av prosjektet skal dokumenteres. Dette inkluderer bla plot av skjematikk samt simuleringsresultater som demonstrerer funksjonalitet hos de ulike byggeblokkene. LVS rapporter fra Cadence hører også hjemme her. Begrunn og dokumenter de ulike valgene dere har gjort. Dette inkluderer blant annet dimensjonering av aktive og passive komponenter, problematikk omkring matching, tiltak mot støy, samt layout.

Husk at bidrag fra de ulike gruppemedlemmene skal være identifiserbare.

Rapporten skal også inneholde informasjon om hvor Cadence-filer ligger tilgjengelige for etterkontroll av resultater.

Sensor bedømmer rapporten. Derfor er det viktig at denne er mest mulig forståelig for sensor.

5. frister for innlevering.

Prosjektet skal være avsluttet og rapport innlevert senest 9/5-2008 kl. 12:00. Alle gruppene må presentere resultatene av prosjektet etter innlevering. Følg med på fagets hjemmeside for evt andre beskjeder. Vurdering baseres på en bedømming av arbeidets kvalitet, og rapportens kvalitet, slik dette framgår av sistnevnte. En prosentuell score vektes inn i endelig karakter for faget.

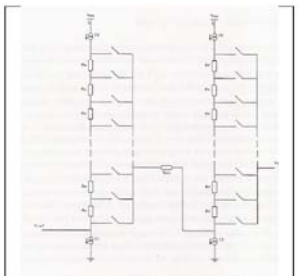


Fig 4.6 Diagram, two-stage balanced current DAC.

Fra "High-Speed Data Converters Fully Integrated in CMOS". Leif Hanssen, dr. scient. avhandling., ifi, UiO, 1990.

Lykke til!!

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INF4420 Project 2009 (1/2)

INF4420 project description

Some years from now, you have been hired by an undisclosed chip maker as their mixed signal designer, partly because of your achevements in the INF4420 course. The company is currently working hard towards finishing their new flagship product. The system designers in your group already have very promising high level simulation results of the product. From these simulations they have derived the specifications for each building block.

The OTAs are central components in this system, as a lot of the specifications for the final product relies on OTA performance. Your group's analog designer already have a working folded cascode OTA which almost meets the spec, except for the offset voltage. This is not easily correctable in the layout because the required transitor sizing would be impractical and incur other unacceptable side effects.

At the next meeting, you suggest doing a digital calibration loop[1] for the OTA's offset voltage. The OTA's designer advice you that the trimming can be done easily by drawing a compensation current from the input-stage differential pair.

For this product, timing is not tight so you should have plenty of time for running the calibration. However, if you can make it faster, it will be much easier to apply to future products, without having to go through an expensive redesign.

1 Measuring the OTA performance

The existing OTA is available from `/hom/jorgenam/cadence_stm90/INF4420`. Use the library manager to add this path (Edit → Library path...). Using an ideal 100 fF capacitor as load, connect the OTA in a closed loop unity gain feedback, and measure the following:

- Gain-bandwidth product (GBW)
- Phase margin (PM)

If you like, you can also measure

- Noise
- Slew rate (how does this compare to the theory?)
- Output swing
- Settling behaviour
- Or other relevant parameters

[1] The workings of the calibration loop will be described later.

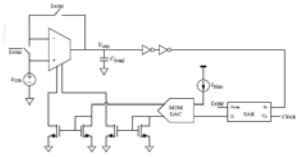

Figure 1: Digital trimming of the OTA's offset voltage (All NMOS are 0.5/0.5 µm)

Next, set up a testbench to find the variation in offset voltage. Use a montecarlo (MC) analysis with 100 runs.

- What is the standard deviation, σ, of the offset voltage?
- If we cover 6σ variation, how many percent of the manufactured OTAs will function to spec?
- What is the 6σ value?

Remembering that g_m is the transistor parameter that relates a change in gate voltage to a change in drain current, we can find the maximum required compensation current as $I_{bias} = 6\sigma \times g_m$. To find the g_m you can use an operating point analysis (remember to save operating point) and the results browser which you find under the tools-menu in ADE.

- What is the value of g_m of transistor M1 or M2 in the OTA?
- What is the value of I_{bias}?

2 Simulating the calibration loop

It's now time to simulate the entire calibration loop using the supplied components `OTA_trim`, `DAC_ideal`, and `SAR`. `OTA_trim` is the same as `OTA` but with an added current-mode trimming port. `DAC_ideal` is an ideal 7 bit D/A converter with radix 1.77 (sub-binary resolution).

If we run the OTA in open loop, an offset voltage will cause the output to rail (assuming sufficient gain). We can use this to detect if the offset voltage is too high or low. To properly buffer the output to a clean digital level, we can add inverters as buffers.

The DAC outputs a differential current approximately proportional to the input word (it does have some redundancy). This current is applied to the trimming port of

2

3. februar 2010 13

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INF4420 project 2009 (2/2)

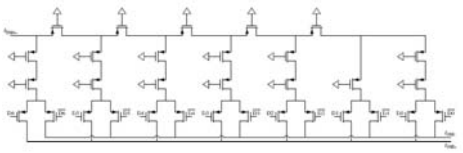

Figure 2: M3M DAC schematics (all PMOS are 0.5/0.2 µm)

the OTA through a current mirror. Thus, we now have a digital input for trimming the OTA's offset voltage. To find the suitable digital correction word, we will use a successive approximation register (SAR). The SAR tests each bit, starting at the MSB. If the OTA output swings above the common mode output voltage, the tested bit is cleared. After testing each bit, the SAR signals that it is done, and that normal system operation can resume. Thus, this signal can be used to switch the OTA between open loop and closed loop unity gain feedback.

- Simulate the system to verify its functionality
- What is the offset voltage after calibration?
- What is the σ of the offset voltage now?

Make a testbench and measure how the added trimming circuitry affect the performance of the OTA.

- Is the performance different compared to your previous measurements?
- What can be done to counter this?

3 DAC design

- Draw ideal transfer functions for a radix 2 converter and a radix 1.77 converter in the same plot.

Figure 3 depicts the schematics of a so called M3M DAC. The mosfets are all in the triode region.

- How does this structure compare to the more familiar R2R DAC?
- Make a testbench where you compare the transfer function of the ideal DAC with the M3M DAC.

3

Replace the ideal DAC in your calibration loop test bench with the M3M DAC.

- How does this affect the performance of the calibration loop?

Draw layout for the M3M DAC and the current mirror, remember to verify its correctness using DRC and LVS. Finally, do a parasitic extraction of the layout.

- Simulate the calibration loop with the extracted netlists.

4 Project requirements

The transistor sizing given in this document are reasonable guidelines to get you started. You are free to change this if neccessary.

Document everything, including but not limited to, all relevant schematics, layout, and simulation results. Discuss the choices you have made in designing and testing. Everything should be clear just from reading the documentation.

5 Deliverables

1. Do the first part of the project, described in Sect 1. Deadline March 19.
2. Do the second part of the project, described in Sect 2. Deadline April 2.
3. Finalize the project by completing the third and final part of the project, described in Sect 3, and write your final report. Deadline May 11.

In the first two deliverables, write a short report observing the guidelines in Sect 4. The final report must be comprehensive and document the entire project (i.e. include all deliverables). Only this final report will contribute towards your final grade. Please make all schematics and layout available for inspection.

JAM, February 12, 2009

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Cadence (http://www.cadence.com/)

- Widely used IC design tool worldwide, both in companies and academia
- Very large system
  - PCB-design
  - IC-design
    - Synthesis
    - Schematic entry
    - Simulator (Analog Environment / Spectre)
    - Layout (Virtouso)
- DRC and LVS performed by Calibre (Mentor)

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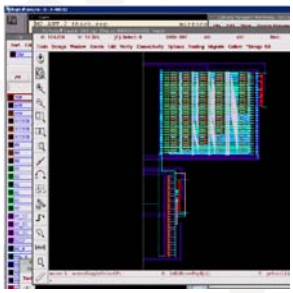
Full-custom (”handmade”) design flow

- Design and calculation
  - Design equations
  - Dimensioning for matching
- Schematic entry
  - Simulations on cells and top level
  - Several interactions
- Layout
  - Module interface
  - Symmetry/hierarchy
  - Post Layout Simulations on critical modules
- Next module….



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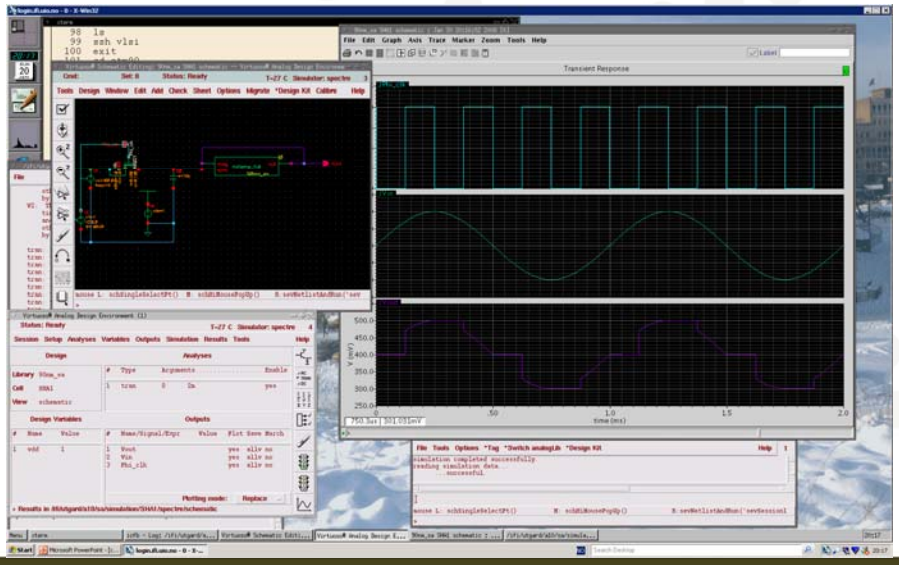
Cadence forts.

- Start-up:
  - Web manual
- Standard libraries:
  - tsmcN90rf
  - analogLib
- Design views:
  - Symbol
  - Schematic
  - Layout

Schematic entry and simulations in Cadence



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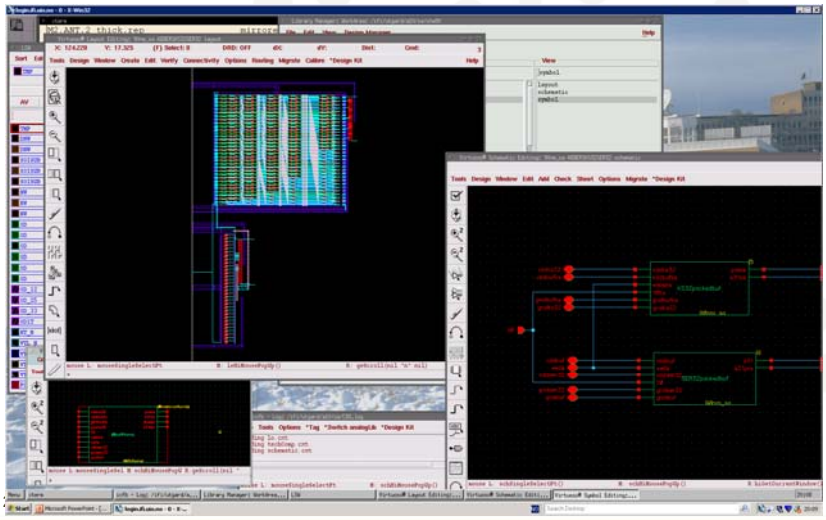
Symbol, schematic and layout (Cadence)



Process

- TSMC 90 nm low power CMOS:
  - Minimum gate length: 90nm
  - 1 Poly-layer
  - 9 Metal-layers
  - True triple well
  - Three different threshold voltages
  - Supply voltage: 1.2 V typ.
  - Very advanced process

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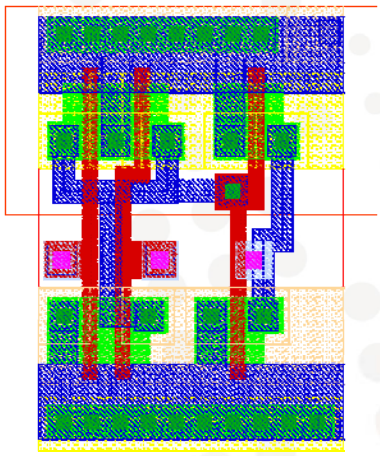
AND-gate



Challenges regarding the project

- Project administration
- Theoretical analysis and circuit design
- Design errors
  - LVS
- Parasitic components
  - Extraction and Post Layout Simulation (PLS)
- Process variations
  - Simulations (Corner + Monte-Carlo)
- Noise
  - Component and crosstalk
- Good layout practice / Symmetry

Practical information

- Lectures:
  - Tuesdays . 9.15 – 11.00 (should not collide with FYS3240).
  - From. 26/2: Tuesday . 9.15 – 12.00 (Might be 9:15 – 11:00 in most cases)
- Syllabus:
  - Johns and Martin: Analog Integrated Circuit design (Kap. 2, 8-14, 16. Not bipolar)
  - Selected additional material and lecture notes
  - LTH: Cadence 4.4
  - IFI: Lokal guide til Cadence
- Exercises
  - 2 hours per week – Time will be set next week. Amir Hasanbegovic, amirh@ifi.uio.no
- Projectsupervision/design lab
  - 2/4 hours each week – Time may be adjusted. Amir H., amirh@ifi.uio.no .
  - Room 3217 (?)
- Software:
  - Cadence 5.00 or 6.00 ((?))
  - TSMC 90 nm design kit
- Where to run the software:
  - Win PC running X-Win connected to Linux server /remote desktop and Linux
  - Linux computer
- Student reference group
  - 1-2 students

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What do we expect from you?

- The course is demanding
- Theoretical background
  - INF3410 analog microelectronics, or similar
  - FYS3220 linear circuit theory, or similar
  - INF3440 signal processing, or similar
- Prepare for the lectures
- Exercises
- Use the reference group and course evaluations to provide feedback

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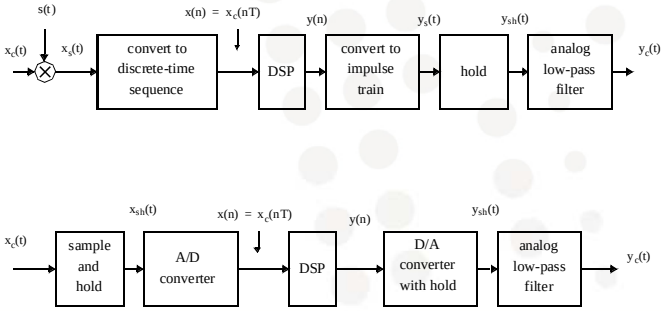
Final exam – a few words

- Thursday 3rd of June, starting 14:30 (3 hours)
- Problems usually related to every single of the relevant chapters in the book (2,8,9,…,14,16), and material from the lectures



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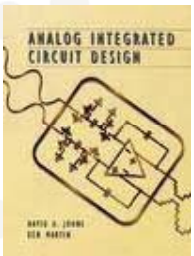
Syllabus; chapters 2,8,9,10,11,12,13,14,16



- Chapter 2 Processing and layout
- Chapter 8 Sample and Holds, Voltage references, and translinear circuits
- Chapter 9 Discrete-Time Signals
- Chapter 10 Switched-capacitor circuits
- Chapter 11 Data converter fundamentals
- Chapter 12 Nyquist-rate D/A converters
- Chapter 13 Nyquist-rate A/D converters
- Chapter 14 Oversampling converters
- Chapter 16 Phase-locked loops

(in lectures, tuesdays)

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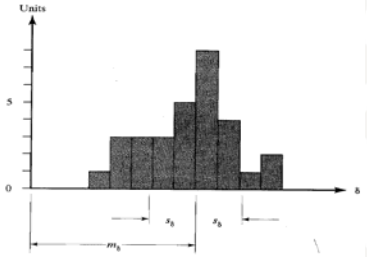
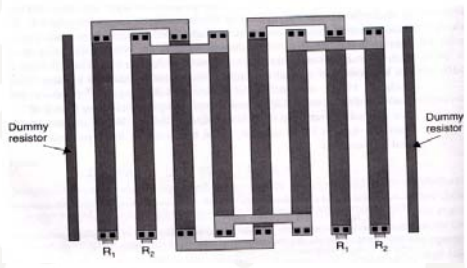
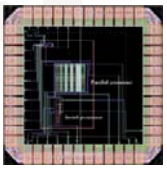
Syllabus; chapter 2





- CMOS processing
- Relative matching far better than absolute accuracy in CMOS
- CMOS layout and design rules
- "*Matching is the Achilles heel of analog*" C. Diorio, Impinj / Washington State University
- A bad layout can ruin about any analog circuit.

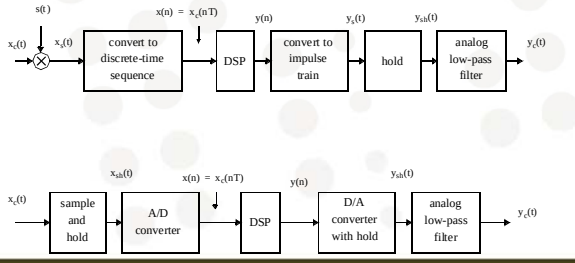
Chapter 8 Sample and Holds, Voltage References



- Performance of S/H
- S/H basics
- Bandgap voltage reference basics
- Circuits for bandgap references

Chapter 9 Discrete-Time Signals

- Signal spectra
- Laplace transform of discrete-time signals
- Z-transform
- Downsampling and upsampling
- Discrete-time filters
- S/H response



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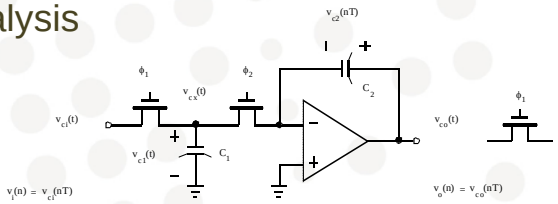
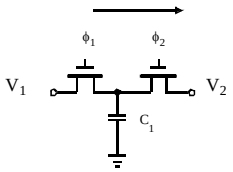
Chapter 10 Switched-Capacitor Circuits

- Building blocks
- Operation and analysis
- First-order filters
- Biquad filters





$\Delta Q = C_1(V_1 - V_2)$ every clock period

$R_{eq} = \frac{T}{C_1}$

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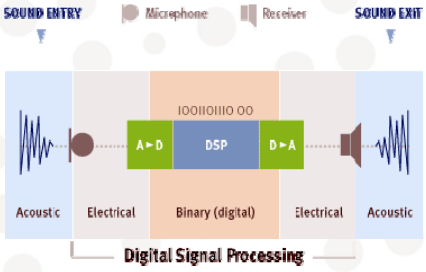
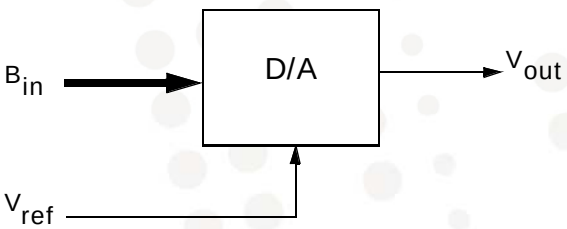
Chapter 11 Data converter fundamentals

- Ideal D/A and A/D
- Quantization noise
- Signed codes
- Performance limitations



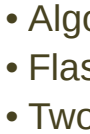
Chapter 12 Nyquist-Rate D/A Converters

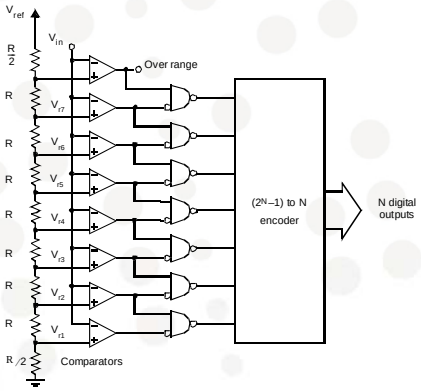
- Decoder-based converters
- Binary-scaled converters
- Thermometer-code converters
- Hybrid conv.



Chapter 13 Nyquist-Rate A/D Converters

- Integrating converters
- Successive approx. converters
- Algorithmic converters
- Flash (parallell) conv.
- Two-step, interpolating,
- Folding, pipelined conv.



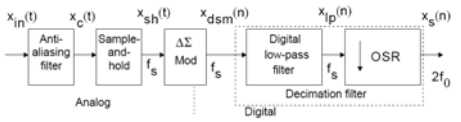


Two consequences of the Nyquist-theorem and anti-aliasing filters (Wikipedia):

- If the highest frequency *B* in the original signal is known, the theorem gives the lower bound on the sampling frequency for which perfect reconstruction can be assured. This lower bound to the sampling frequency, 2*B*, is called the Nyquist rate.
- If instead the sampling frequency is known, the theorem gives us an upper bound for frequency components, $B<fs/2$, of the signal to allow for perfect reconstruction. This upper bound is the Nyquist frequency, denoted *fN*.
- An **anti-aliasing filter** is a filter used before a signal sampler, to restrict the bandwidth of a signal to approximately satisfy the sampling theorem. Since the theorem states that unambiguous interpretation of the signal from its samples is possible only when the power of frequencies outside the Nyquist bandwidth is zero, the anti-aliasing filter would have to have perfect stop-band rejection to completely satisfy the theorem. Every realizable anti-aliasing filter will permit some aliasing to occur; the amount of aliasing that does occur depends on how good the filter is.

Chapter 14 Oversampling Converters

- Oversampling (>> 2 Nyquist bandwidth) relaxes requirements for matching
- High resolution, low to medium speed
- Noise shaping & oversampling
- N+1 order modulator gives a certain SNR for lower OSR
  than N-order mod.
- 24 bit Audio conv.



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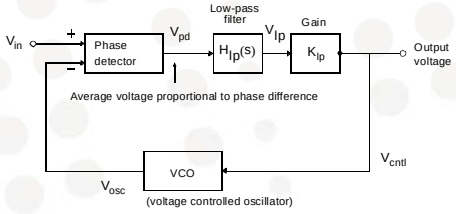
Chapter 16 Phase-locked loops

- Application examples:
- clock multiplication,
- Freq. generation: The PLL output is a signal with frequency N times the input frequency where N may be a fractional number
- FM demodulation (The input is a FM signal (IF) The output is the demodulated baseband signal
- Products: TV and wireless



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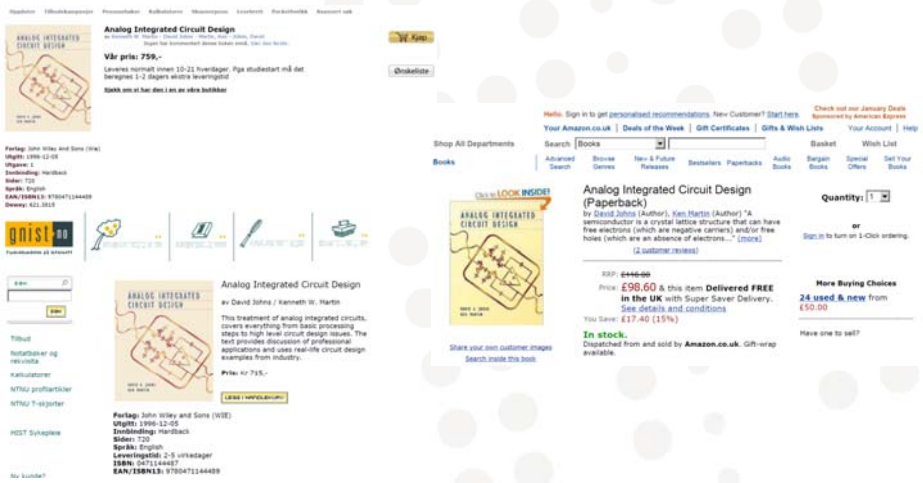
www.akademika.no / www.gnist.no / www.amazon.co.uk



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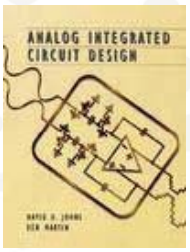
Next week:

- Sample and Hold circuits (chapter 8)
- Questions: sa@ifi.uio.no



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