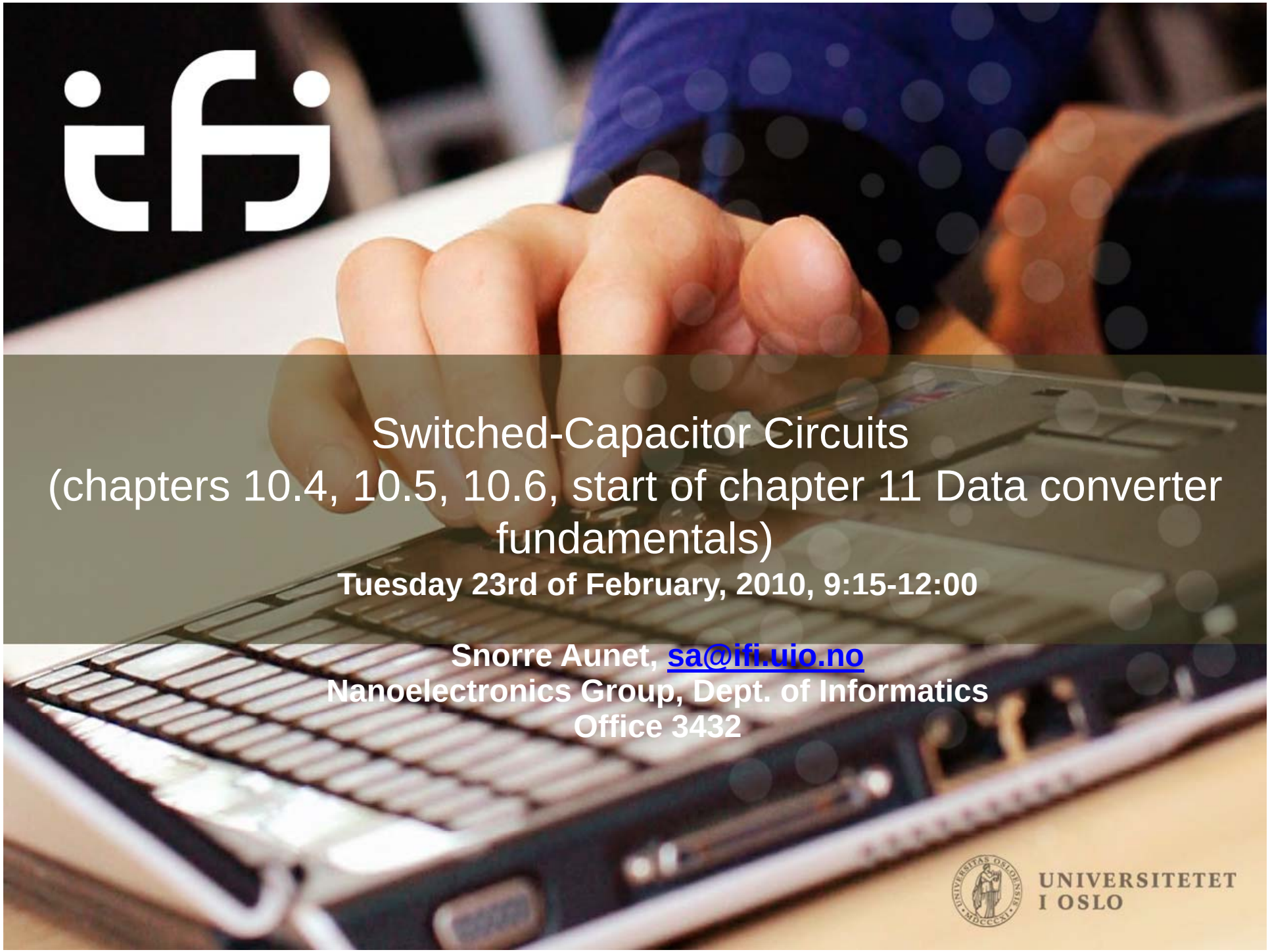

Switched-Capacitor Circuits
(chapters 10.4, 10.5, 10.6, start of chapter 11 Data converter fundamentals)

Tuesday 23rd of February, 2010, 9:15-12:00

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UNIVERSITETET I OSLO

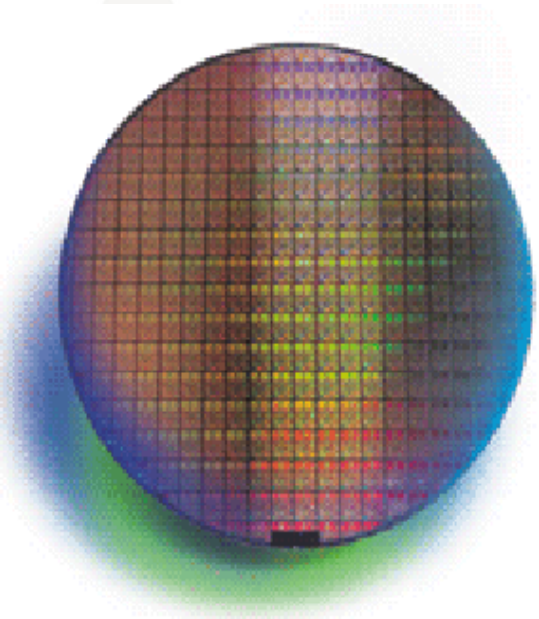
Last time – and today, Tuesday 23rd of February:

9.2 Laplace Transform of Discrete Time Signals
9.3 z-transform
9.4 downsampling and Upsampling
9.5 Discrete Time Filters
9.6 Sample-and-Hold Response

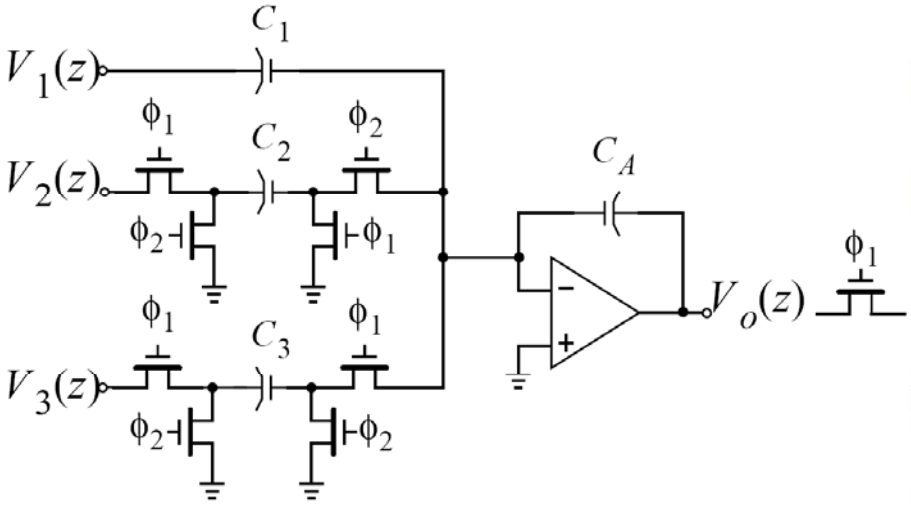
10.1 Switched Capacitor Circuits
10.2 Basic Operation and Analysis

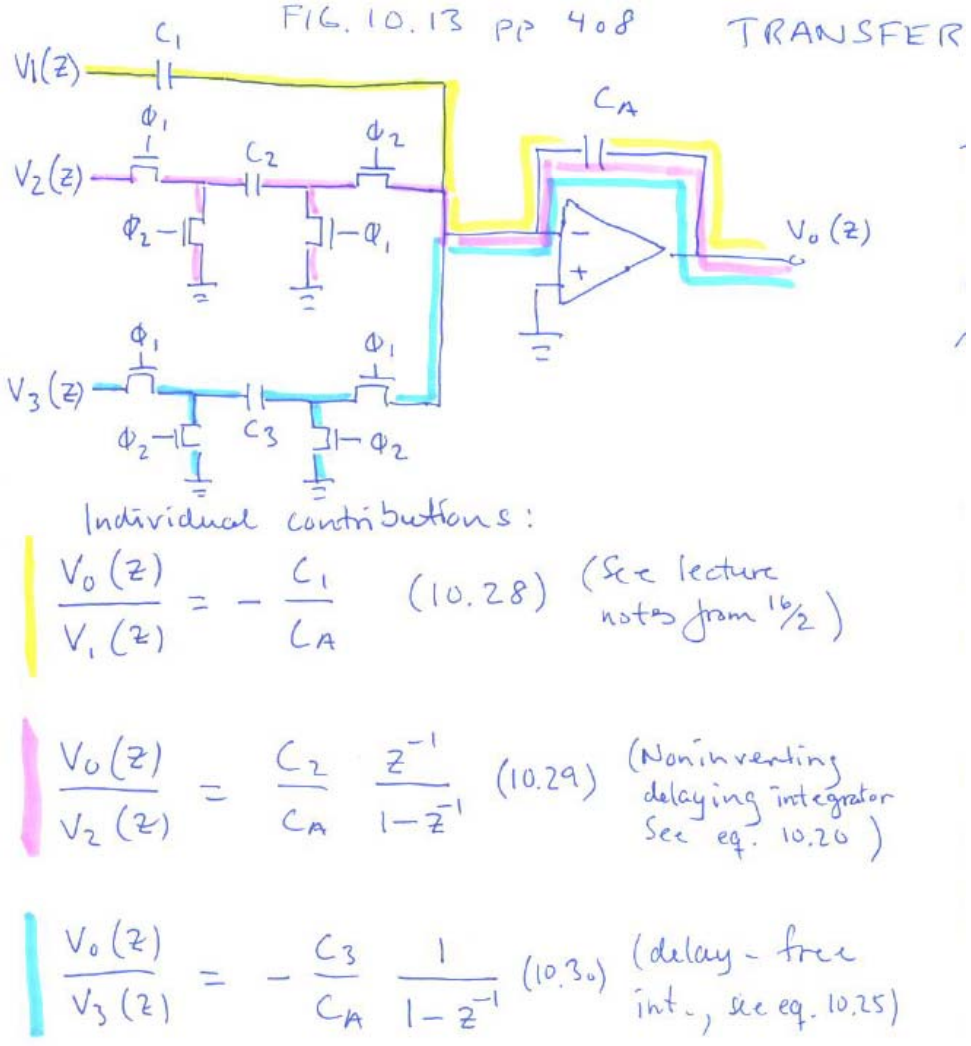
Today:

10.3 First-order filters
10.4 Biquad filters (high-Q)
10.5 Charge injection
10.7 Correlated double sampling techn
11.1 Ideal D/A converter
11.2 Ideal A/D converter
11.3 quantization noise
11.4 signed codes



Signal-flow-graph analysis (p. 407)





- Applying charge equations is tedious for larger circuits. Using some rules and signal-flow-graph analysis simplifies analysis and design of SC-circuits.
- Superposition (Wikipedia)In a linear system, *the net response at a given place and time caused by two or more independent stimuli is the sum of the responses which would have been caused by each stimulus individually*.

Getting the transfer function..

Multiplying each of the equations (10.28), (10.29), (10.30) by their respective input voltages, on each side:

$$V_o(z) = -\frac{C_1}{C_A} \cdot V_1(z)$$

$$V_o(z) = \frac{C_2}{C_A} \frac{z^{-1}}{1-z^{-1}} \cdot V_2(z)$$

$$V_o(z) = -\frac{C_3}{C_A} \frac{1}{(1-z^{-1})} \cdot V_3(z)$$

Adding the contributions:

$$V_{out}(z) = -\frac{C_1}{C_A} \cdot V_1(z) + \frac{C_2}{C_A} \frac{z^{-1}}{1-z^{-1}} V_2(z) + -\frac{C_3}{C_A} \frac{1}{(1-z^{-1})} \cdot V_3(z)$$

As powers of z:

$$V_{out}(z) = -\frac{C_1}{C_A} \cdot V_1(z) + \frac{C_2}{C_A} \frac{1}{z-1} V_2(z) - \frac{C_3}{C_A} \frac{z}{z-1} V_3(z) \qquad (10.31)$$

Signal Flow Graph (Fig. 10.13 in "J & M")

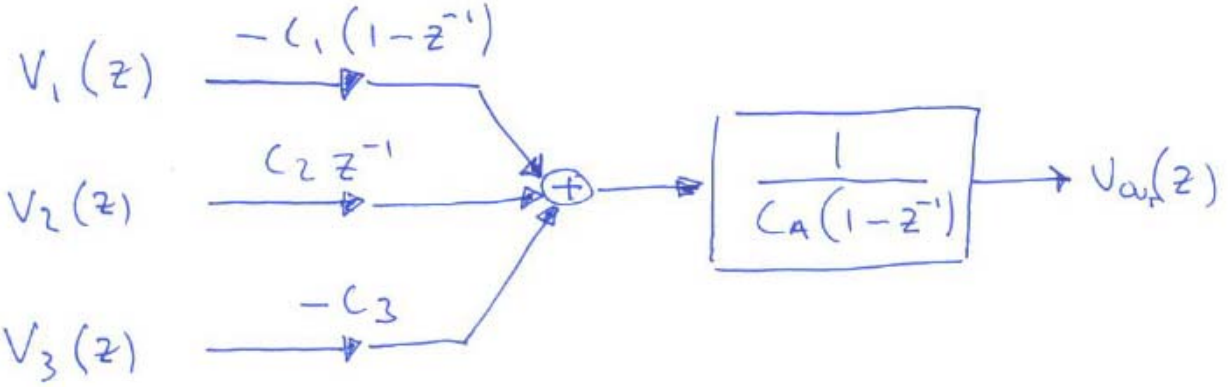
SIGNAL FLOW GRAPH IN FIG 10.13

(10.30)

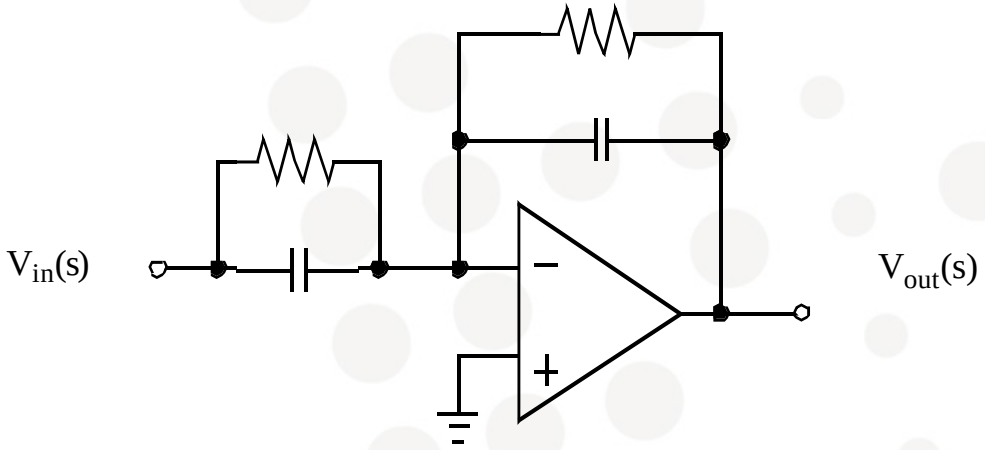
$$V_{out}(z) = -\frac{C_1}{C_A} \cdot V_1(z) + \frac{C_2}{C_A} \frac{z^{-1}}{1-z^{-1}} V_2(z) - \frac{C_3}{C_A} \frac{1}{1-z^{-1}} V_3(z)$$

$$= -\frac{C_1}{C_A} \frac{(1-z^{-1})}{(1-z^{-1})} \cdot V_1(z) + \frac{C_2}{C_A} \frac{z^{-1}}{1-z^{-1}} V_2(z) - \frac{C_3}{C_A} \frac{1}{1-z^{-1}} V_3(z)$$

See that $\frac{1}{C_A(1-z^{-1})}$ is a common factor



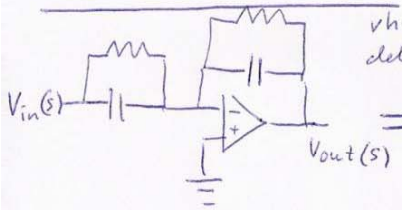
First-Order Filters



- Select a known Active-RC circuit
- Replace resistors by SC-equivalents
- Analyze using discrete-time methods

Making 1st order SC-filter from active RC equivalent

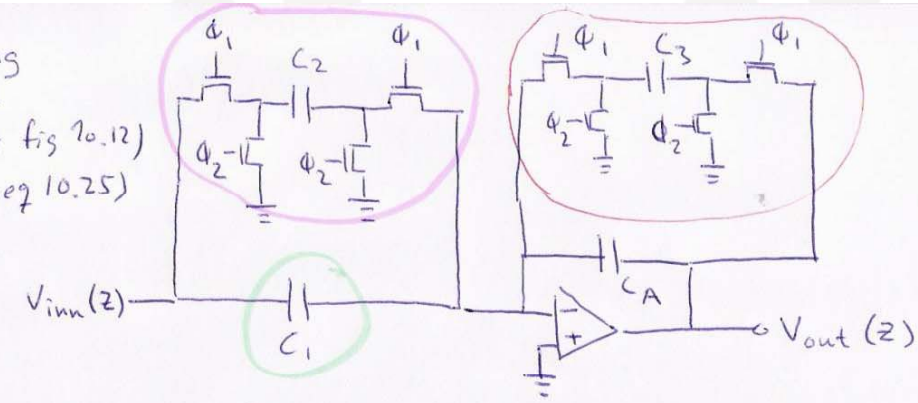
1st order filters



vha inverting delay-free SC

(See fig 10.12)

(See eq 10.25)



Superposition

$$V_{out}(z) = -\frac{C_2}{C_A}\frac{z^{-1}}{1-z^{-1}} \cdot V_{in}(z) - \frac{C_3}{C_A}\frac{1}{1-z^{-1}} \cdot V_{out}(z) - \frac{C_1}{C_A} V_{in}(z)$$

$$V_{out}(z) \cdot C_A (1-z^{-1}) = -C_2 \cdot V_{in}(z) - C_3 \cdot V_{out}(z) - C_1 (1-z^{-1}) \cdot V_{in}(z)$$

$$\Updownarrow$$

$$V_{out}(z) \cdot C_A (1-z^{-1}) + C_3 V_{out}(z) = -C_2 \cdot V_{in}(z) - C_1 (1-z^{-1}) V_{in}(z)$$

$$\Updownarrow$$

$$V_{out}(z)\left[C_A (1-z^{-1}) + C_3\right] = -V_{in}(z)\left[C_2 + C_1 (1-z^{-1})\right]$$

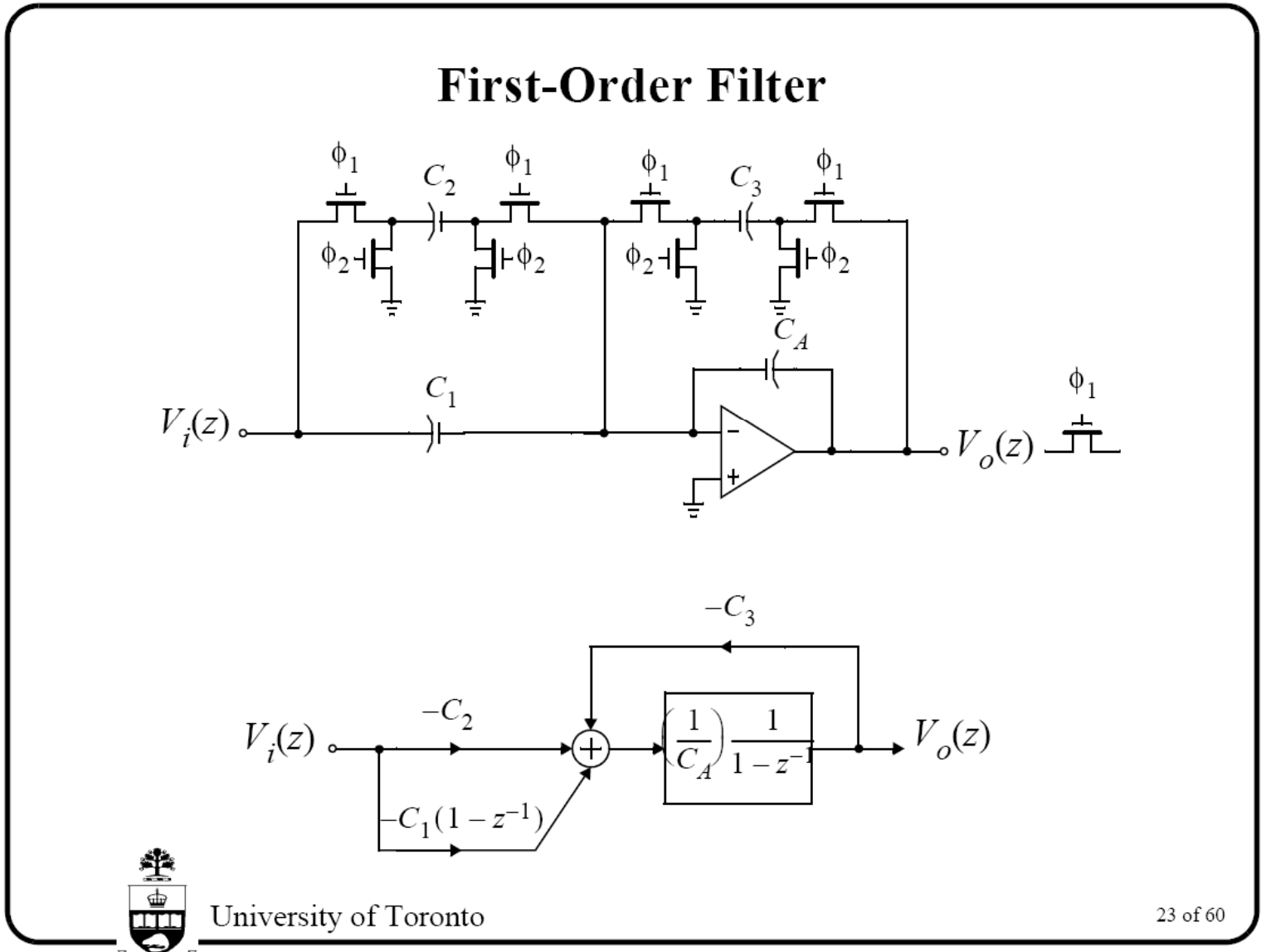
$$\Updownarrow$$

$$H(z) = \frac{V_{out}(z)}{V_{in}(z)} = -\frac{\left[C_2 + C_1 (1-z^{-1})\right]}{\left[C_A (1-z^{-1}) + C_3\right]} = \frac{\frac{C_2}{C_A} + \frac{C_1}{C_A}(1-z^{-1})}{1 - z^{-1} + \frac{C_3}{C_A}} = \frac{\frac{C_2}{C_A} z + \frac{C_1}{C_A}(z-1)}{z - 1 + \frac{C_3}{C_A} \cdot z} = \frac{\frac{C_2}{C_A} z + \frac{C_1}{C_A} z - \frac{C_1}{C_A}}{z + \frac{C_3}{C_A} z - 1}$$

eq 10.33:

$$= \frac{\left(\frac{C_1 + C_2}{C_A}\right) z - \frac{C_1}{C_A}}{\left(1 + \frac{C_3}{C_A}\right) z - 1}$$

SFG based on superposition, similar as in fig 10.13.



POLES?

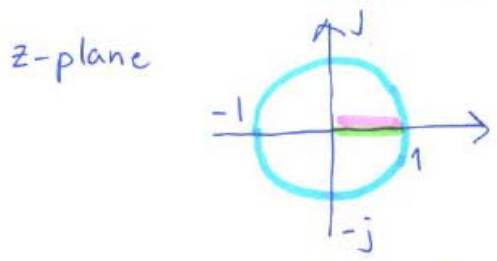
Equating the denominator to zero, in $H(z)$:

$$\left(1+\frac{C_3}{C_A}\right)z-1=0$$

$$\Updownarrow$$

$$z_p=\frac{C_A}{C_A+C_3}$$

For positive capacitance values this pole is restricted to the real axis between zero and one



In this case the circuit is always stable.

The case of $C_3=0$:

$$z_p=\frac{C_A}{C_A+C_3}=\frac{C_A}{C_A}=1$$

ZEROS?

Numerator in $H(z)=0$

$$\left(\frac{C_1+C_2}{C_A}\right)z-\frac{C_1}{C_A}=0$$

$$\left(\frac{C_1+C_2}{C_A}\right)z=\frac{C_1}{C_A}\Leftrightarrow z=\frac{C_1}{C_1+C_2}$$

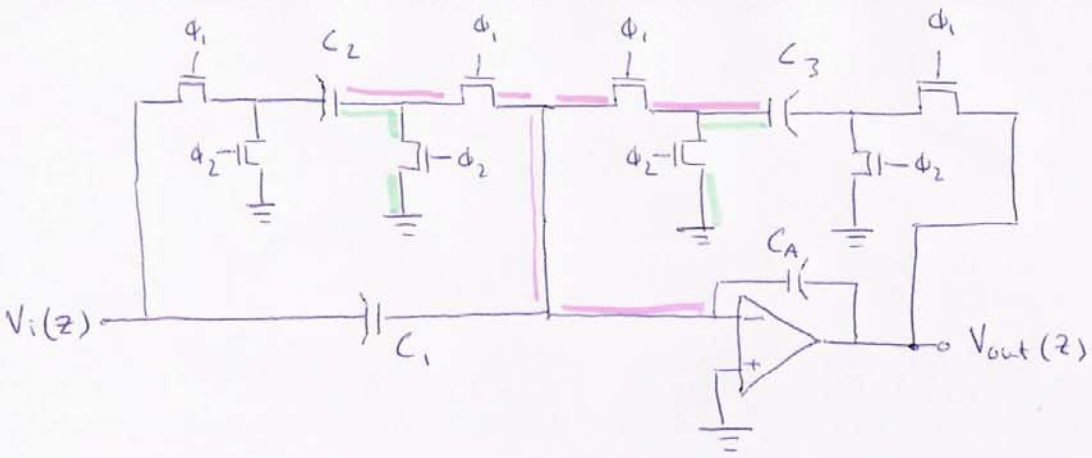
For positive capacitances the zero is located to the real axis between 0 and 1.

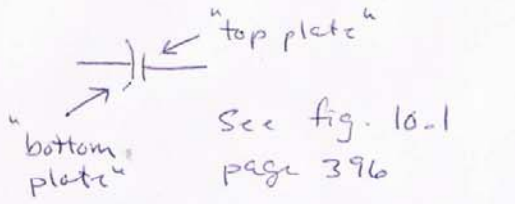
DC-gain ($z=1$):

$$H(1)=-\frac{\left(\frac{C_1+C_2}{C_A}\right)z-\frac{C_1}{C_2}}{\left(1+\frac{C_3}{C_A}\right)z-1}=-\frac{\frac{C_1}{C_A}+\frac{C_2}{C_A}-\frac{C_1}{C_A}}{1+\frac{C_3}{C_A}-1}$$

$$=-\frac{\frac{C_2}{C_A}}{\frac{C_3}{C_A}}=-\frac{C_2}{C_3}.$$

Switch sharing (p. 413)





Switch sharing, page 413 in "J&M"

in Φ_1 : C_2 top plate switched to (virtual) ground

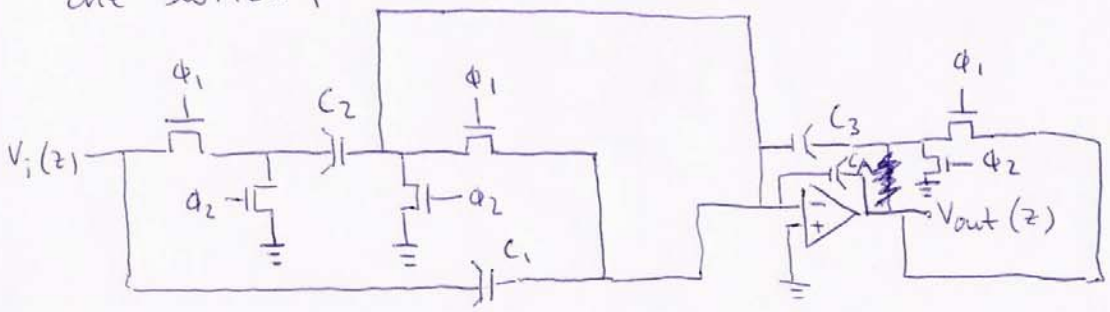
C_3 ——— || ———

in Φ_2 : C_2 ——— || ——— ground

C_3 ——— || ———

$\Rightarrow$ Top plates of C_2 and C_3 can be connected together and one pair of switches eliminated

Connecting the top plates and letting them share one "switch-pair":



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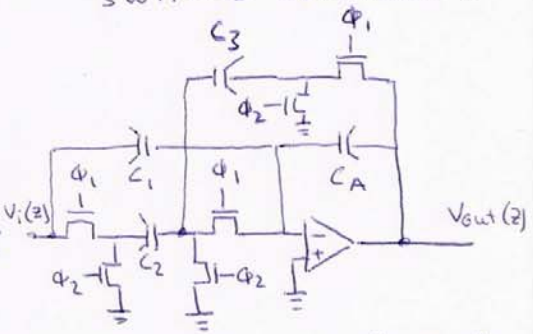
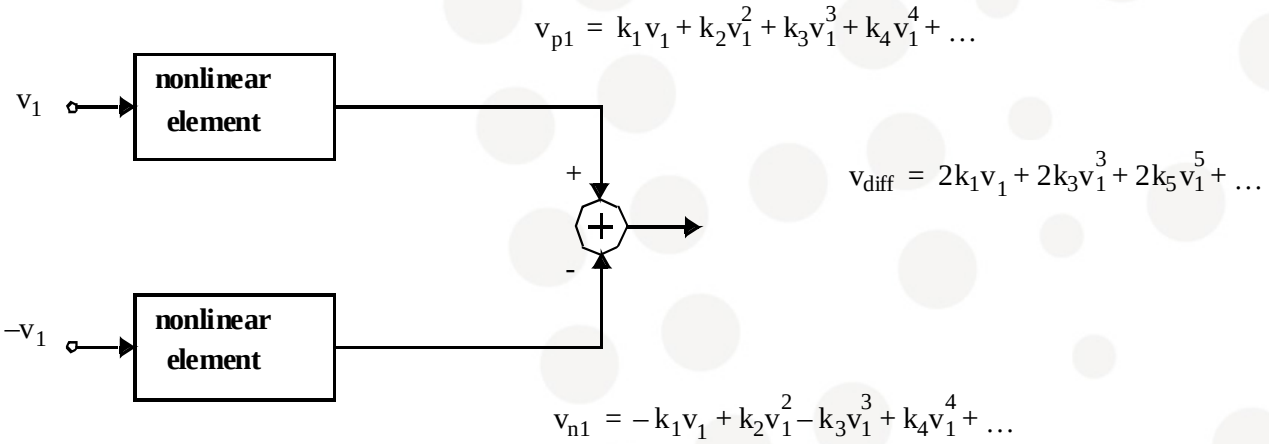


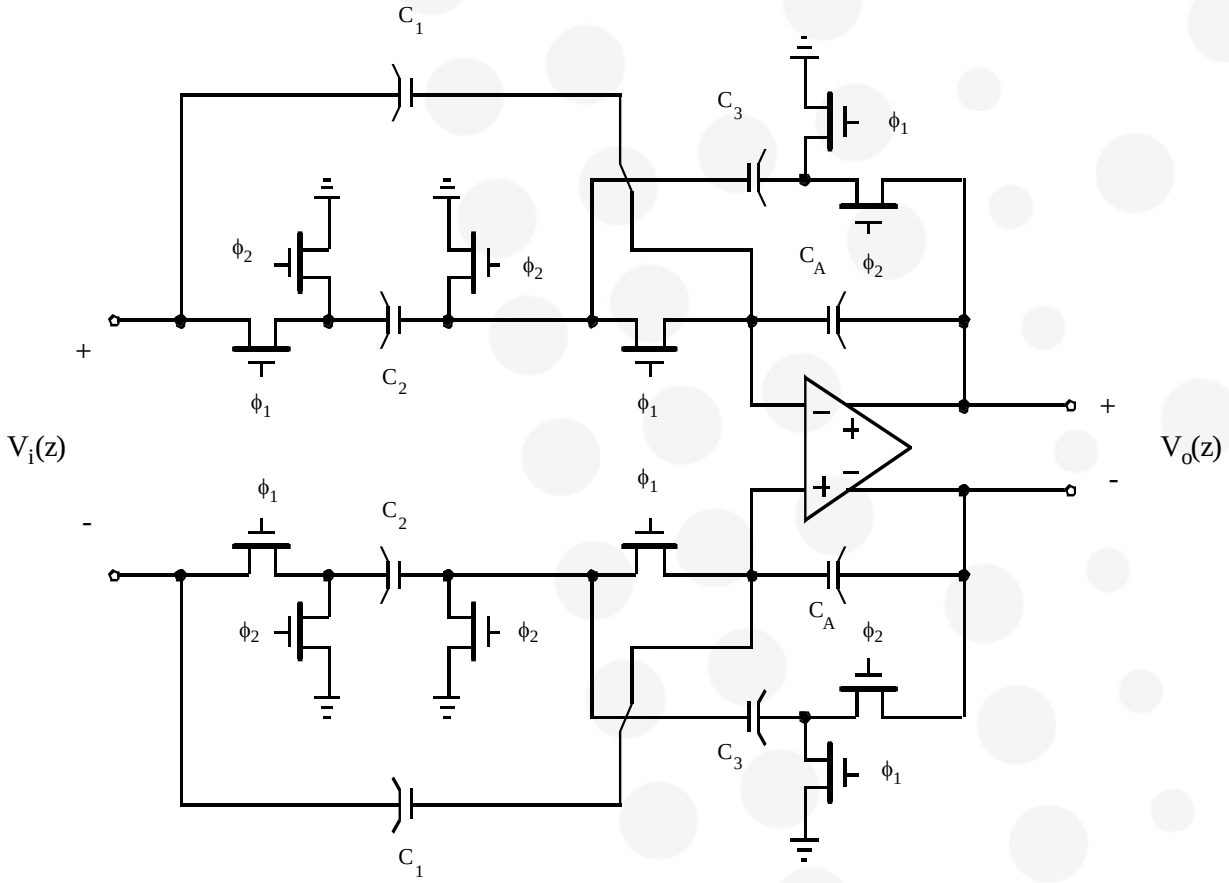
Fig. 10.16 i "J&M"

Fully Differential Filters (p. 414 (1/3))

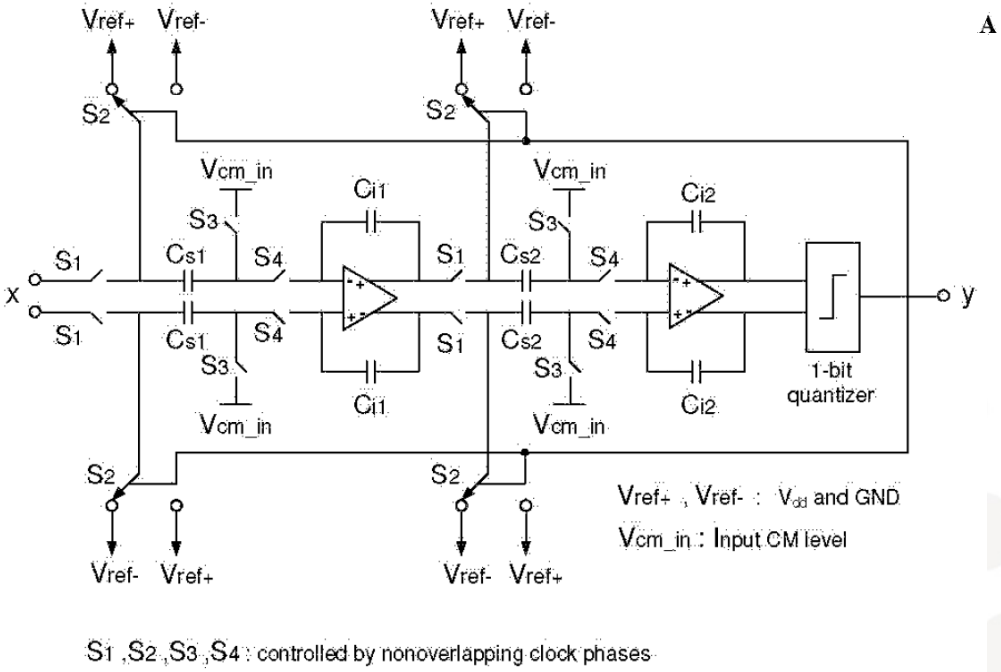


- The signal is represented by the difference of two voltages
- Most SC-designs are fully differential, typically operating around a dc common-mode voltage halfway between the supply voltages
- Reduced common-mode noise
- Cancellation of even-order harmonic distortion, if the nonlinearity is memoryless

Differential implementation (fig. 10.18 p. 415)



Example: Fully differential SC-sigma-delta ADC published May 2007



A MICRO POWER SIGMA-DELTA A/D CONVERTER IN 0.35-μM CMOS FOR LOW FREQUENCY APPLICATIONS

Adnan Gundel[1,2], William N. Carr[1]
Email: adnangundel@ieee.org; william.carr@njit.edu

[1]New Jersey Institute of Technology, Newark, NJ 07102
[2]Telephonics Corporation, 815 Broad Hollow Road, Farmingdale, NY 11735

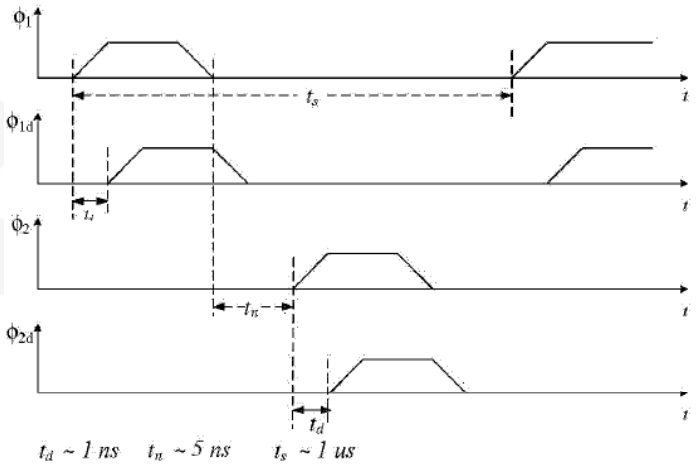


Figure 4. Nonoverlapping clock phases.

- Downloaded from IEEEXplore (http://ieeexplore.ieee.org/Xplore/dynhome.jsp)

Properties of Fully Differential Filters, compared to single-ended solutions

- Requires two copies of a single-ended filter except from the Opamp which is shared
- Common-mode feedback circuitry is required
- The input- and output signal amplitude are doubled. The same dynamic range can be achieved with half-sized capacitors:
  - Area reduction and less power consumption
  - Reduced size of switches (less charge)
- More wires are required
- Improved performance with respect to noise and distortion

Some Active RC 1st order filters (Sedra & Smith p. 779). Filter in fig 10.14 in ”Johns & Martin” lowermost.

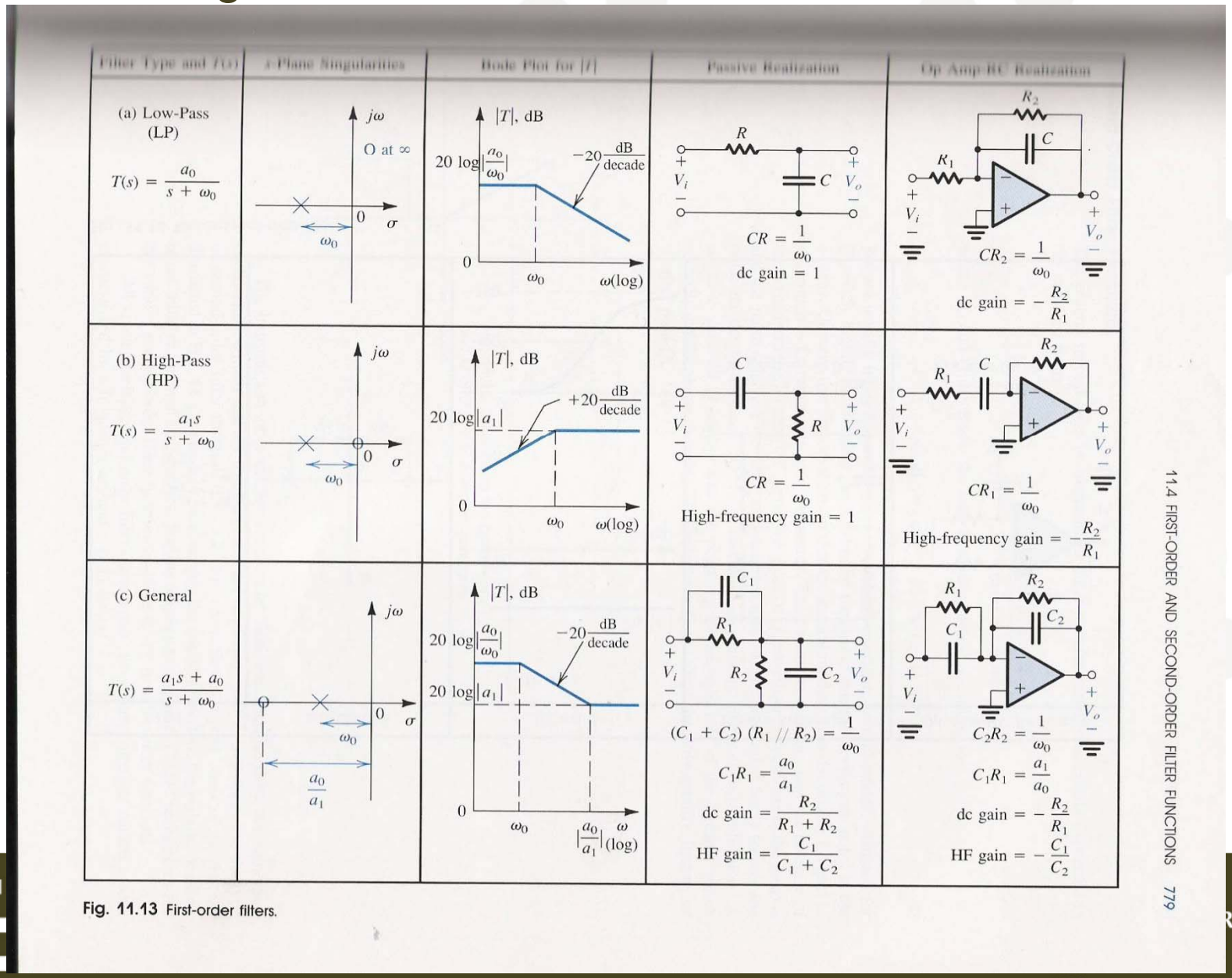
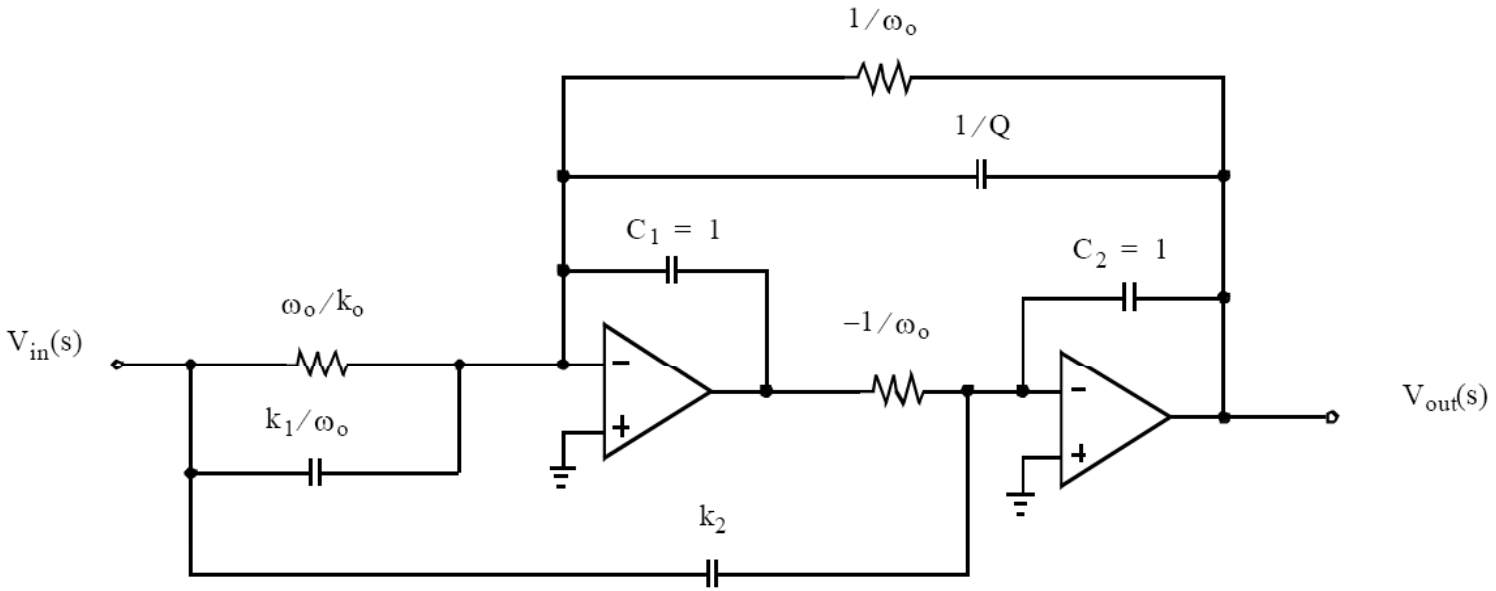


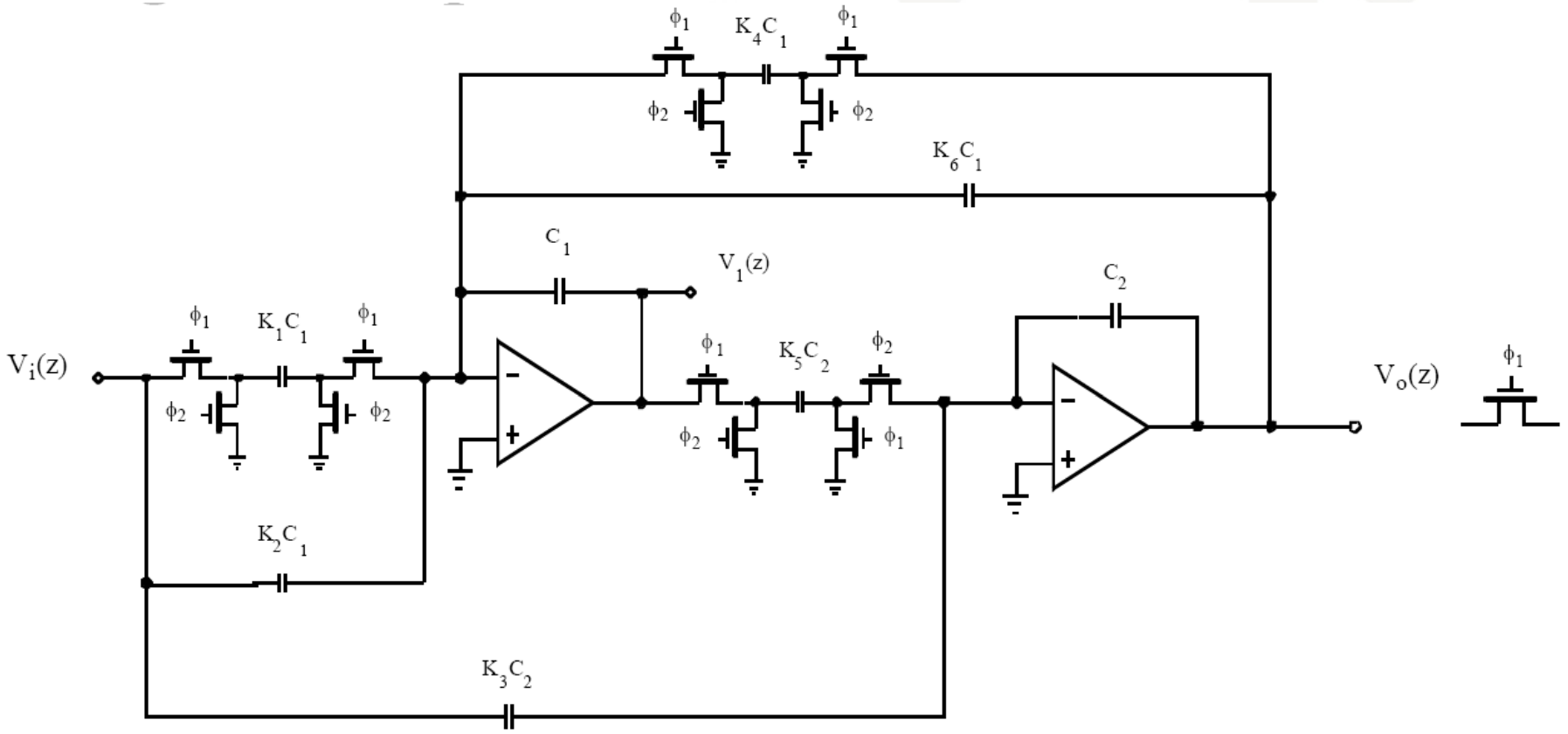
Fig. 11.13 First-order filters.

High-Q Biquad active RC-filter



- Another circuit is required for high Q-values and small capacitor spread
- Q-damping is obtained by adding a capacitor around both integrators instead of a resistive feedback around the last integrator

High-Q Switched-capacitor biquad filter (Fig. 10.25, p. 421) by changing the resistors with SC-equivalents



High-Q Biquad Filter

- General transfer function:

$$H(z) \equiv \frac{V_o(z)}{V_i(z)} = -\frac{K_3 z^2 + (K_1K_5 + K_2K_5 - 2K_3)z + (K_3 - K_2K_5)}{z^2 + (K_4K_5 + K_5K_6 - 2)z + (1 - K_5K_6)}$$

- The function can be rewritten as:

$$H(z) = -\frac{a_2 z^2 + a_1 z + a_0}{z^2 + b_1 z + b_0}$$

- The coefficients are then:

$$K_1K_5 = a_0 + a_1 + a_2$$

$$K_2K_5 = a_2 - a_0$$

$$K_3 = a_2$$

$$K_4K_5 = 1 + b_0 + b_1$$

$$K_5K_6 = 1 - b_0$$

- A signal-flow-graph approach is used to find the transfer function. There is some freedom in chossing the coefficients as there is one less equation than the number of coefficients. K4 = K5 = SQR (1+b0 + b1) defines the other ratios.

Ex 10.5 1) BP-filter, peak gain 5 near fs/10 amd Q of about 10

$$H(z) = -\frac{0.288\,(z-1)}{z^2 - 1.5722 + 0.9429}$$

Find the largest to smallest capacitor ratio if this transfer function is realized using the high-Q biquad circuit. Let $C_1 = C_2$.

(10.74): $K_4 = K_5 = \sqrt{1 + b_0 + b_1} = \sqrt{1 + 0.9429 + 1.572}$

$= \sqrt{0.3709} = 0.6090$

$K_5 - K_6 = 1 - b_0 \Leftrightarrow K_6 = \frac{(1-b_0)}{K_5}$

$= \frac{1 - 0.9429}{0.6090} = \frac{0.0571}{0.6090}$

$= 0.0938$

(10.71) $K_3 = a_2 = 0$ (Sec 10.68)

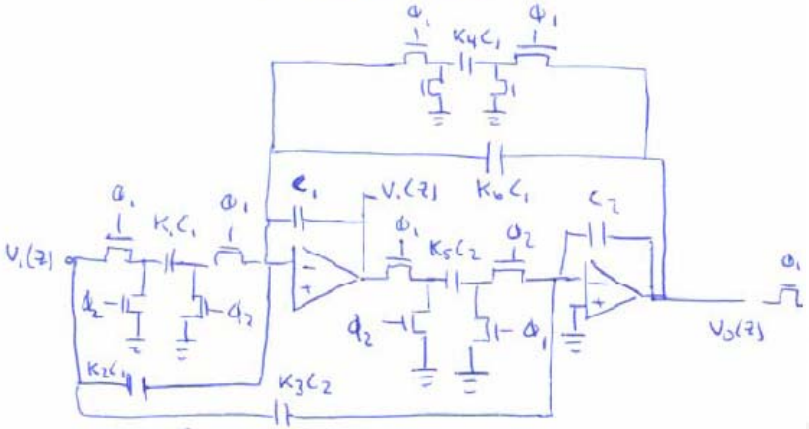
(10.69): $K_1 K_5 = a_0 + a_1 + a_2$

$K_1 = (a_0 + a_1 + a_2)/K_5$

$= \frac{-0.288 + 0.288}{0.6090} = 0$

(10.70) $K_2 - K_5 = a_2 - a_0 \Leftrightarrow K_2 = \frac{0 + 0.288}{0.6090} = 0.4729$

10.68: $H(z) = -\frac{a_2 z^2 + a_1 z + a_0}{z^2 + b_1 z + b_0}$



$C_1 = C_2 = 1$

$K_1 \cdot C_1 = 0$

$K_2 \cdot C_1 = 0.4729 \cdot C_1$

$K_3 \cdot C_2 = 0$

$K_4 \cdot C_1 = 0.6090 \cdot C_1$

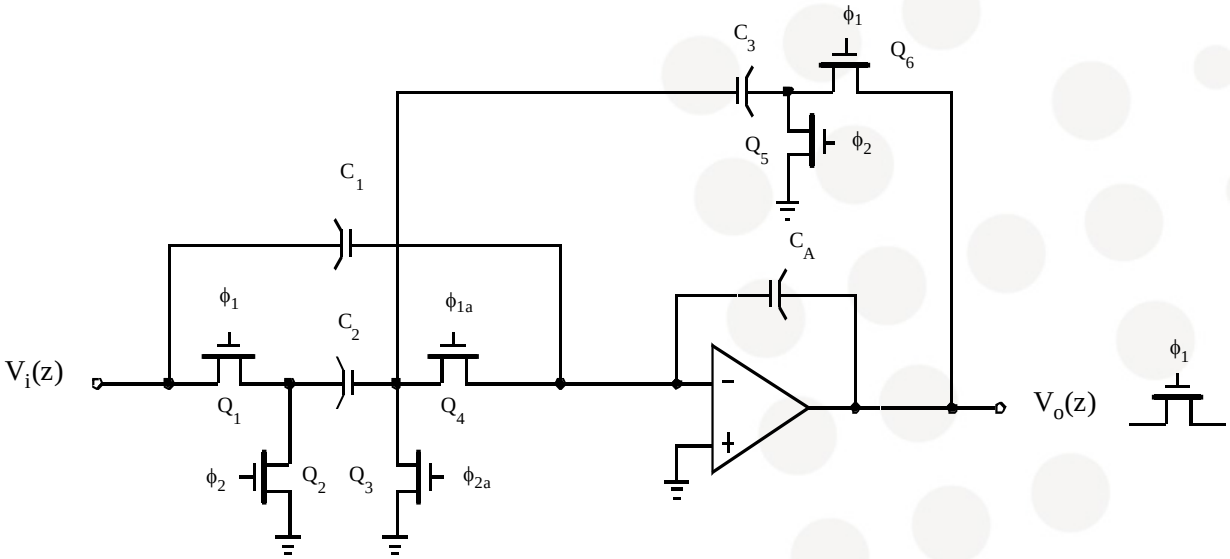
$K_5 \cdot C_2 = 0.6090 \cdot C_1$

$K_6 \cdot C_1 = 0.0938 \cdot C_1$

$\frac{C_1}{K_6 C_1} = \frac{1}{0.0938} = 10.66$

Max. capacitance spread is 10.66

Charge Injection (chapter 10.5)



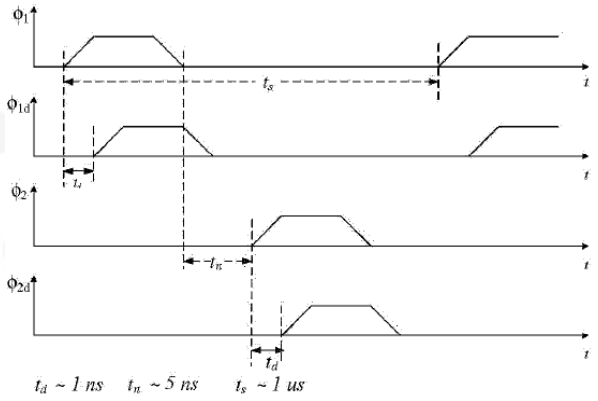
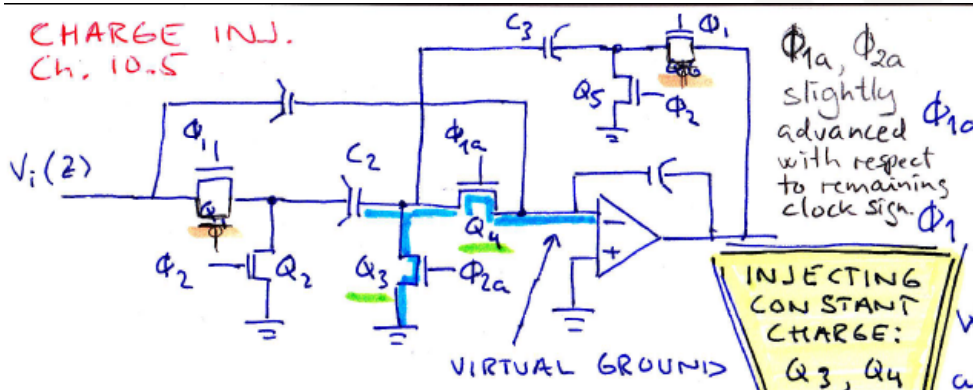


Figure 4. Nonoverlapping clock phases.

- To reduce the effects of charge injection in SC circuits, realize all switches connected to ground or virtual ground as n-channel switches only, and turn off the switches connected to ground or virtual ground first. Such an approach will minimize distortion and gain error as well as keeping DC offset low.
- In this case θ_{1a} and θ_{2a} are turned off first to prevent other switches affecting the output voltage of the circuit.

CHARGE INJ.
Ch. 10.5



Φ_{1a}, Φ_{2a} slightly advanced with respect to remaining clock sign.

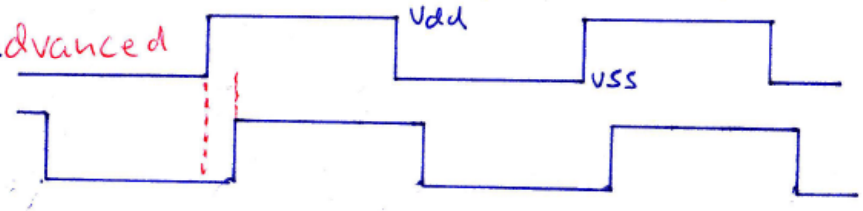
INJECTING CONSTANT CHARGE: Q_3, Q_4 Q_2, Q_5

Q_3 and Q_4 connect to ground or virtual ground, respectively, meaning that when they are turned on (Φ_{2a} = Vdd or Φ_{1a} = Vdd) they need only pass a signal near the ground node (VSS = 0V).

These two switches can be realized using single n-channel transistors. A 2nd important reason for this is that the charge injections due to Q_3 and Q_4 are not signal dependent (as will be seen)

Channel charge of an NMOS in triode, (chapter 7): $Q_{CH} = -WLC_{ox} \cdot V_{eff}$

$$Q_{CH} = -WLC_{ox}(V_{GS} - V_t) \quad (10.82)$$



When Q_3 and Q_4 are on, $V_{GS} = V_{DD}$, and since their source remain at 0 volts, their V_t's remain constant (in eq 10.82): THE CHARGE INJECTED BY Q_3, Q_4 IS THE SAME FROM ONE CLOCK CYCLE TO THE NEXT, AND CAN BE CONSIDERED AS A DC OFFSET.

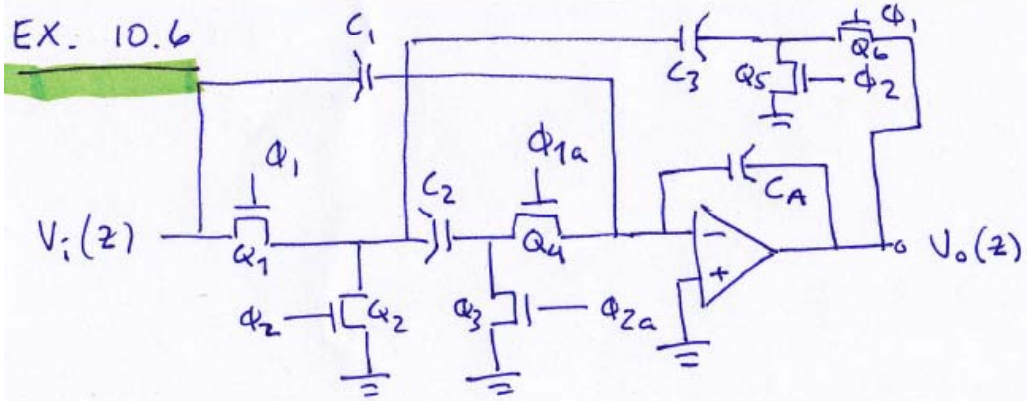
Unfortunately this is not the case for Q_1 and Q_6. Ex Q_1: $Q_{CH_1} = -W_1L_1C_{ox}(V_{DD} - V_i - V_{tn})$

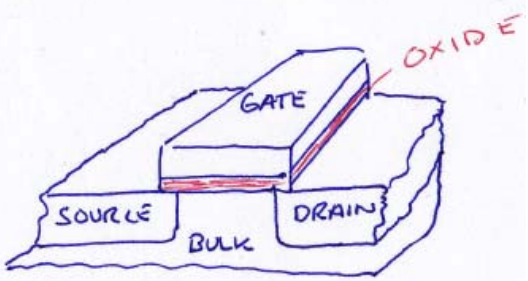
In this case one portion of the channel charge is linearly related to V_i. The V_{tn} changes in a nonlinear relationship (bulk effect). Q_{CH1} has a lin. and nonlin. relationship to V_i and would cause a gain error and distortion if Q_1 were turned off early.

TO MINIMIZE DISTORTION, GAIN ERR. AND DC OFFS.:

TO REDUCE THE EFFECTS OF CHARGE-INJECTION IN SC-CIRCUITS, REALIZE ALL SWITCHES CONNECTED TO GROUND OR VIRTUAL GROUND AS n-CHANNEL SWITCHES, AND TURN OFF THE SWITCHES NEAR THE VIRTUAL GROUND OF THE OPAMPS FIRST.

Ex. 10.6 (1/2)





Assume an ideal opamp. Estimate the amount of dc offset at the output due to channel-charge injection when $C_1 = 0$ and $C_2 = C_A = 10\ C_3 = 10\ pF$. $V_{tn} = 0.8V$, $W = 30\ \mu m$, $L = 0.8\ \mu m$. $V_{dd} = \pm 2.5V$

$C_{ox} = 3.9 \cdot 10^{-3}\ pF/(\mu m)^2$

Q_3 and Q_4 are advanced, and contribute with channel charge.

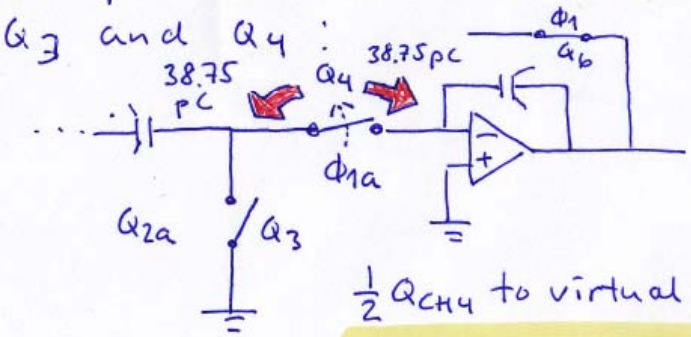
$$\underline{Q_{CH3}} = \underline{Q_{CH4}} = (-30 \cdot 10^{-6})(0.8 \cdot 10^{-6})\, 1.9 \cdot 10^{-3} \cdot \frac{10^{-12}}{(10^{-6})^2}(2.5 - 0.8)\,C$$

$$= -30 \cdot 0.8 \cdot 0.0019 \cdot 1.7\ pC = \underline{0.07752\ pC}$$

The dc feedback will keep the virtual input of the opamp at 0 volts. All feedback current is charge transferred through C_3.

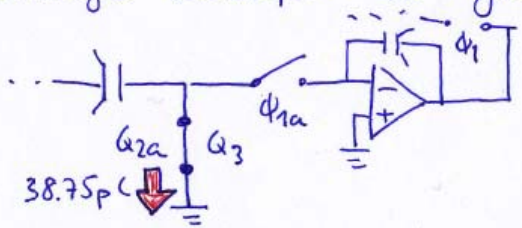
Ex. 10.6 (2/2)

When Φ_{1a} turns off, half the charge, Q_{CH4}, goes to virtual ground, while half of Q_{CH4} is placed on the node between Q_3 and Q_4:



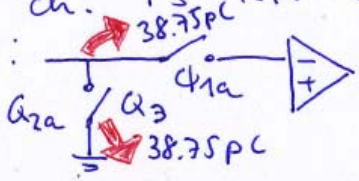
$\frac{1}{2} Q_{CH4}$ to virtual gnd = 38.75 pC

When Q_{2a} goes high, the 2nd charge escapes to ground:

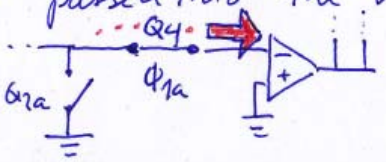


$Q = CV$

When Q_{2a} goes low, half of it's channel ch. is left between Q_3 and Q_4:



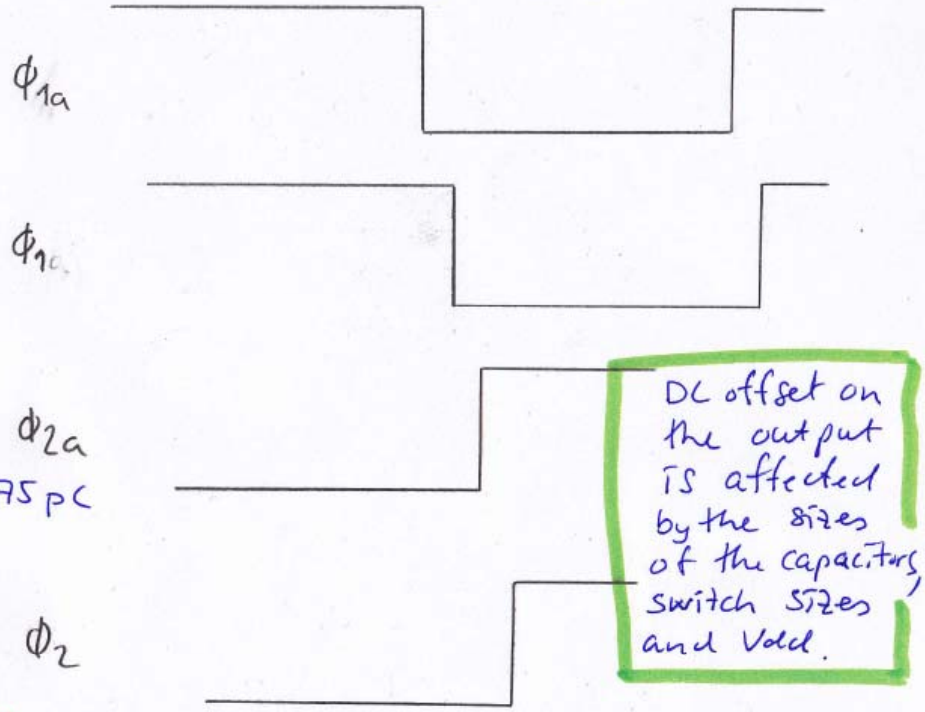
At "last" when Φ_{1a} goes high again, the previously mentioned charge package is passed into the virtual ground:



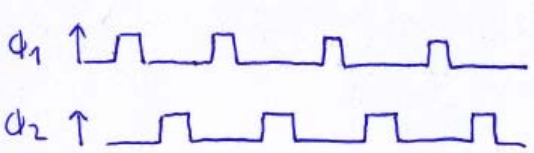
$\frac{1}{2} Q_{CH3}$ to virtual gnd = 38.75 pC

$V_{out} = \frac{Q_{C3}}{-C_3}$ $\quad \frac{Q_{C3}}{C_3} = \frac{77.5 \cdot 10^{-3} pC}{1pF} = 77.5mV$

$\frac{1}{2} Q_{CH4} + \frac{1}{2} Q_{CH3} = 77.5 \cdot 10^{-3} pC$

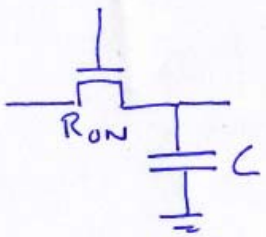


DC offset on the output is affected by the sizes of the capacitors, switch sizes and Vdd.



NON-OVERL. CLOCKS, PP. 398 IN "J & M".

CHARGE INJECTION AND HIGHER FREQUENCIES



$Q = CV$

$V = \frac{Q}{C}$

The smaller the R_{ON} and smaller the C, the higher the frequency of switching (possible)

$$H(s) = \frac{1}{1+\tau s} \quad \wedge \quad \tau = RC$$

To decrease R_{ON} the size of the switch increases, and thus the charge injection.

Will derive a simple formula that gives the upper bound on the frequency of operation of an SC circ. for a max. voltage change due to charge inj.: (ignore overlap capacitance)

MOST SC CIRC. HAVE 2 SERIES SWITCHES PER CAPACITOR. AS A RULE OF THUMB, FOR 6000 SETTLING, THE SAMPLING CLOCK HALF PERIOD MUST BE GREATER THAN 5 TIME CONST.

$$\frac{T}{2} > 5 R_{ON} \cdot C \iff f_{clk} < \frac{1}{10 R_{ON} C} \quad (10.89)$$

$$f_{clk} = \frac{1}{T}$$

$$R_{ON} = \frac{1}{\mu_n C_{ox} \cdot \frac{W}{L} \cdot V_{eff}} \quad (1.108)$$

Using (10.83) the charge change due to the channel charge caused by turning an n-channel switch off is approximated by

$$|\Delta V| = \frac{1}{2} Q_{CH} \cdot \frac{1}{C} = \frac{WL C_{ox} V_{eff}}{2C}$$

For a specified $|\Delta V|_{max}$

$$C = \frac{WL C_{ox} V_{eff}}{2 |\Delta V|_{max}}$$

Substituting in (10.89):

$$f_{clk} < \frac{1}{10 \cdot \frac{1}{\mu_n C_{ox} \frac{W}{L} V_{eff}} \frac{WL C_{ox} V_{eff}}{2 |\Delta V|_{max}}}$$

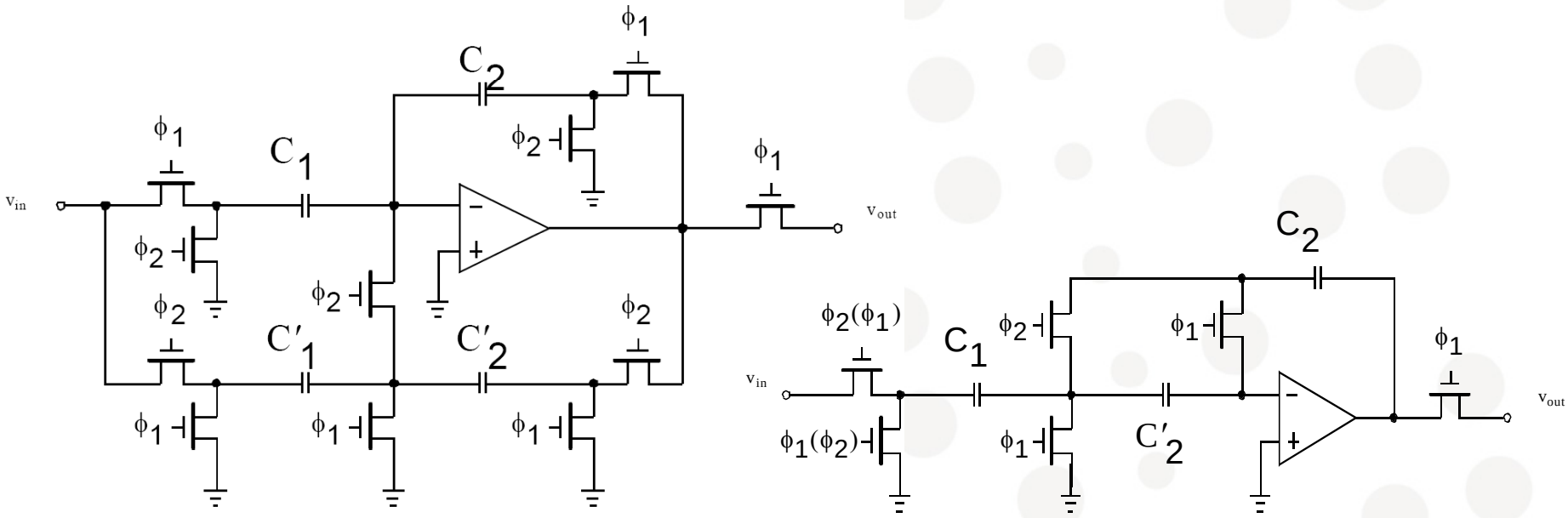
$$f_{clk} < \frac{\mu_n |\Delta V|_{max}}{5 L^2}$$

$\Rightarrow$: UPPER FREQ. LIMIT INVERSELY PROPORTIONAL TO L^2. IT IGNORES OVERLAP CAP. AND IS SOMEWHAT OPTIMISTIC

Correlated Double Sampling (”CDS”)

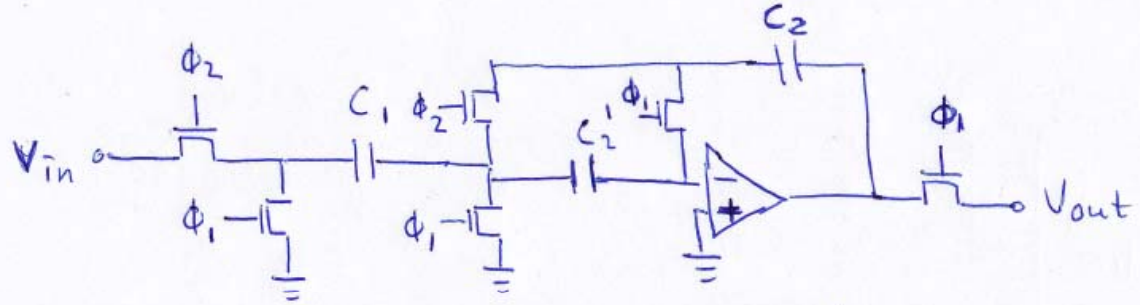
- Used to realize highly accurate gain amplifiers, sample-and-hold circuits and integrators to reduce errors due to offset voltages, 1/f noise and finite opamp gain.
- Method: During a calibration phase the input voltage of an opamp is sampled and stored (accross a C) and later subtracted from the signal in the operational phase (when the output is being sampled), by appropriate switching of the capacitors.
- A detailed description is beyond the scope of the text in ”J & M”. The interested reader may check : C. G. Themes, C. Enz: ”Circuit techniques for reducing the effects of opamp imperfections: Autozeroing, Correlated Double Sampling, and Chopper Stabilization”, Proceedings of the IEEE, Nov. 1996.

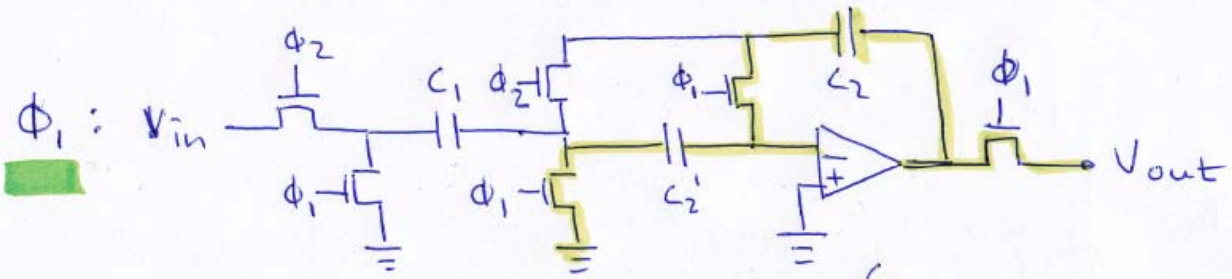
SC amplifier (left) and SC integrator with CDS (right)

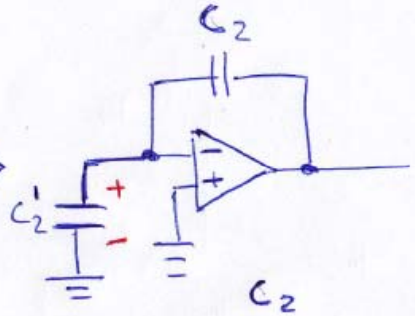


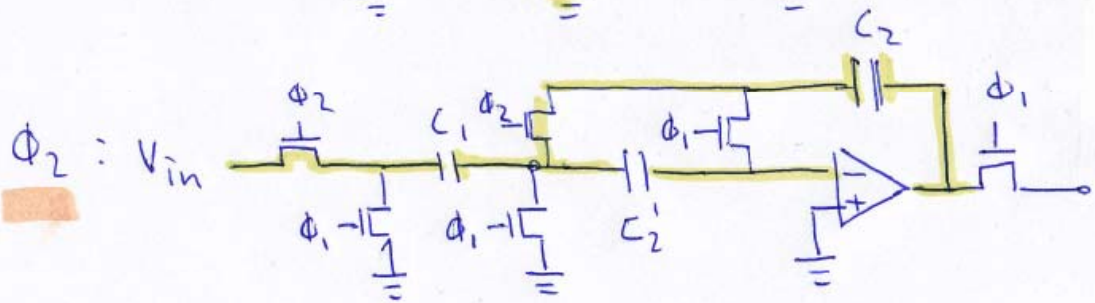
- For the amplifier: During θ2 the error is sampled and stored across C1 and C2
- The stored error is then subtracted during θ1
- For the integrator: During θ1 the error is sampled and stored across C'2
- The stored error is then subtracted during θ2

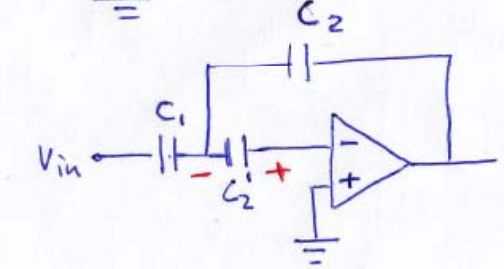
CORRELATED DOUBLE SAMPLING







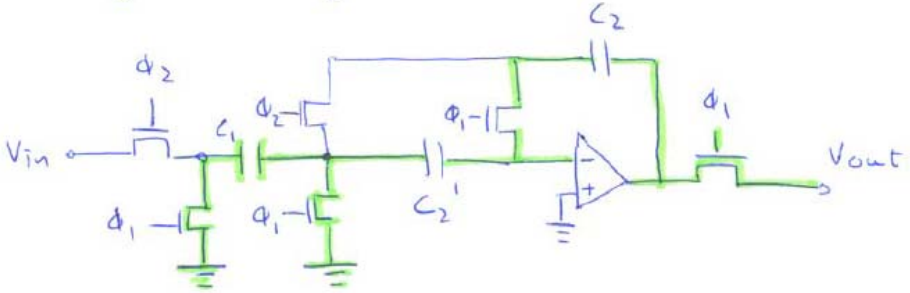




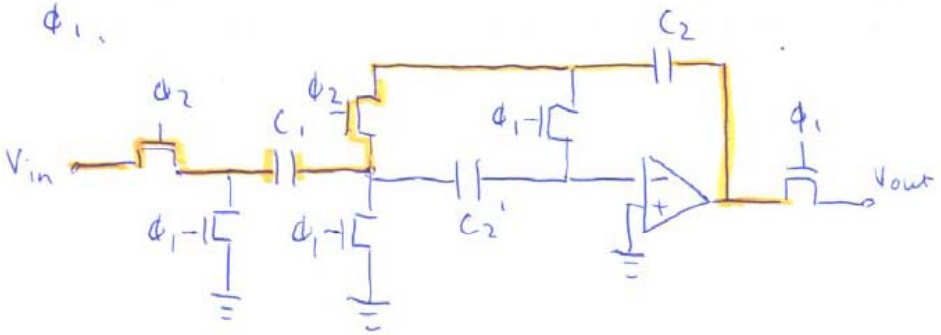
The opamp input error voltage is sampled during ϕ_1. Next, during ϕ_2', C_2' is connected in series with the opamp's inverting input and greatly minimizes the effects of those errors (by a factor of the inverse of the opamp's gain over what would otherwise occur at frequencies substantially less than the sampling frequency).

CORRELATED DOUBLE SAMPLING (CDS)

Integrator, fig. 10.35



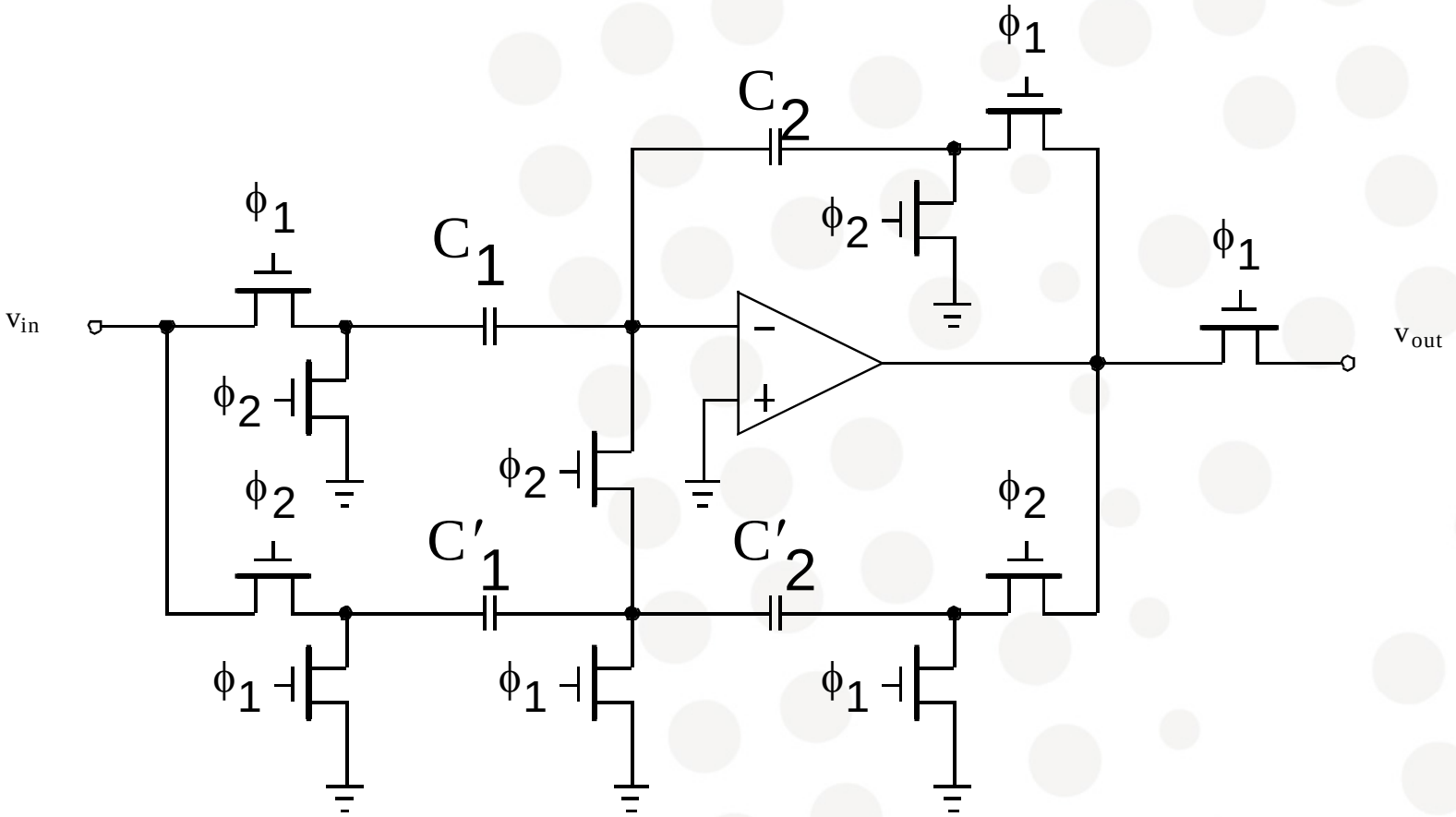
An additional capacitor, C_2' samples the opamp input error voltage during ϕ_1.



During ϕ_2, C_2' is connected in series with the opamp's inverting input and greatly minimizes the effects of these errors

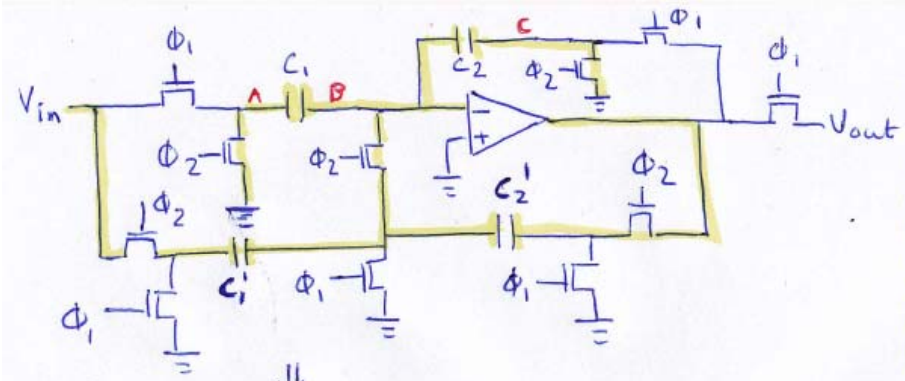
- Reducing errors by a factor of the inverse of the opamp's gain over what would otherwise occur at frequencies substantially less than the sampling frequency
- When CDS is used, the opamps should be designed to minimize thermal noise rather than 1/f noise.
- When used in SC-filters only a couple among the stages typically need CDS
- Very useful in over-sampling A/D converters.

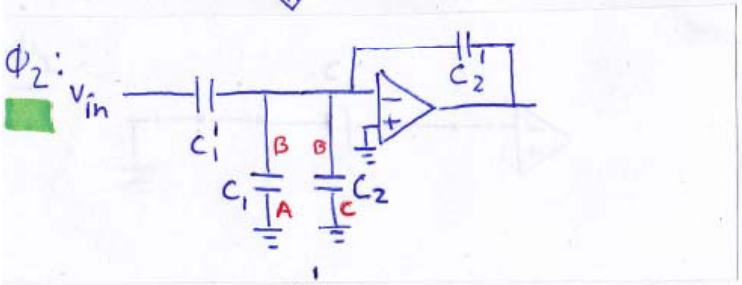
SC-integrator with CDS (”J & M” page 434)



- During Phi2 the error is sampled and stored accross C2

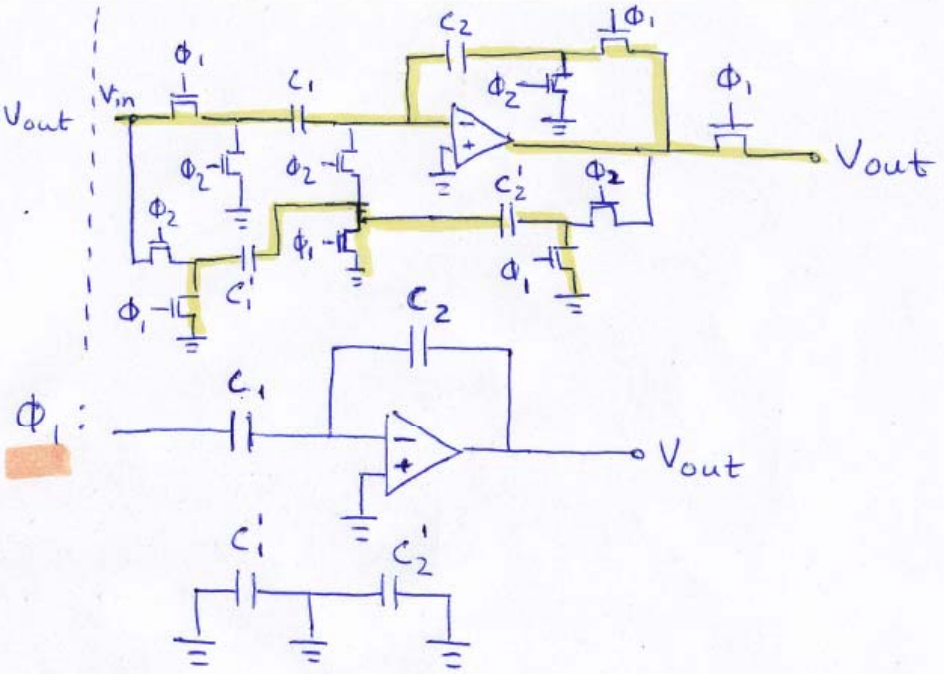
”
Johns & Martin” page 434





$$V_{out} \cong -\frac{C_1'}{C_2'} \cdot V_{in}$$

Errors due to finite-offset voltage, 1/f noise and gain are included. At the same time the finite opamp input voltage caused by these errors is sampled and stored accross C_1 and C_2.



Next, during Φ_1, this input error voltage is subtracted from the signal (applied to the opamp input) at that time.
Assuming that the input voltage and the opamp input error voltages did not change appreciably from Φ_1 to Φ_2, errors due to them will be significantly reduced.

Data Converter Fundamentals (chapter 11)

Main data converter types:

- Nyquist-rate converters:
  - Each value has a one-to-one correspondencewith a single input
  - The sample-rate must be at least equal to twice the signal frequency (Typically somewhat higher)
- Oversampled converters:
  - The sample-rate is much higher than the signal frequency, typically 20 – 512 times.
  - The extra samples are used to increase the SNR
  - Often combined with noise shaping

Flash ADC from 1926 (Analog Digital Conversion handbook, Analog Devices)

The first documented flash converter was part of Paul M. Rainey's electro-mechanical PCM facsimile system described in a relatively ignored patent filed in 1921 (Reference 5—see further discussions in Chapter 1 of this book). In the ADC, a current proportional to the intensity of light drives a galvanometer which in turn moves another beam of light which activates one of 32 individual photocells, depending upon the amount of galvanometer deflection (see Figure 3.49). Each individual photocell output activates part of a relay network which generates the 5-bit binary code.

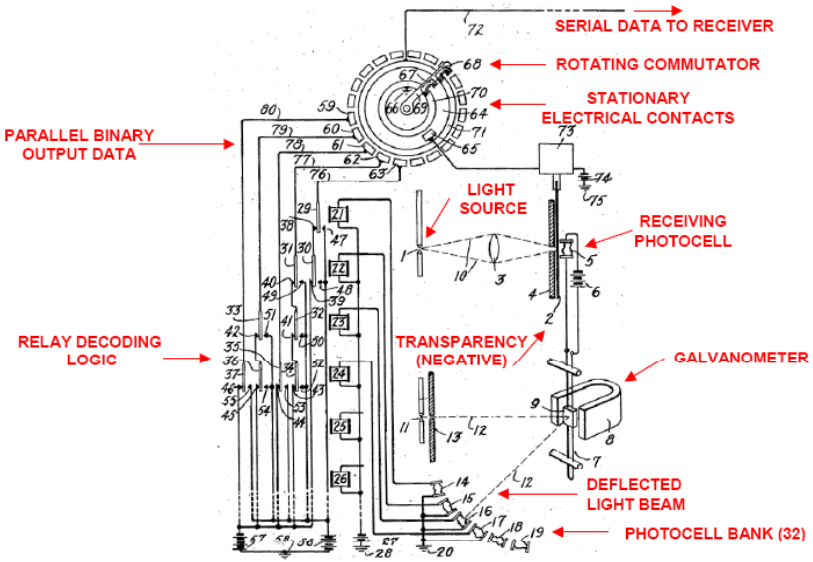
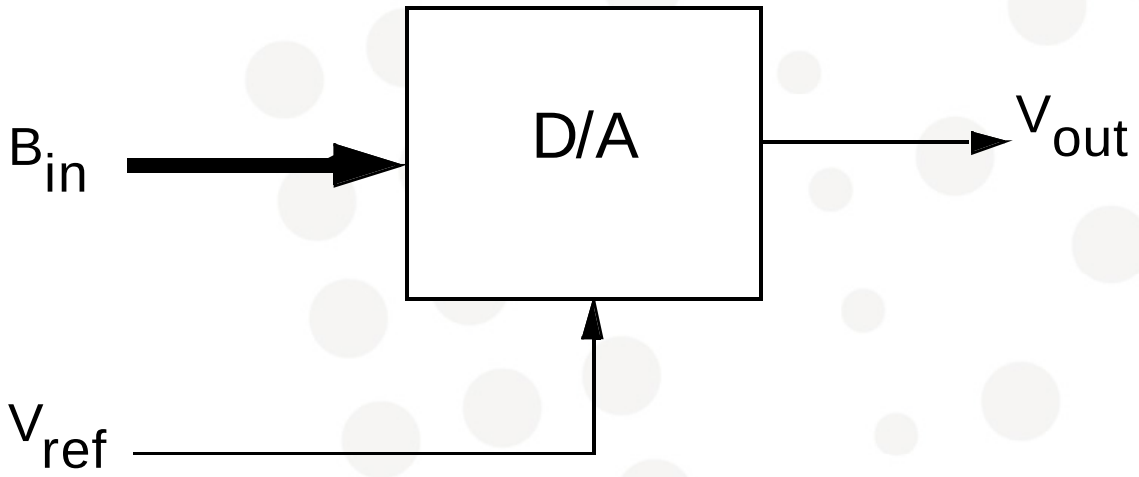


Figure 3.49: *A 5-Bit Flash ADC Proposed by Paul Rainey*
Adapted from Paul M. Rainey, "Facsimile Telegraph System," U.S. Patent 1,608,527, Filed July 20, 1921, Issued November 30, 1926

11.1 Ideal D/A converter



$$B_{in} = b_1 2^{-1} + b_2 2^{-2} + \ldots + b_N 2^{-N}$$

$$V_{out} = V_{ref}(b_1 2^{-1} + b_2 2^{-2} + \ldots + b_N 2^{-N})$$

Example 11.1 : 8-bit D/A converter

An ideal D/A converter has

$$V_{ref} = 5\ V$$

Find Vout when

$$B_{in} = 10110100$$

$$B_{in} = 2^{-1} + 2^{-3} + 2^{-4} + 2^{-6} = 0{,}703125$$

$$V_{out} = V_{ref} B_{in} = 3{,}516\ V$$

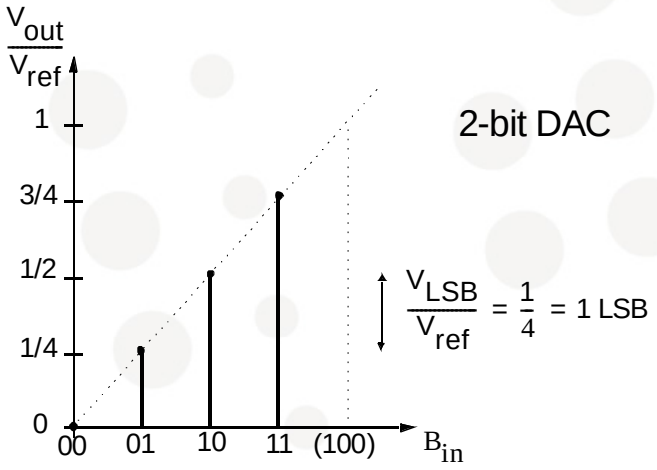
Find

$$V_{LSB}$$

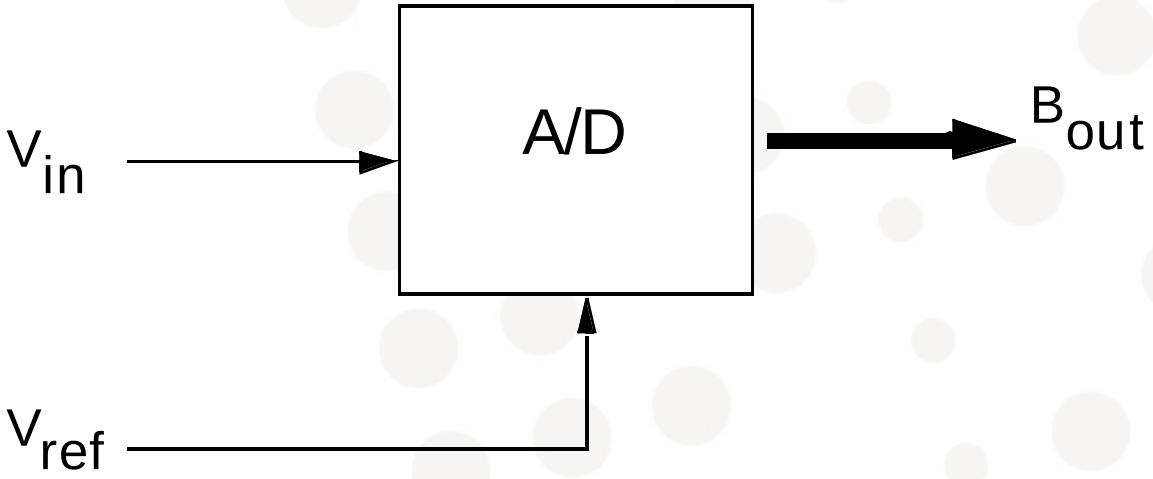
$$V_{LSB} = 5/256 = 19{,}5\ mV$$

$$V_{LSB} \equiv \frac{V_{ref}}{2^N}$$

$$1\ LSB = \frac{1}{2^N}$$



11.2 Ideal A/D converter (Fig. 11.3)

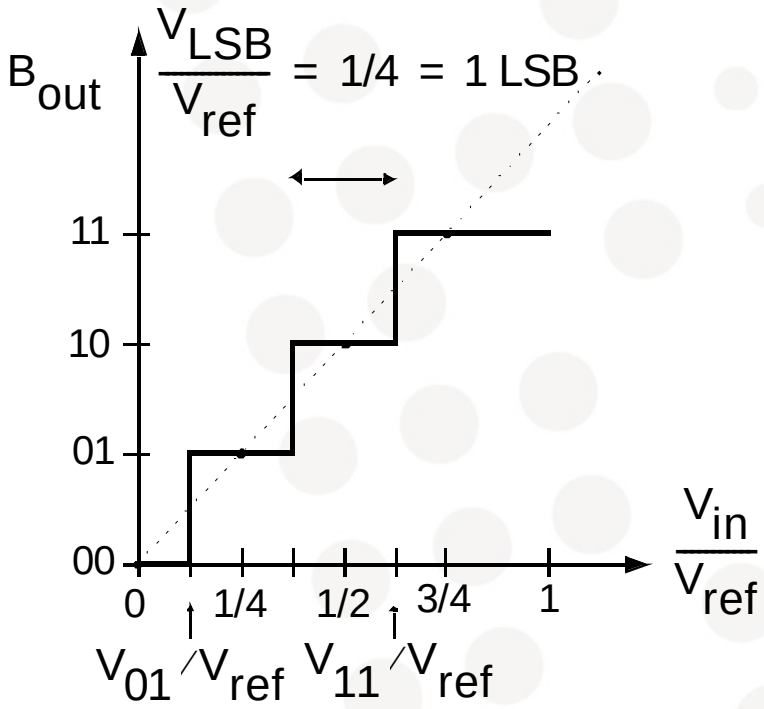


$$V_{ref}(b_1 2^{-1} + b_2 2^{-2} + \ldots + b_N 2^{-N}) = V_{in} \pm V_x$$

where

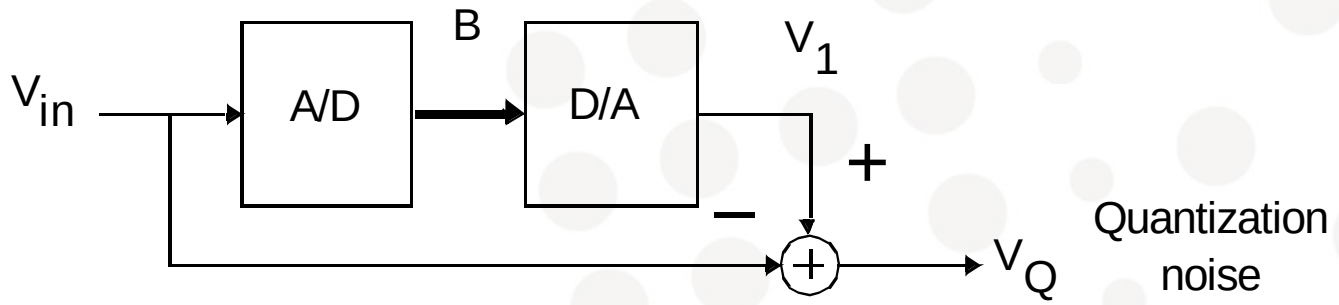
$$-\frac{1}{2}V_{LSB} \leq V_x < \frac{1}{2}V_{LSB}$$

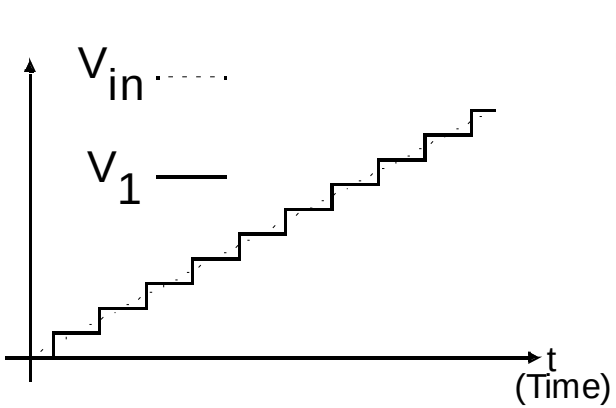
Ideal transfer curve for a 2-bit A/D converter (Fig. 11.4)

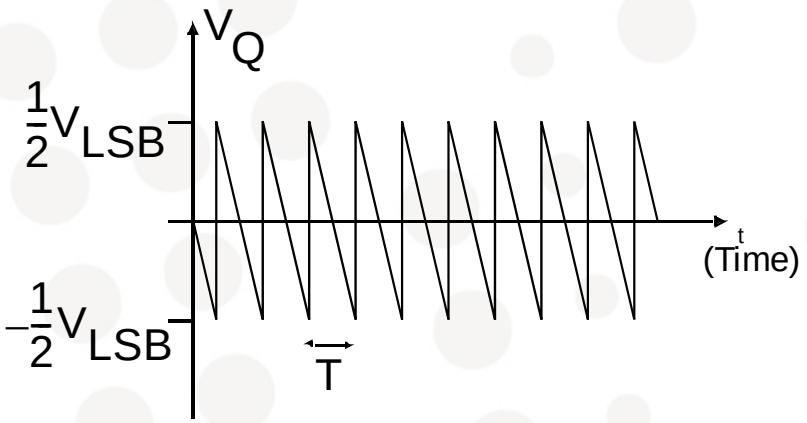


- A range of input values produce the same output value (QA range of input values produce the same output value (Quantization error)
- Different from the D/A case

11.3 Quantization noise

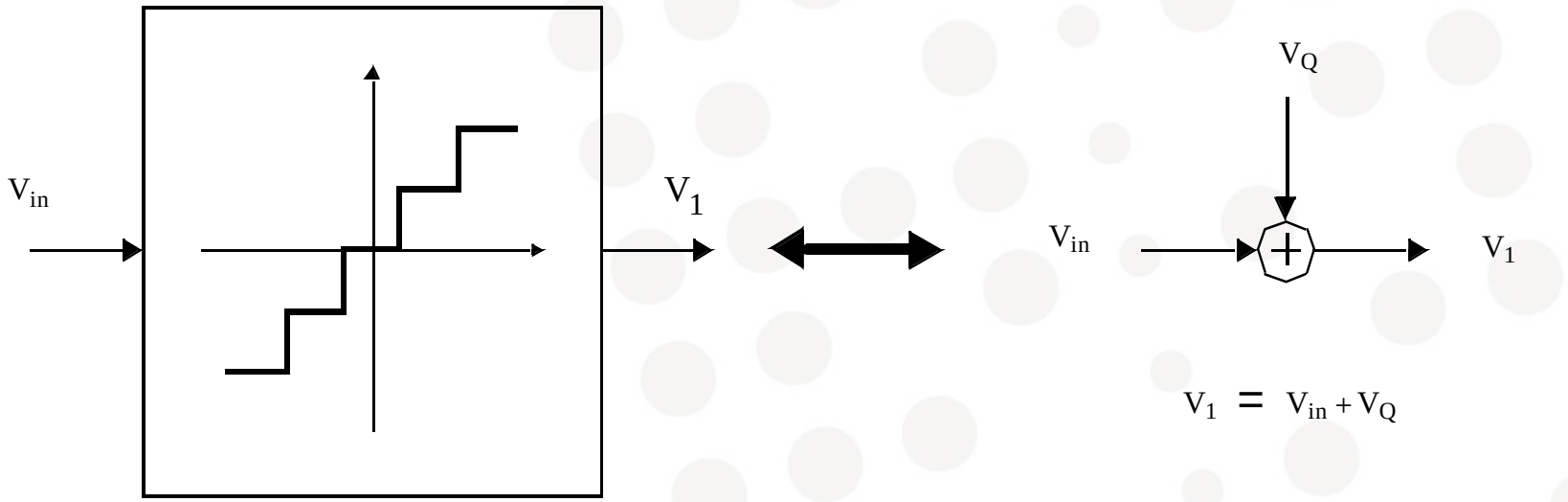






$$V_Q = V_1 - V_{in}$$

Quantization noise model



Quantizer

Model

- The model is exact as long as V_Q is properly defined
- V_Q is most often assumed to be white and uniformely distributed between +/- $V_{lsb}/2$

Quantization noise

- The rms-value of the quantization noise can be shown to be:

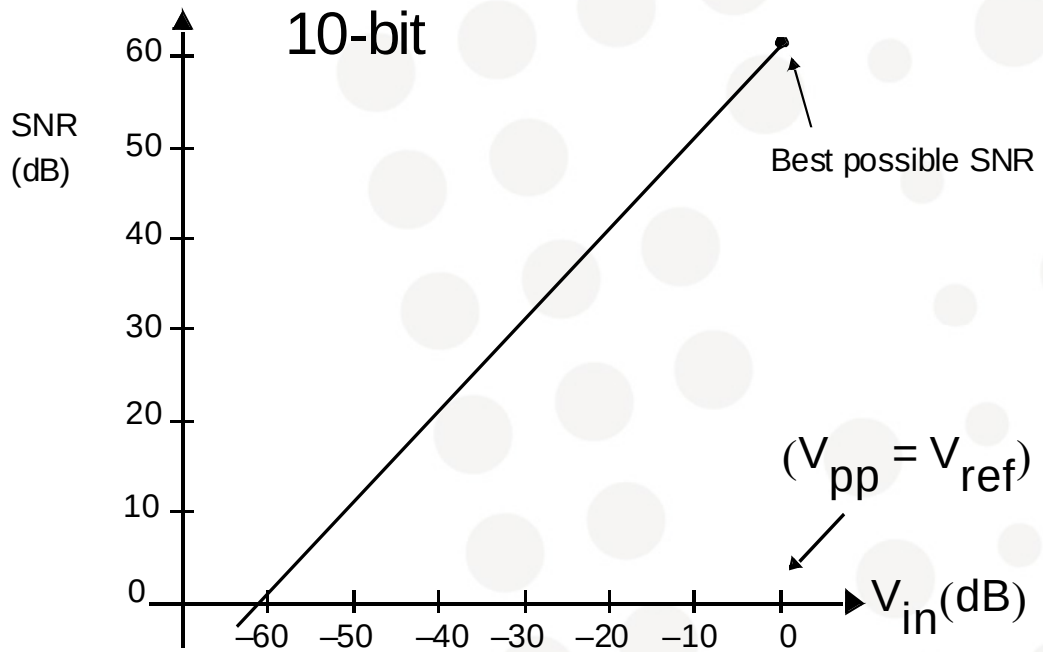
$$V_{Q(rms)} = \frac{V_{LSB}}{\sqrt{12}}$$

- Total noise power is independent of sampling frequency
- In the case of a sinusoidal input signal with p-p amplitude of $V_{ref}/2$

$$SNR = 20\log\left(\frac{V_{in(rms)}}{V_{Q(rms)}}\right) = 20\log\left(\frac{V_{ref}/(2\sqrt{2})}{V_{LSB}/(\sqrt{12})}\right)$$

$$SNR = 6{,}02N + 1{,}76\ \text{dB}$$

Quantization noise (SNR as a function of Vin)



•Signal-to Noise ratio is highest for maximum input signal amplitude

11.4 Signed codes

Table 11.1 Some 4-bit signed digital representations

Number	Normalized number	Sign magnitude	1's complement	Offset binary	2's complement
+7	+7/8	0111	0111	1111	0111
+6	+6/8	0110	0110	1110	0110
+5	+5/8	0101	0101	1101	0101
+4	+4/8	0100	0100	1100	0100
+3	+3/8	0011	0011	1011	0011
+2	+2/8	0010	0010	1010	0010
+1	+1/8	0001	0001	1001	0001
+0	+0	0000	0000	1000	0000
(–0)	(–0)	(1000)	(1111)		
–1	–1/8	1001	1110	0111	1111
–2	–2/8	1010	1101	0110	1110
–3	–3/8	1011	1100	0101	1101
–4	–4/8	1100	1011	0100	1100
–5	–5/8	1101	1010	0011	1011
–6	–6/8	1110	1001	0010	1010
–7	–7/8	1111	1000	0001	1001
–8	–8/8			0000	1000

- Unipolar / bipolar
- Common signed digital repr.: sign magnitude, 1's complement, 2's compl.
- Sign. M.: 5:0101, -5:1101, two repr. Of 0, 2^N-1 numb.
- 1's compl.: Neg. Numbers are complement of all bits for equiv. Pos. Number: 5:0101, -5:1010
- Offset bin: 0000 to the most neg., and then counting up..

  +: closely related to unipolar through simple offset

2's complement

A3a2a1a0	Sign magnitude	2s complement
0111	+7	+7
0110	+6	+6
0101	+5	+5
0100	+4	+4
0011	+3	+3
0010	+2	+2
0001	+1	+1
0000	+0	+0
1000	-0	-8
1001	-1	-7
1010	-2	-6
1011	-3	-5
1100	-4	-4
1101	-5	-3
1110	-6	-2
1111	-7	-1

- 5_{10} : 0101 = $2^2 + 2^0$
- -5_{10} : (0101)' +1 = 1010 + 1 = 1011

- Addition of positive and negative numbers is straightforward, using addition, and requires little hardware
- 2's complement is most popular representation for signed numbers when arithmetic operations have to be performed

7_{10}-6_{10} via addition using two's complement of -6

- 0000 0000 0000 0000 0000 0000 0000 $00111_2 = 7_{10}$
- 0000 0000 0000 0000 0000 0000 0000 $00110_2 = 6_{10}$
- *Subtraction uses addition: The appropriate operand is negated before being added*
- *Negating a two's complement number: Simply invert every 0 and 1 and add one to the result.* Example:
- 0000 0000 0000 0000 0000 0000 0000 0110_2 becomes
- 1111 1111 1111 1111 1111 1111 1111 1001_2

\+ 1_2

= 1111 1111 1111 1111 1111 1111 1111 1010_2

0000 0000 0000 0000 0000 0000 0000 $0111_2 = 7_{10}$

\+ 1111 1111 1111 1111 1111 1111 1111 $1010_2 = -6_{10}$

= 0000 0000 0000 0000 0000 0000 0000 $0001_2 = 1_{10}$

11.5 performance limitations

- Resolution
- Offset and gain error
- Accuracy
- Integral nonlinearity (INL) error
- Differential nonlinearity (DNL) error
- Monotonicity
- Missing codes
- A/D conversion time and sampling rate
- D/A settling time and sampling rate
- Sampling time uncertainty
- Dynamic range
- NB!! Different meanings and definitions of performance parameters sometimes exist. → Be sure what's meant in a particular specification or scientific paper.. There are also more than those mentioned here.

Resolution

- Resolution usually refers to the number of bits in the input (D/A) or output (ADC) word, and is often different from the accuracy.
- Analog-Digital Conversion Handbook, Analog Devices, 3rd Edition, 1986: *An n-bit binary converter should be able to provide 2n distinct and different analog output values corresponding to the set of n binary words. A converter that satisfies this criterion is said to have a resolution of n bits.*

A Cost-Efficient High-Speed 12-bit Pipeline ADC in 0.18-μm Digital CMOS

Terje Nortvedt Andersen, Bjørnar Hernes, *Member, IEEE*, Atle Briskemyr, Frode Telstø, Johnny Bjørnsen, *Member, IEEE*, Thomas E. Bonnerud, and Øystein Moldsvor

TABLE I
KEY DATA FOR THE ADC

Nominal sampling rate	110MS/s
Technology	0.18µm digital CMOS
Nominal supply voltage	1.8V
Resolution	12bit
Full scale analog input	$2V_{P-P}$
Area	$0.86mm^2$
Power consumption	97mW
DNL	±1.2 LSB
INL	-1.5/+1 LSB
SNR (f_{in}=10MHz)	67.1 dB
SNDR (f_{in}=10MHz)	64.2 dB
SFDR (f_{in}=10MHz)	69.4 dB
ENOB (f_{in}=10MHz)	10.4 bit

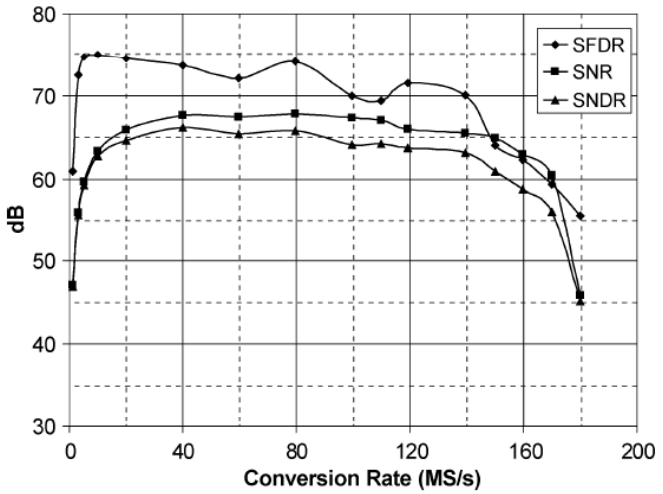


Fig. 8. SFDR, SNR, and SNDR versus conversion rate. The input frequency and signal swing is 10 MHz and $2V_{P-P}$, respectively.

Next Tuesday (2/3-10):

- Chapter 12 Nyquist DACs

Du er her: UiO > Studier > Emner > Matematikk og naturvitenskap > Informatikk > INF4420 > V10 >

Undervisningsplan (INF4420 - Vår 2010)

Dato	Undervises av	Sted	Tema	Kommentarer / ressurser
26.01.2010	Snorre Aunet ("SA")	Lille Auditorium, Ifi	introduksjon til INF4420	Slides. Slides, two per page .
02.02.2010	SA, Amir Hasanbegovic ("AH")	Lille Auditorium, Ifi.	From chapter 8 i "Johns & Martin". + SW intro (Cadence)	Slides. Slides, two per page . Other relevant material .
09.02.2010	SA	Lille Aud.	from chapters 8 and 9 in "Johns & Martin".	Slides. Slides, two per page .
16.02.2010	SA	Lille Aud.	9.2-9.6, 10.1-10.2	Slides Slides, two per page
23.02.2010	SA	Lille Aud.	Chapter 10.3, --> , beg. of chapter 11.	
02.03.2010	SA	Lille Aud.	chapter 12; Nyquist-rate DACs	
09.03.2010	SA	Lille Aud.	chapter 13; Nyquist-rate ADCs I	
16.03.2010	SA	Lille Aud.	chapter 13; Nyquist-rate ADCs II	
23.03.2010	SA	Lille Aud.	Chapter 14; Oversampling Converters	
30.03.2010				No teaching in week 13.
06.04.2010				No teaching in week 14, due to Easter holidays.
13.04.2010	SA	Lille Aud.	chapter 16; PLLs	
20.04.2010	SA, AH	Lille Aud.	"project meeting"	
27.04.2010	SA	Lille. Aud.	To be defined.	In case..
10.05.2010	AH	Lille Aud.	Selected problems relevant for the exam.	
11.05.2010	SA, AH	Lille Aud.	presentation of the project work.	

Redaksjon: Redaksjon for informasjon om studietilbudet ved UiO
Dokument opprettet: 26.12.2009, endret: 17.02.2010

Additional litterature

- Adnan Gundel, William N. Carr: A micropower sigma-delta A/D converter in 0.35 um CMOS for low-frequency applications, Proceedings of IEEE Long Island Systems, Applications and Technology Conference, IEEE 2007
- [GrTe86]: Roubik Gregorian, Gabor C. Temes: Analog MOS Integrated Circuits for signal processing, Wiley, 1986.
- [Haah94]: Nils Haaheim: Analog CMOS, Universitetet i Trondheim, Norges Tekniske Høgskole, 1994.
- Adel S. Sedra, Kenneth C. Smith: Microelectronic Circuits, Saunders College Publ., 1989.
- Kenneth R. Laker, Willy M. C. Sansen: Design of analog integrated circuits and systems, McGraw-Hill, 1994.

Additional litterature:

1506 IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. 40, NO. 7, JULY 2005

A Cost-Efficient High-Speed 12-bit Pipeline ADC in 0.18-μm Digital CMOS

Terje Nortvedt Andersen, Bjørnar Hernes, *Member, IEEE*, Atle Briskemyr, Frode Telstø, Johnny Bjørnsen, *Member, IEEE*, Thomas E. Bonnerud, and Øystein Moldsvor

ANALOG-DIGITAL CONVERSION

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