Nyquist Rate D/A Converters (12.1-12.4)

Tuesday 2nd of March, 2010, 9:15-11:00

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Last time – and today, Tuesday 2nd of March:

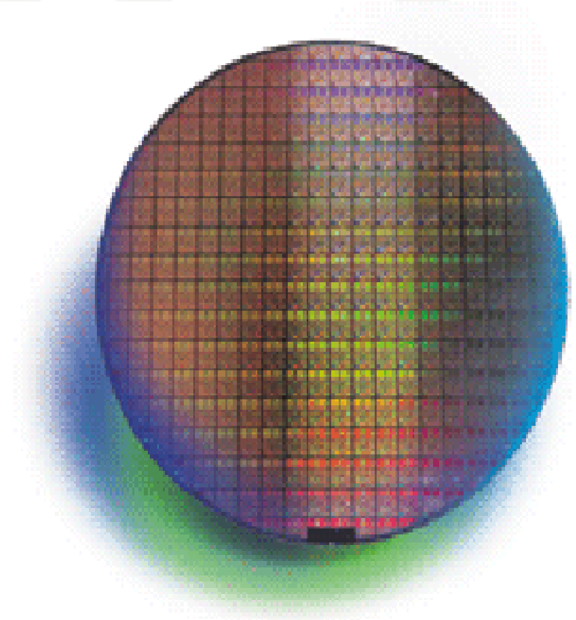
Last time:

10.3 First-order filters
10.4 Biquad filters (high-Q)
10.5 Charge injection
10.7 Correlated double sampling techniques
11.1 Ideal D/A converter
11.2 Ideal A/D converter
11.3 quantization noise
11.4 signed codes

Today:

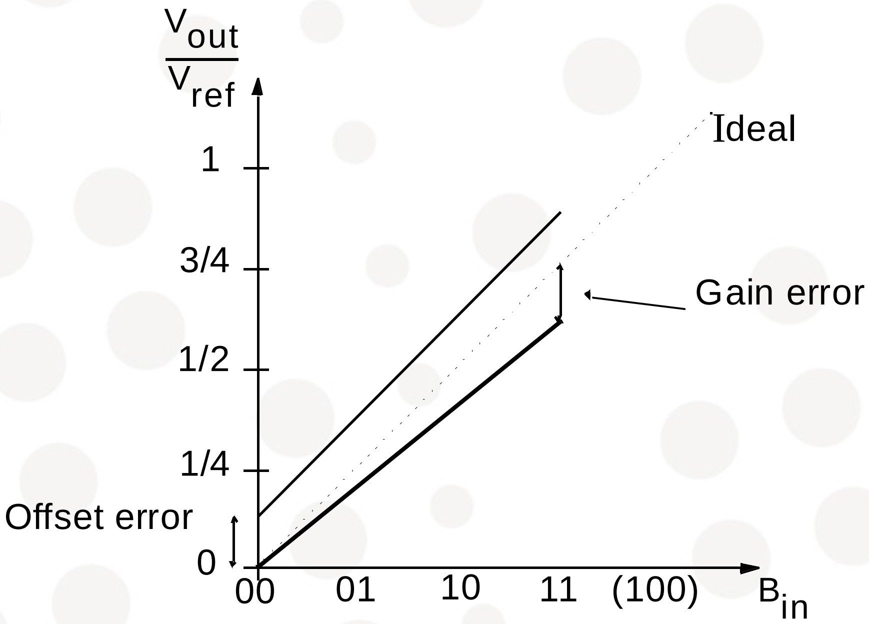
11.5 Performance Limitations
12.1 Decoder-based converters
12.2 Binary-scaled converters
12.3 Thermometer-code converters
12.4 Hybrid converters

10:55 : 5 minute survey by ”Micro”



Offset and gain error

- In a D/A converter ("DAC") the *offset error* is defined to be the output that occurs for the input code that should provide zero output. For an A/D converter ("ADC") the offset error is the deviation of V0…01 from ½ LSB.
- The gain error is the the difference at the full scale value between ideal and actual curves when the offset has been reduced to zero. For a DAC it is given in units of LSBs.

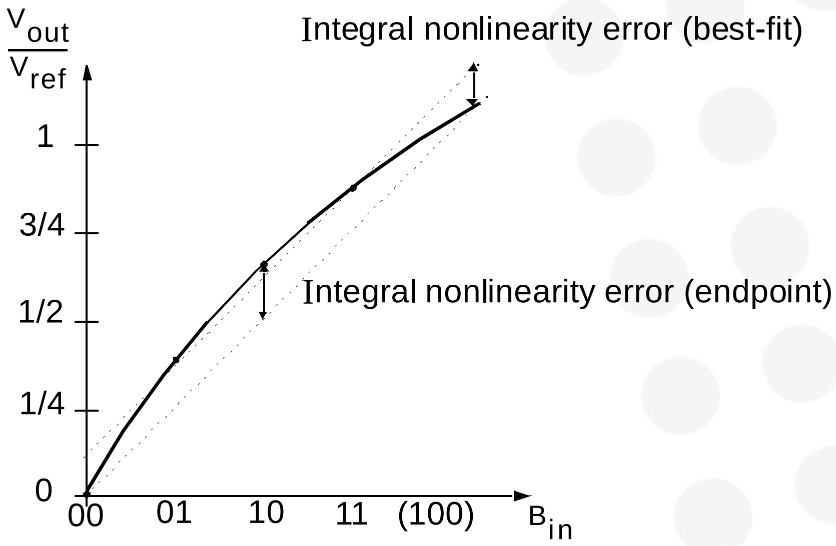


ADC:

given by

$$E_{gain(A/D)} = \left(\frac{V_{1\ldots1}}{V_{LSB}} - \frac{V_{0\ldots01}}{V_{LSB}}\right) - (2^N - 2) \qquad (11.25)$$

Integral nonlinearity error (INL)



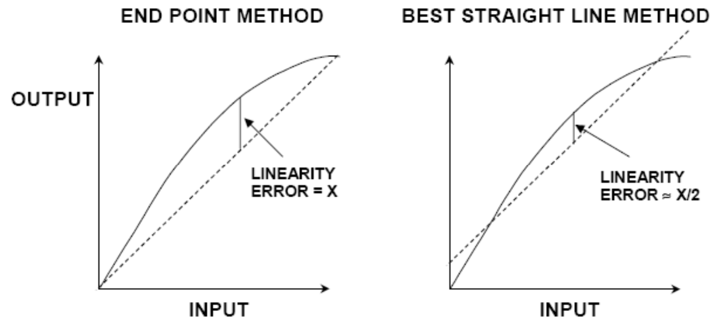
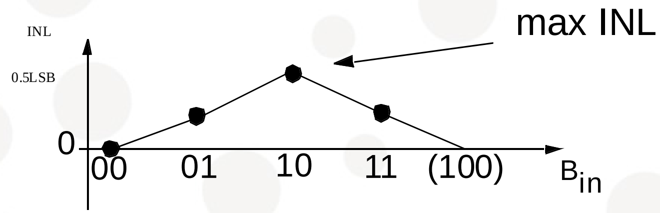
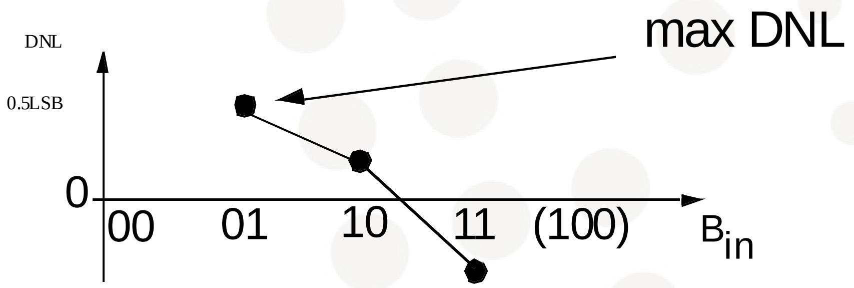


Figure 2.18: *Method of Measuring Integral Linearity Errors (Same Converter on Both Graphs)*



- After both offset and gain errors have been removed, the integral nonlinearity (INL) error is defined to be the deviation from a straight line. Possible straight lines: endpoints of the converters transfer respons, best-fit straight line such that the difference (or mean squared error) is minimized.

Differential nonlinearity error (DNL)

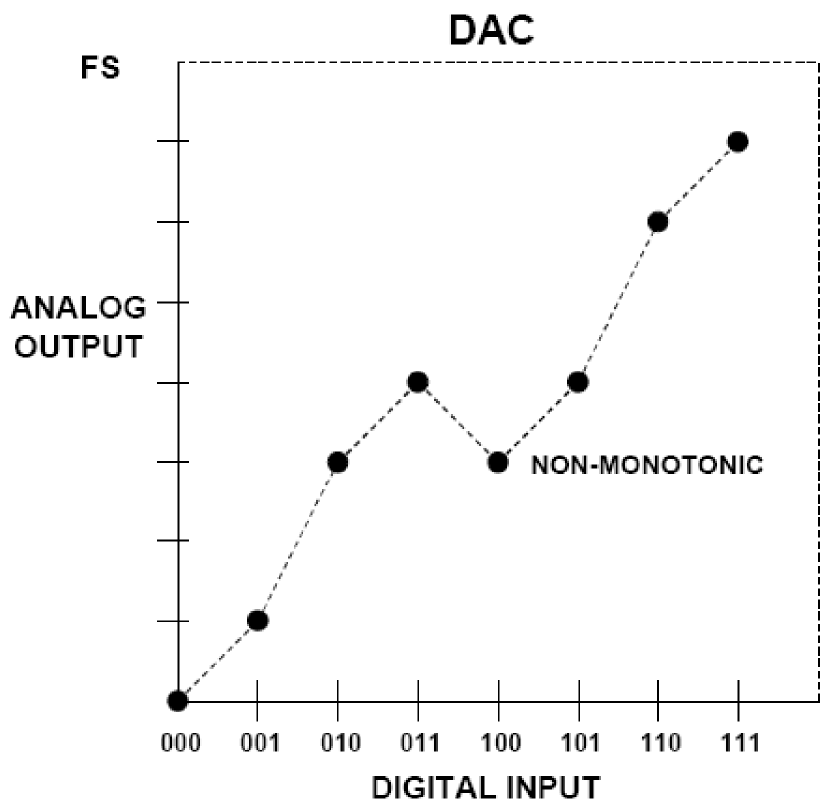


step size between 00 and 01 is 1.5 LSB
step size between 10 and 11 is 0.7 LSB

- Ideally, each analog step size is equal to 1 LSB. DNL is variation in step size from V_{LSB} (after removal of gain and offset errors). Ideally DNL is 0 for all digital values. DNL is in “J & M” defined for each digital word, whereas other sometimes refer to DNL as the maximum magnitude of DNL values.

Monotonicity in DACs

- A monotonic DAC is one in which the output always increases as the input increases (slope of the transfer response is of only one sign.)
- If the maximum DNL error is less than 1 LSB, the DAC is guaranteed to be monotonic.
- However, many monotonic converters may have a maximum DNL greater than 1 LSB.
- Similarly, a converter is guaranteed to be monotonic if maximum DNL is < 1 LSB.



- 3-bit nonmonotonic example in the figure is from Analog-Digital conversion handbook by Analog Devices

D/A (DAC) settling time and sampling rate

- In a DAC the settling time is defined as the time it takes for the converter to settle within some specified amount of the final value (usually 0.5 LSB).
- The sampling rate is the rate at which samples can be continously converted and is typically the inverse of the settling time.
- Different combinations of input vectors give different settling times. Picture from ”High-speed data converters fully integrated in CMOS”, dissertation for the dr. scient. degree by Leif Hanssen, Ifi, UiO, 1990.

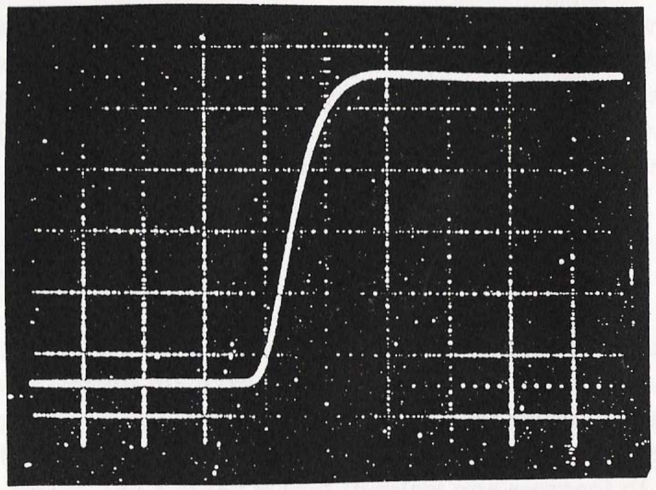
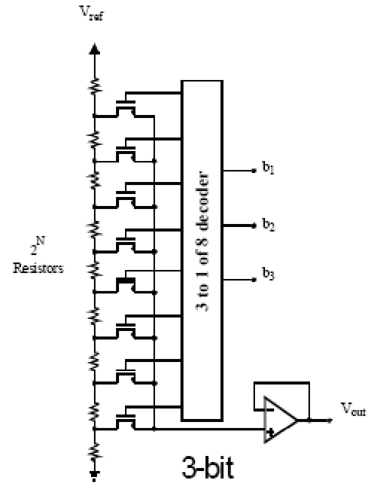
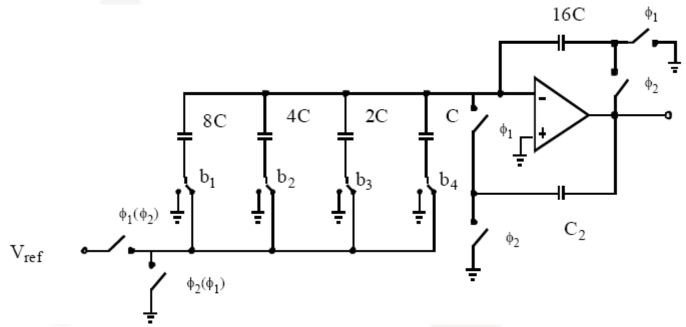


Fig 3.9 Risetime 6 bit DAC, input 0 to 128. (Xdivision = 50ns)

Nyquist Rate D/A Converters

- 12.1 Decoder-based converters
  - resistor string conv.
  - folded resistor string conv.
  - multiple R-string converters
- 12.2 Binary-Scaled converters
  - binary-weighted resistor converters
  - reduced resistance-ratio ladders
  - R-2R-based converters
  - charge-redistribution switched-capacitor conv.
  - current-mode conv.
- 12.3 Thermometer-code converters
  - thermometer-code current-mode D/A converters
  - single-supply positive-output converters
  - dynamically matched current sources
- 12.4 Hybrid converters
  - resistor-capacitor hybrid converters
  - segmented converters





Some systems exploiting data converters, "Allen & Holberg"

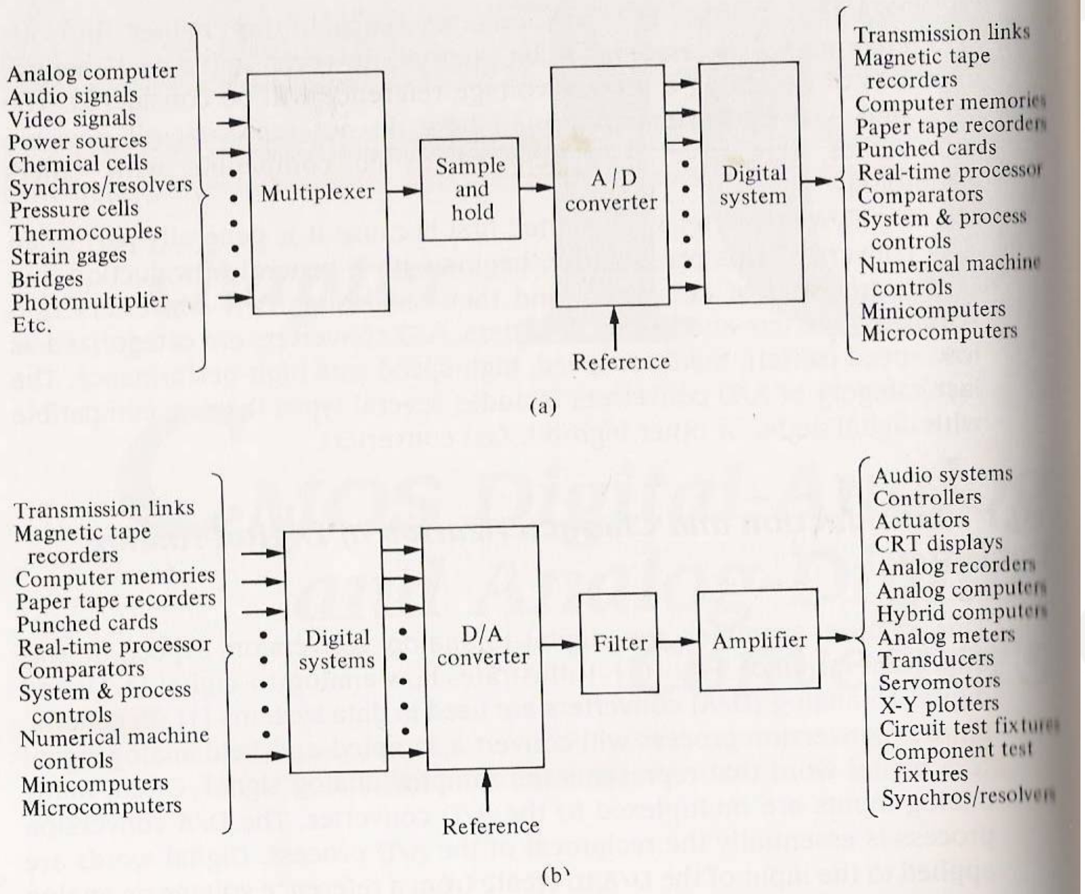
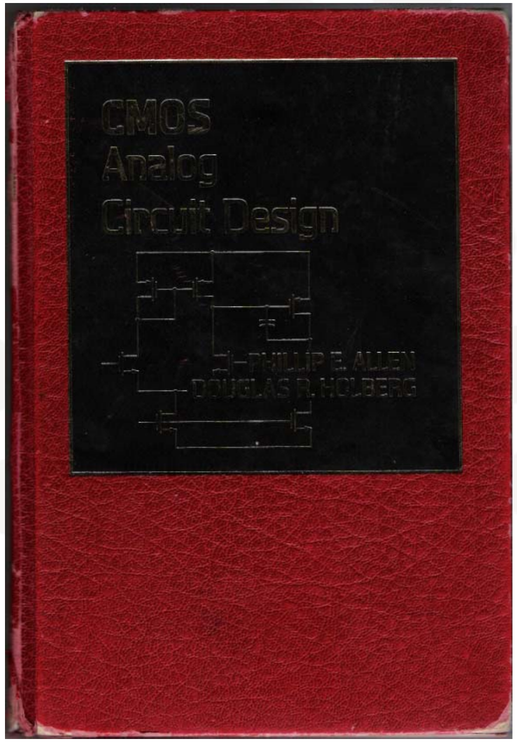
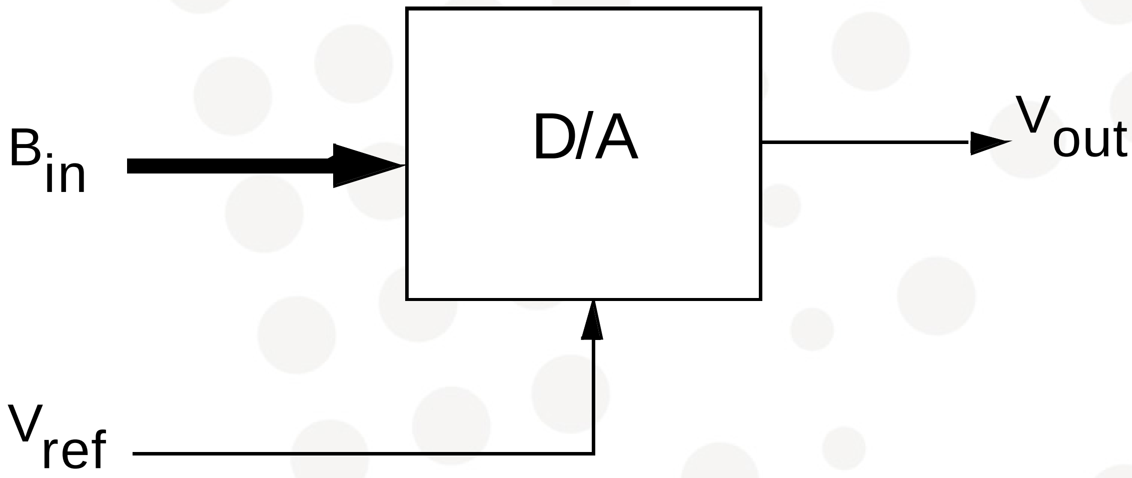


Figure 10.1-1 (a) A/D converters and (b) D/A converters in signal processing systems.



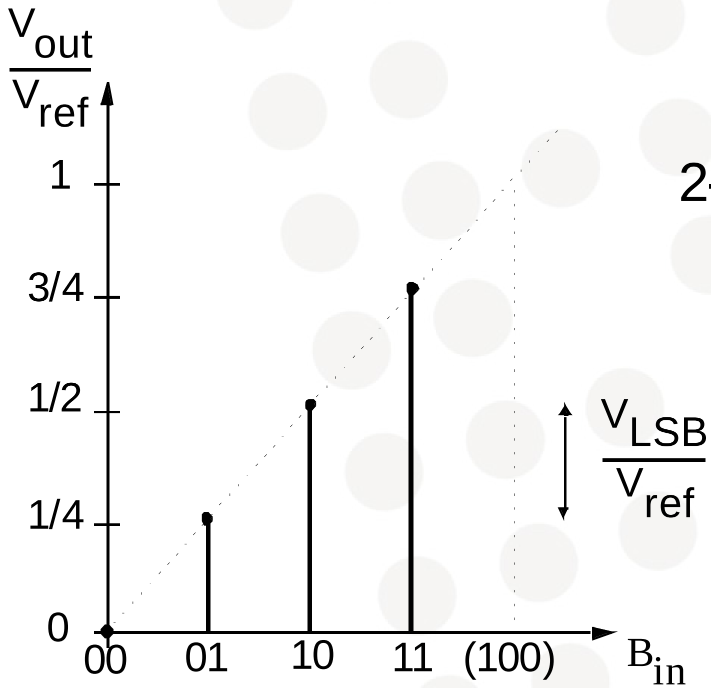
Ideal D/A converter



$$B_{in} = b_1 2^{-1} + b_2 2^{-2} + \ldots + b_N 2^{-N}$$

$$V_{out} = V_{ref}(b_1 2^{-1} + b_2 2^{-2} + \ldots + b_N 2^{-N})$$

Ideal D/A converter



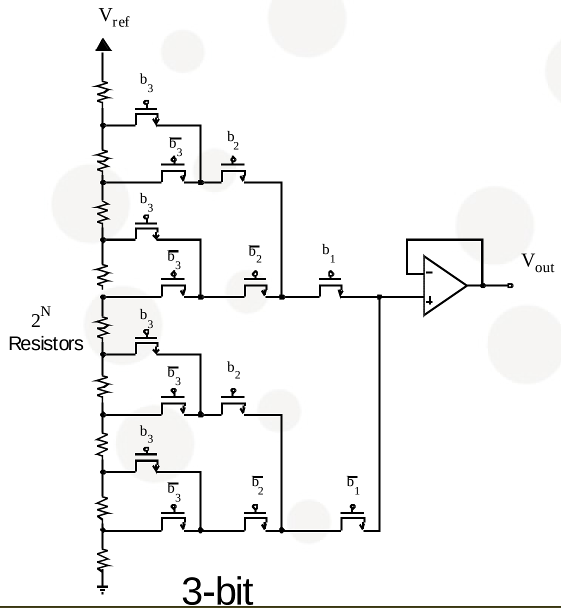
2-bit DAC

$$\frac{V_{LSB}}{V_{ref}} = \frac{1}{4} = 1\text{ LSB}$$

$$V_{LSB} \equiv \frac{V_{ref}}{2^N} \qquad 1\text{ LSB} = \frac{1}{2^N}$$

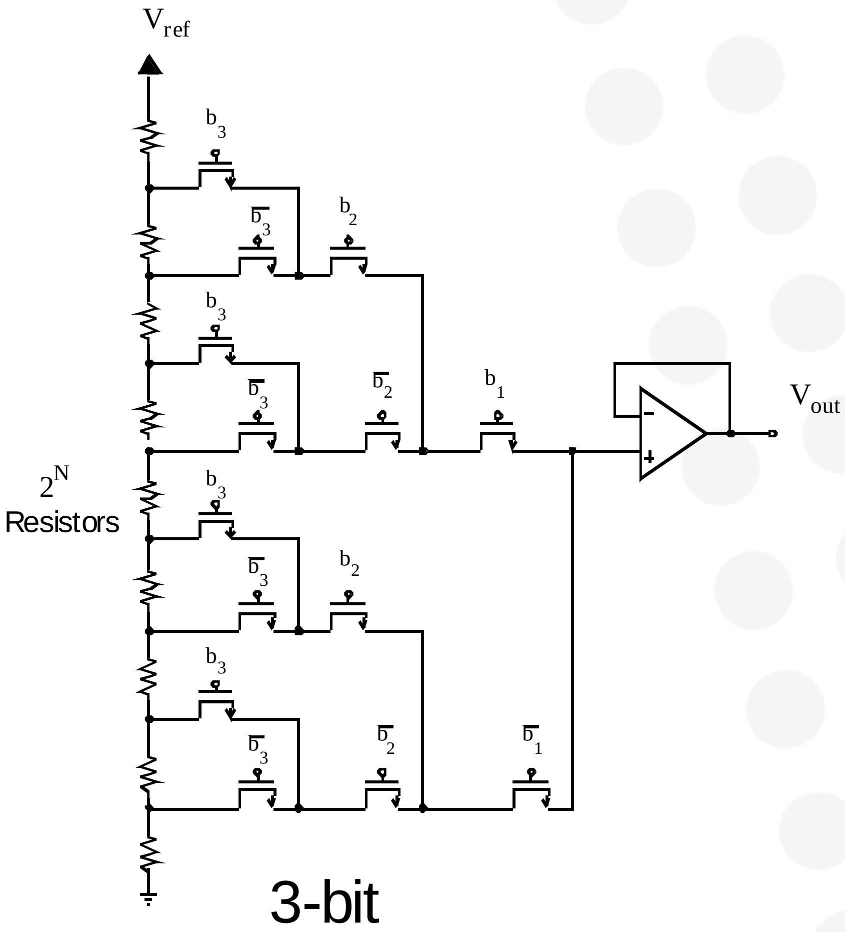
12.1 Decoder-Based Converters

- Creates 2^N reference signals and passes the appropriate signal to the output, depending on the digital input word.
- The switching network produces one, and only one, low impedance path between the resistor string and the input of the buffer
- Relatively compact switches if n-channel devices are used instead of transmission gates.



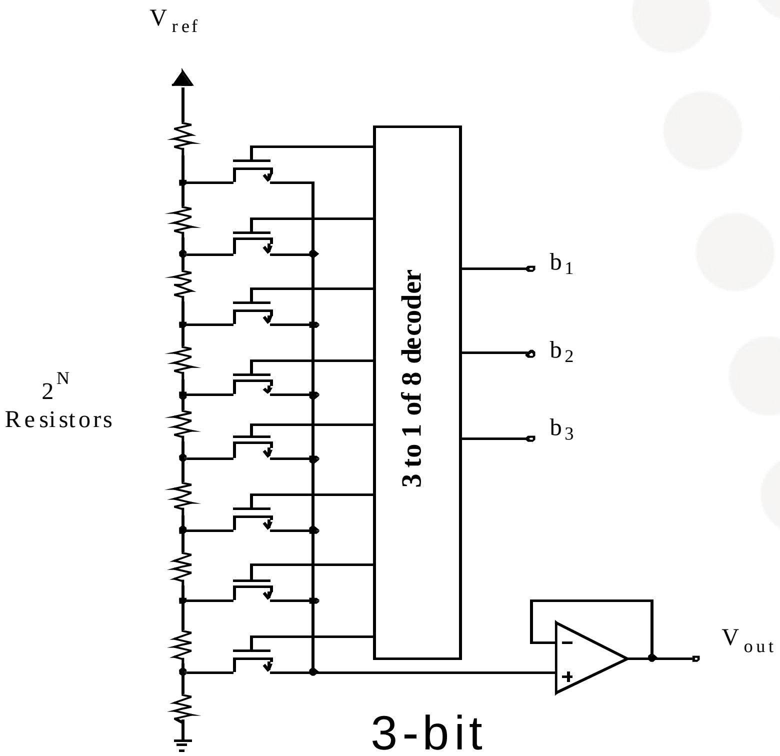
3-bit

Resistor String Converters (12.1)



- Only one path between resistor string and D/A-output
- Guaranteed monotonicity, provided that the voltage follower does not have too large offset
- Compact design when using only n-transistors (no contacts)
- Polysilicon resistors may give resolution up to 10 bit
- Delay through switch network is the major speed limitation of the circuit
- 2^N resistors are required (when only one resistor string is included)

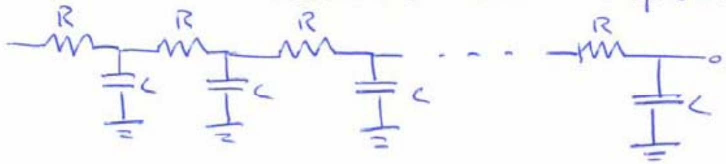
Resistor String Converters (12.1)



- High-speed implementation (when compared to the previous one), due to maximum of one switch in series →
- Less resistance through switches
- The switches are controlled by digital logic
- More area for the decoder compared to the previous DAC
- Larger capacitance on the buffer input, due to the 2^N transistors connected to it
- Pipelining may be applied for "moderate speed"
- 2^N resistors are required

Estimating the time constant for n resistors and capacitors in series (ex. 12.2)

Estimating the time constant for n resistors and capacitances in series (ex. 12.2)



$e^{-1} = 0.36$
$e^{-2} = 0.13$
$e^{-6} = 0.00248$
$e^{-7} = 0.000911$
≈ 0.001

time constant due to the first capacitor : RC
——— " ——— 2nd —— " —— : 2RC
——— " ——— nth —— " —— : nRC

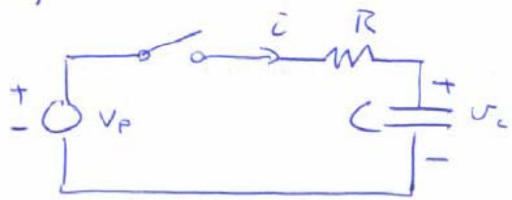
total : $\tau = RC + 2RC + \ldots + nRC = RC(1+2+\ldots+n)$

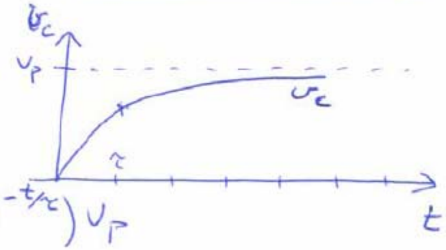
K. Rottman, s. 111:
("Formelsammlung")

$$\boxed{\sum_{x=1}^{x=n} x = \frac{n(n+1)}{2}}$$

$$\tau = RC\left[\frac{(n+1)n}{2}\right] \xrightarrow{\text{for large } n} \tau = RC\left(\frac{n^2}{2}\right)$$

n	1	5	10	50	100
$\frac{(n+1)n}{2}$	1	15	55	1275	5050
$\frac{n^2}{2}$	$\frac{1}{2}$	12.5	50	1250	5000

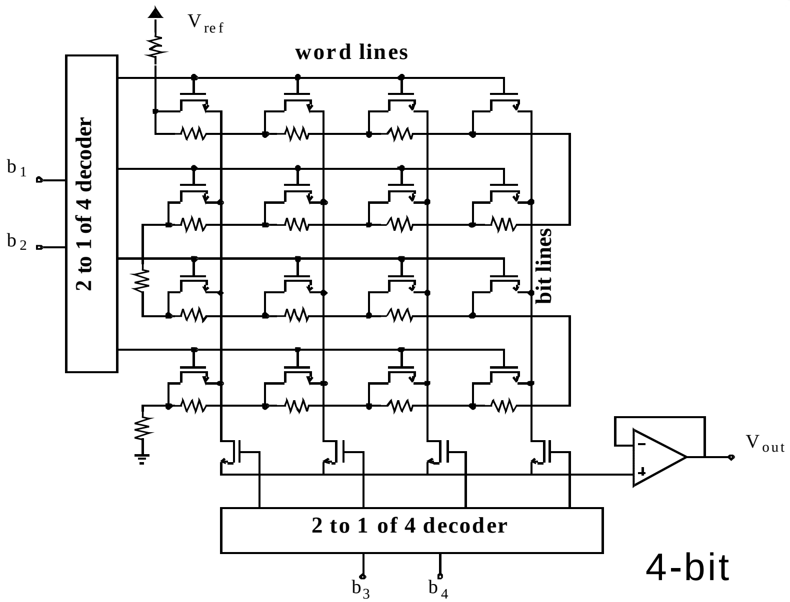




$V_{out} \cong (1 - e^{-t/\tau}) V_p$

$V_{out} = 0.999\, V_p$: about 7τ is needed

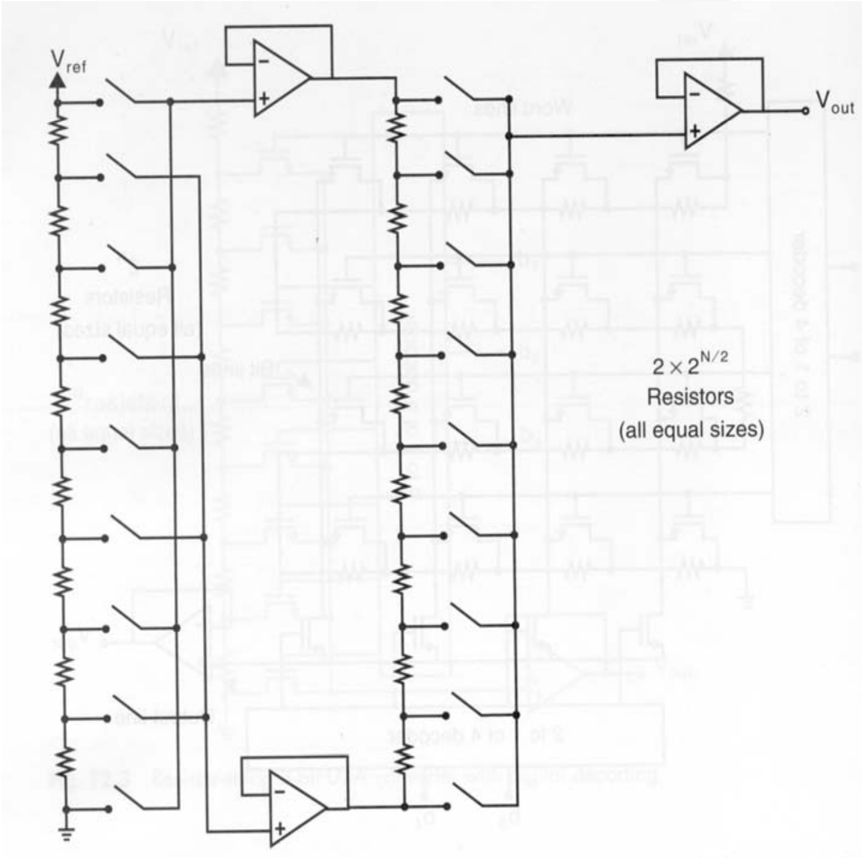
Folded Resistor-String Converters 12.1



4-bit

- Reduzing size of digital circuitry and capacitive loading
- 2^N resistors are required
- b1b2 : Most significant bits in the 4 bit case (selects one single word line.)
- Structure similar to what can be found in digital memories.
- OBS! NMOS switches here
- Number of transistor junctions connected to the output line is now 2 SQRT (2^N), instead of 2^N
- 4 bit case: 8 instead of 16
- 8 bit case: 32 instead of 256
- 10 bit case: 64 instead of 1024
- When a word line goes high, alle the bit lines must be pulled to new levels, limiting speed (no increase equal to the ratio ([2 SQRT (2^N)] / 2^N)

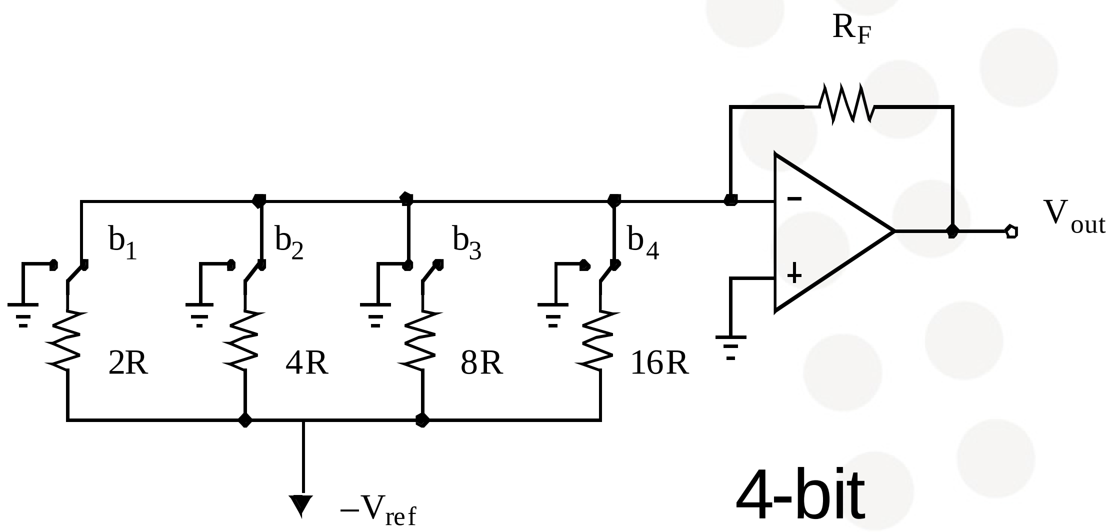
Multiple R-String Converters (12.1)



- A second tapped resistor string is connected between buffers whose inputs are two adjacent nodes of the first resistor string, as shown.
- In this 6-bit case the 3 MSBs determine the two adjacent nodes. The 2nd ("fine") string linearly interpolates between the two adjacent voltages from the first ("coarse") resistor string
- Additional logic needed to handle polarity switching, related to which intermediate buffer has the highest voltage on the input
- Guaranteed monotonicity assuming matched opamps and voltage insensitive offset voltages
- 2 x $2^{N/2}$ resistors are required
- Relaxed matching requirements for the 2nd resistor string.
- Ex.: 10 bit, 4 bits for the 1st string, matched to 0.1 %. Requirements for 2nd string? 2^4 x 0.1 % = 1.6 %

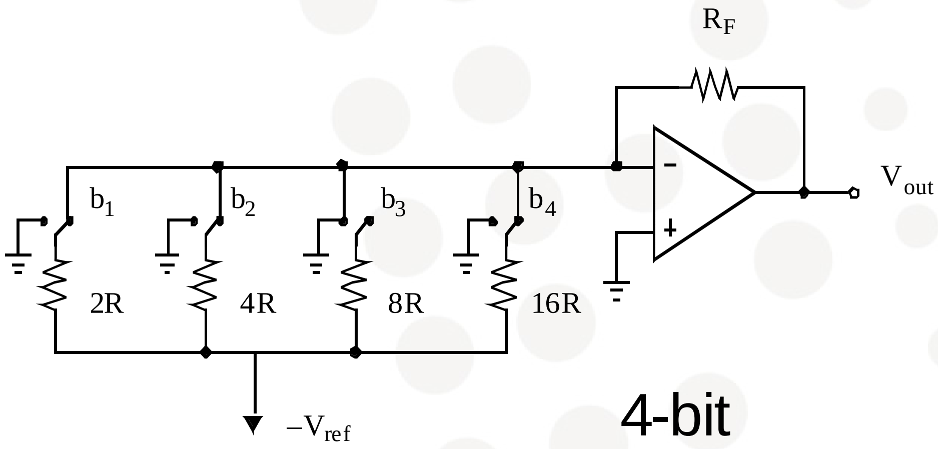
12.2 Binary-Scaled Converters

- Combining a set of signals that are related in a binary fashion
- Typically currents (resistors or plain current) or binary weighted arrays of charges
- Example: 4-bit binary-weighted resistor DAC:



4-bit

Binary-Weighted Resistor Converters (12.2)



4-bit

$$V_{out} = -R_F V_{ref}\left(-\frac{b_1}{2R} - \frac{b_2}{4R} - \frac{b_3}{8R} - \dots\right)$$

- Few switches and resistors
- Large resistor and current ratios (2^N)
- Monotonicity not guaranteed
- Prone to glitches for high-speed operation

Glitches –from Analog Digital Conversion Handbook

Glitch Impulse Area

Ideally, when a DAC output changes it should move from one value to its new one monotonically. In practice, the output is likely to overshoot, undershoot, or both (see Figure 2.94). This uncontrolled movement of the DAC output during a transition is known as a *glitch*. It can arise from two mechanisms: capacitive coupling of digital transitions to the analog output, and the effects of some switches in the DAC operating more quickly than others and producing temporary spurious outputs.

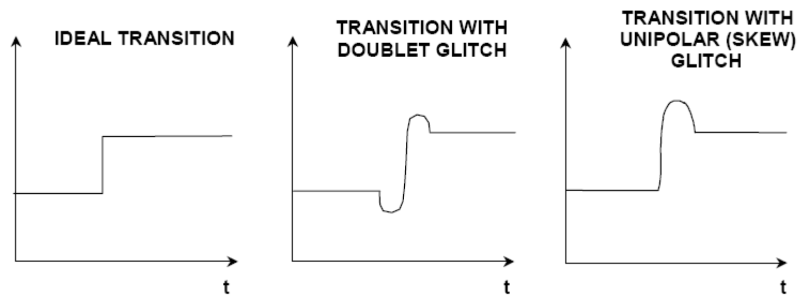


Figure 2.94: *DAC Transitions (Showing Glitch)*

Capacitive coupling frequently produces roughly equal positive and negative spikes (sometimes called a *doublet* glitch) which more or less cancel in the longer term. The glitch produced by switch timing differences is generally unipolar, much larger and of greater concern.

- Glitches waste energy and make noise

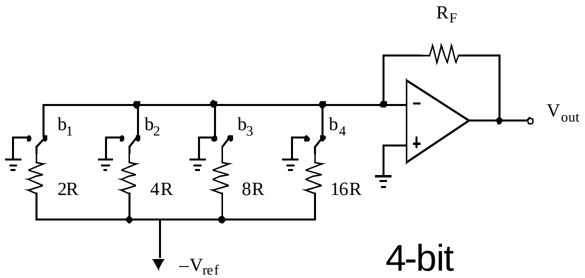
Glitches waste energy and produce noise

- Glitches can be seen as unwanted transitions on the output, instead of a monotonous move from one output value to the next
- Mainly the result of different delays occuring when switching different signals

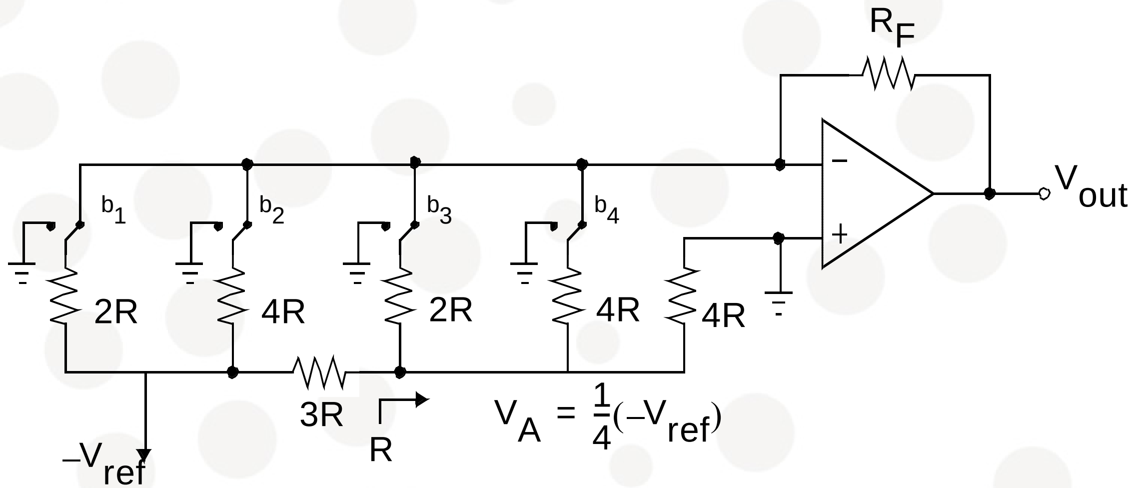
decimal	Binary b1b2b3	Thermometer code d1d2d3d4d5d6d7
0	000	0000000
1	001	0000001
2	010	0000011
3	011	0000111
4	100	0001111
5	101	0011111
6	110	0111111
7	111	1111111

- Potential cures:
- Exact matching in time (difficult)
- Reducing the bandwidth by placing C accross Rf in a circuit similar to the one in fig. 12.13
- Add S/H to the output
- Modify some or all of the digital word from binary to thermometer code (most popular)

Reduced-Resistance-Ratio Ladders (12.2)



4-bit



4-bit

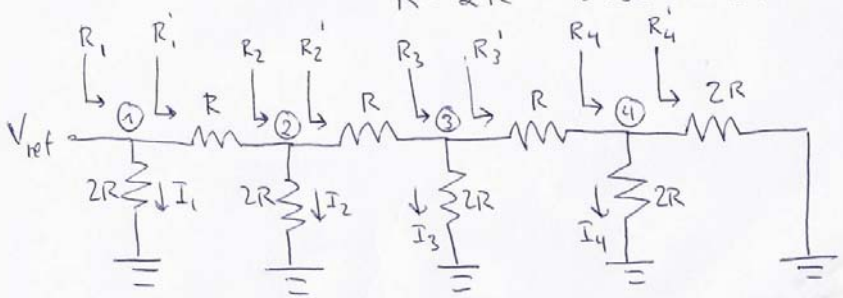
- Reducing the large resistor ratios (compared to Fig. 12.7, left) in a binary weighted array by introducing a series resistor (right).
- Same relationship to the digital binary signals as in the previous case, but with one-fourth the resistance ratio

  (4/2 - not 16/2)

  Somewhat similar to the R-2R ladder structure..

R-2R ladder

R–2R – based structure



$R_4' = 2R$

$R_4 = \frac{2R \cdot 2R}{2R+2R} = \frac{4R^{\cancel{2}}}{4\cancel{R}} = R$

$R_3' = R + R_4 = R + R = 2R$

$R_3 = 2R \,||\, R_3' = \frac{2R \cdot 2R}{4R} = R$

$R_2' = R + R_3 = R + R = 2R$

$R_2 = 2R \,||\, R_2' = R$

$R_1' = R + R_2 = R + R = 2R$

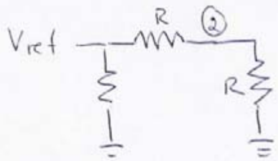
$R_1 = 2R \,||\, R_1' = R$

$\underline{R_i' = 2R \text{ for all } i}$

Therefore :

$I_1 = \frac{V_{ref}}{2R}$

From ② :



The voltage at node ② is half of the voltage at ① :

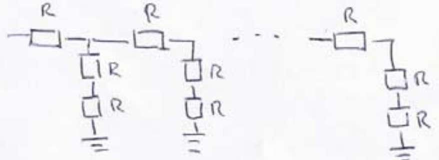
$I_2 = \frac{V_2}{2R} = \frac{\frac{1}{2} V_{ref}}{2R} = \frac{V_{ref}}{4}$

→ $V_③ = \frac{V_②}{2}$

$\boxed{\begin{array}{l} U = RI \\ I = \frac{U}{R} \end{array}}$

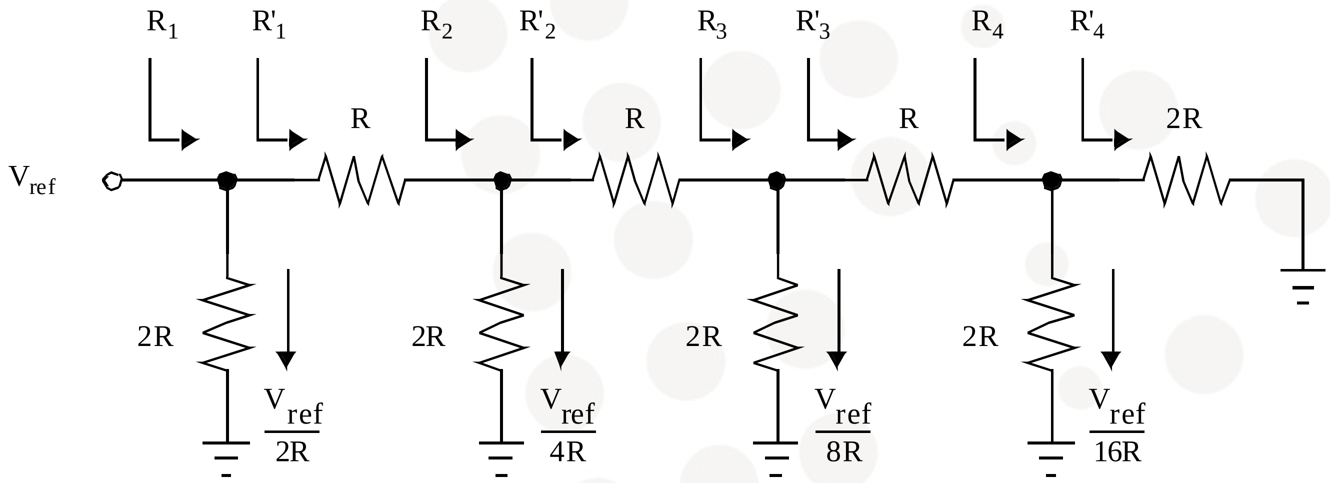
$I_3 = \frac{\frac{V_2}{2}}{2R} = \frac{\frac{1}{2} \cdot \frac{1}{2} \cdot V_{ref}}{2R} = \frac{V_{ref}}{8R}$

And so on..



Resistors of size 2R are made from size R resistors to improve matching.

R-2R-Based Converters (12.2)



- Only two resistor values
- Improved matching
- → smaller size and better accuracy

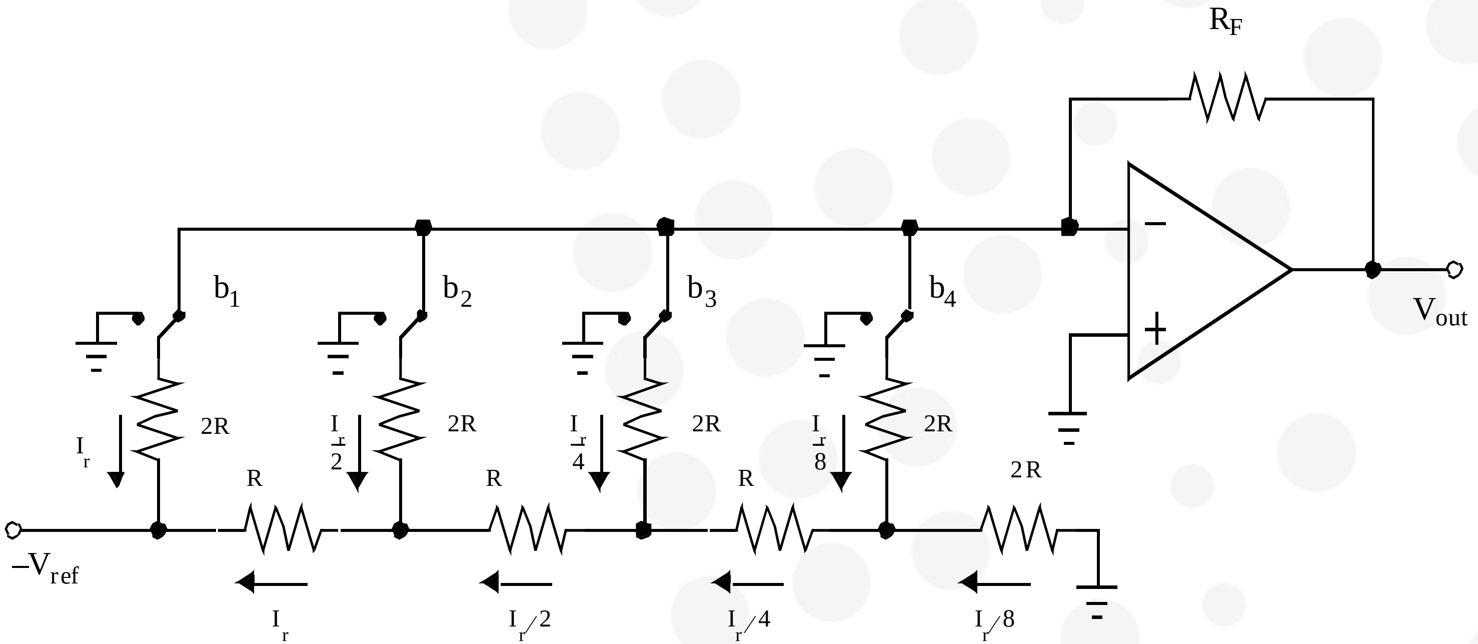
$$R'_4 = 2R$$

$$R_4 = 2R \parallel 2R = R$$

$$R'_3 = R + R_4 = 2R$$

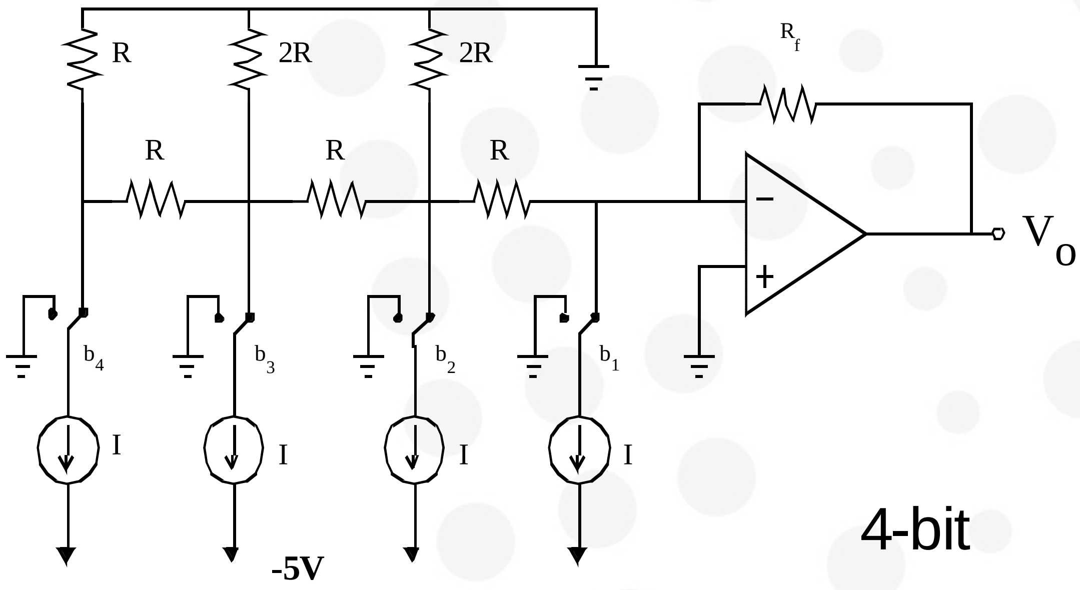
$$R_3 = 2R \parallel R'_3 = R$$

4-bit R-2R Resistor Ladder (12.2)



- The current is scaled by controlling the switches
- Important to scale the switches accordingly
  - Ensuring equal voltage drop across the switches
- Suited for fast operation
  - V_{out} is the only changing voltage

R-2R Resistor Ladder with equal current through all switches
(12.2)



- Not necessary to scale switch sizes (Equal current)
- Slower due to changing node voltages

Binary weighted current mode DAC (12.2)(fig. 12.13)

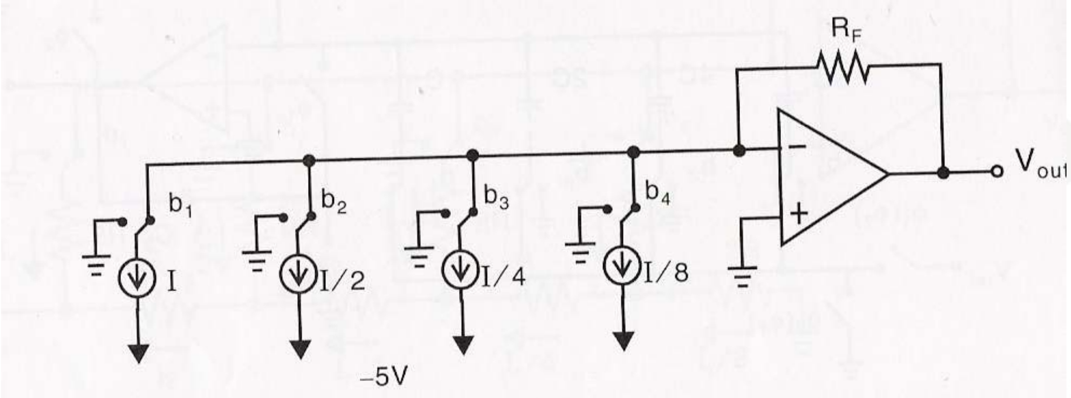


Fig. 12.13 Binary-weighted current-mode D/A converter.

- Current-mode DACs are very similar to resistor-based converters, but intended for higher speed applications
- The output current is converted to a voltage through the use of R_F

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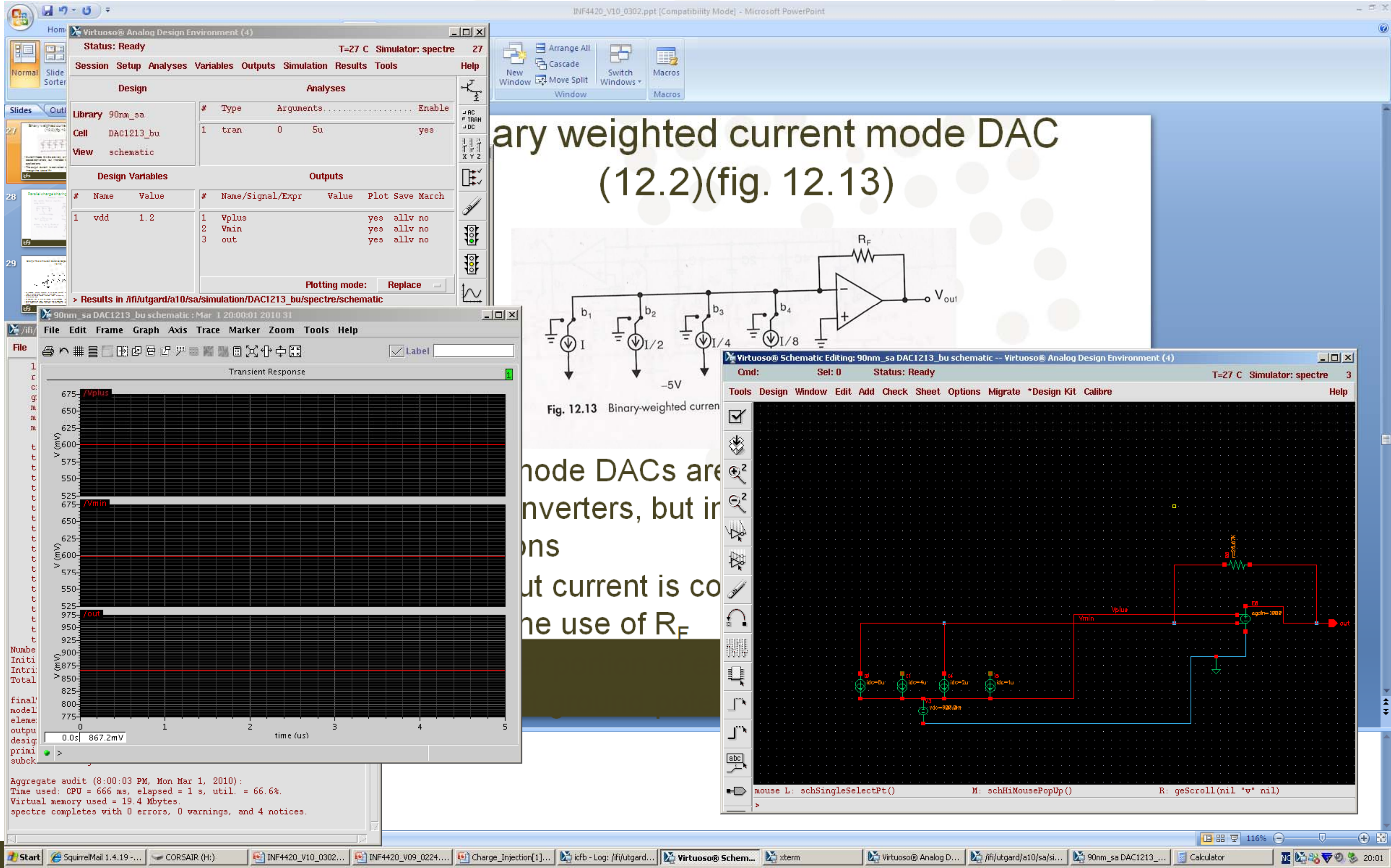
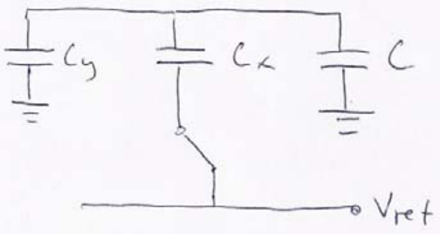


ary weighted current mode DAC
(12.2)(fig. 12.13)
Fig. 12.13 Binary-weighted curren
node DACs are
nverters, but ir
ons
ut current is co
he use of R_F
Virtuoso® Analog Design Environment (4)
Status: Ready
T=27 C Simulator: spectre
Session Setup Analyses Variables Outputs Simulation Results Tools Help
Design
Library 90nm_sa
Cell DAC1213_bu
View schematic
Analyses
1 tran 0 5u yes
Design Variables
1 vdd 1.2
Outputs
1 Vplus yes allv no
2 Vmin yes allv no
3 out yes allv no
Plotting mode: Replace
> Results in /ifi/utgard/a10/sa/simulation/DAC1213_bu/spectre/schematic
Transient Response
time (us)
Virtuoso® Schematic Editing: 90nm_sa DAC1213_bu schematic -- Virtuoso® Analog Design Environment (4)
Cmd: Sel: 0 Status: Ready
Tools Design Window Edit Add Check Sheet Options Migrate *Design Kit Calibre Help
mouse L: schSingleSelectPt() M: schHiMousePopUp() R: geScroll(nil "w" nil)
Aggregate audit (8:00:03 PM, Mon Mar 1, 2010):
Time used: CPU = 666 ms, elapsed = 1 s, util. = 66.6%.
Virtual memory used = 19.4 Mbytes.
spectre completes with 0 errors, 0 warnings, and 4 notices.

Parallel charge sharing DAC principle

PARALLEL CHARGE SCALING DAC

DAC operation based on capacitive voltage division

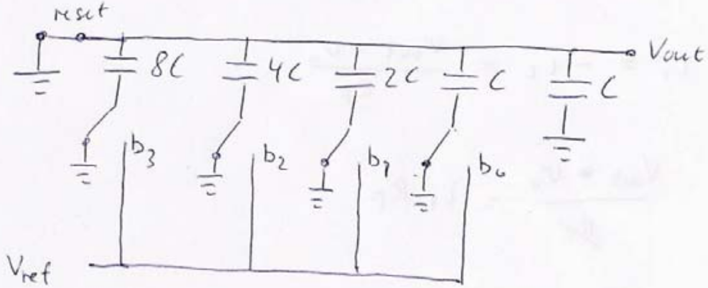


$$V_{out} = \frac{C_x}{C_x + C_y + C} V_{ref}$$

→ Make C_x & C_y function of incoming DAC digital word

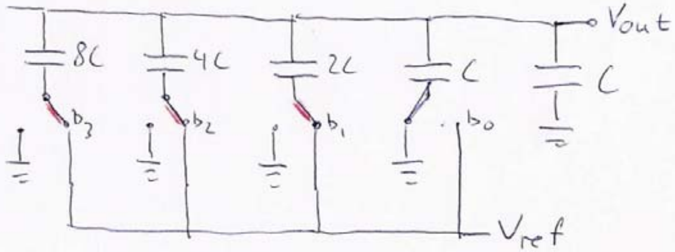
Example: 4-bit DAC, Charge Scaling

Reset phase:



Charge-phase:

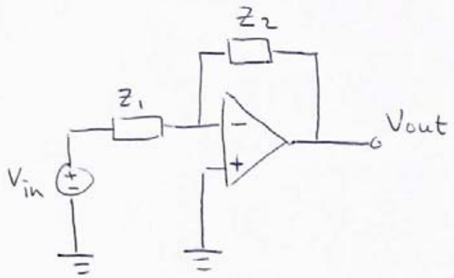
Input-code 1110:



$$V_{out} = \frac{2^1 \cdot C + 2^2 \cdot C + 2^3 \cdot C}{2^4 C} V_{ref} = \frac{(2+4+8)\cdot C}{16C} \cdot V_{ref}$$

Capacitance ratios defining voltage gain

SWITCHED CAPACITOR GAIN STAGES

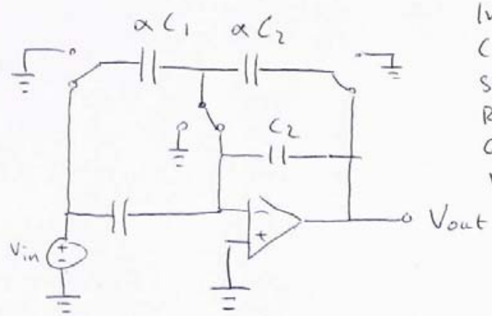


One of the most common functions in analog signal processing is voltage amplification, as shown left (most often used way..)

The input-output relation:

$$\frac{V_{out}}{V_{in}} = -\frac{Z_2}{Z_1}$$

If $Z_2 = k \cdot Z_1$, where k is a constant, a (fixed) gain is achieved.



"Analog MOS Integrated Circuits for Signal processing" R. Gregorian, Gabor C. Temes, Wiley 1986, page 413

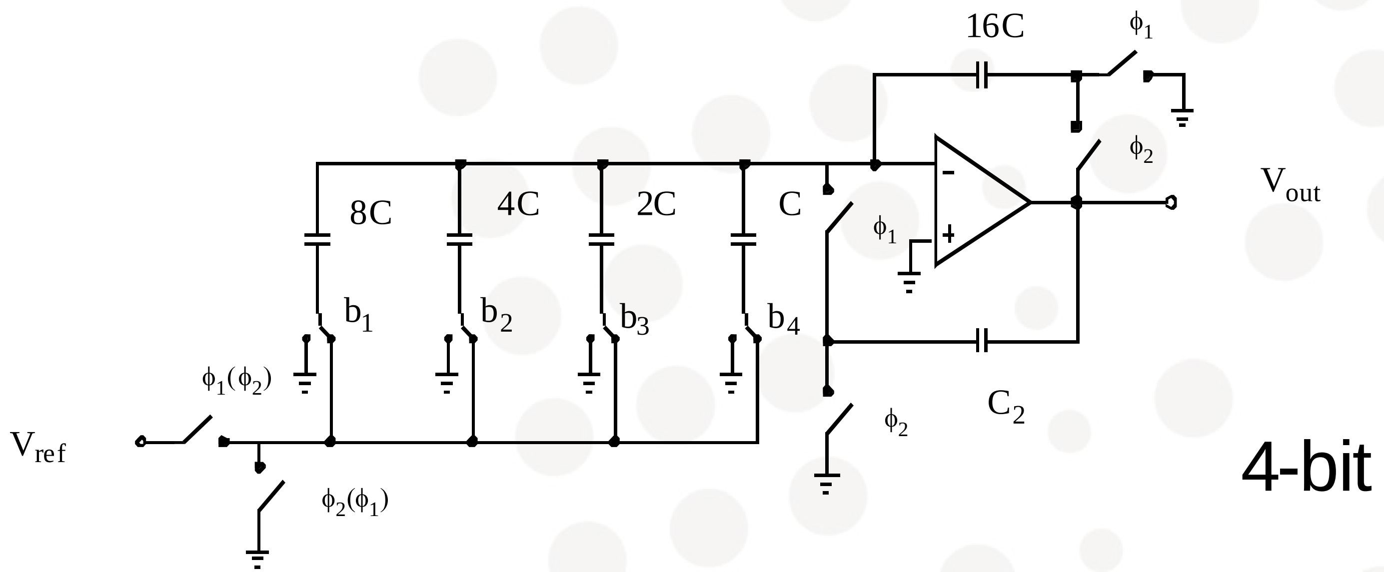
SC voltage amplifier

$$H(z) = \frac{V_{out}(z)}{V_{in}(z)} = -\frac{C_1}{C_2}$$

H(z) is a frequency independent constant.

By switching in different C, the voltage gain may change, depending on dig. input

Charge-Redistribution Switched Capacitor Converter (12.2) (fig. 12.12)



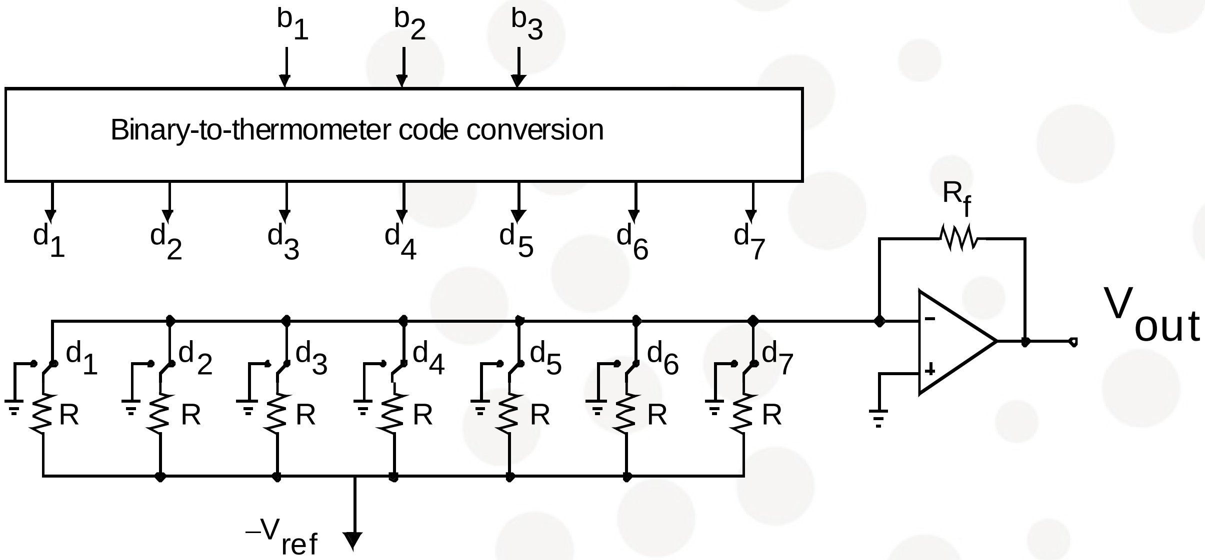
- By replacing the input capacitor of an SC gain amplifier by a programmable capacitor array (PCA) a charge based converter is obtained
- Employs correlated double sampling (CDS) – insensitive to 1/f noise, input-offset voltage and finite amplifier gain.
- An additional sign bit may be realized by interchanging the clock phases
- Carefully generated clock waveforms and a deglitching capacitor are required
- Digital codes must change only when the input-side of the capacitors are connected to ground

Thermometer-Code Converters (Chapter 12.3)- number of 1s represents the decimal value

- + compared to binary counterpart:
- Lower DNL errors
- Reduced glitching noise
- Guaranteed monotonicity
- - compared to binary counterp.:
- Need $2^N - 1$ digital inputs to represent 2^N input values

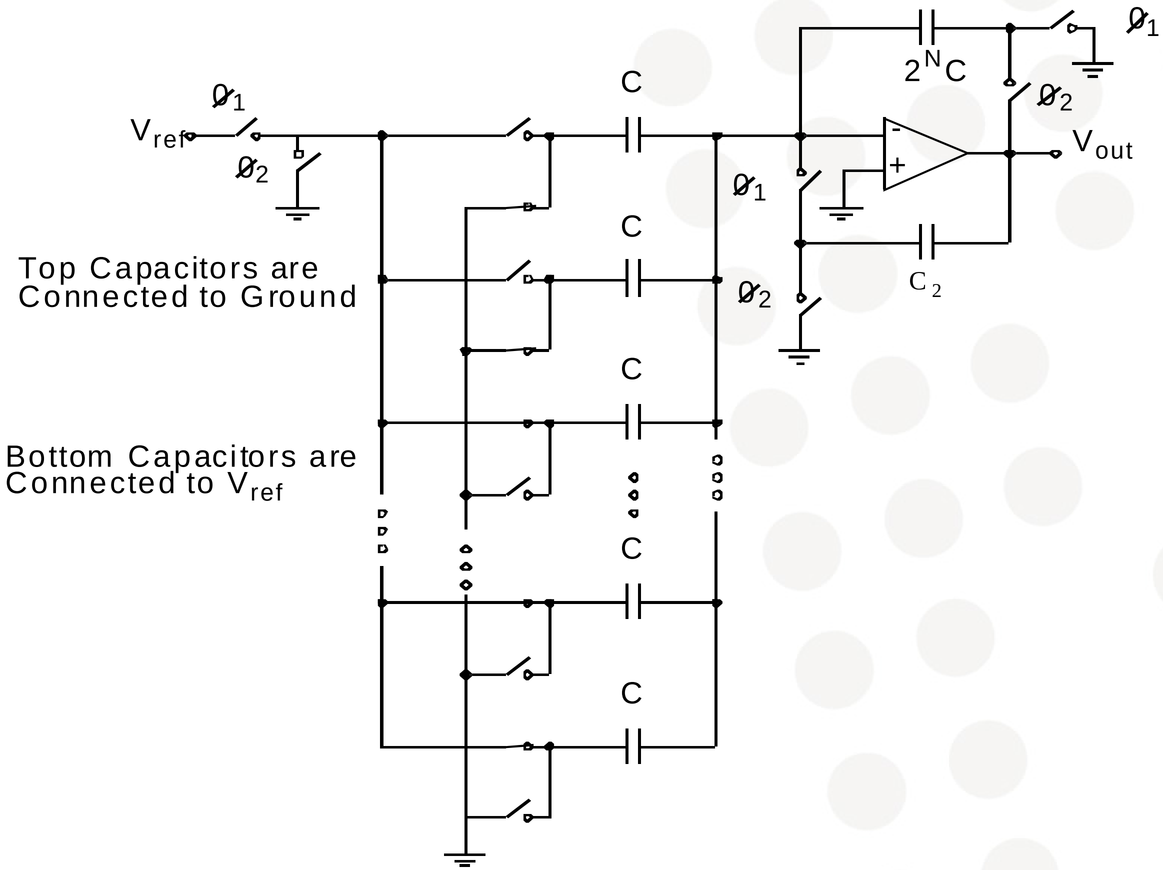
decimal	Binary b1b2b3	Thermometer code d1d2d3d4d5d6d7
0	000	0000000
1	001	0000001
2	010	0000011
3	011	0000111
4	100	0001111
5	101	0011111
6	110	0111111
7	111	1111111

Thermometer Based 3-bit DAC (12.3)



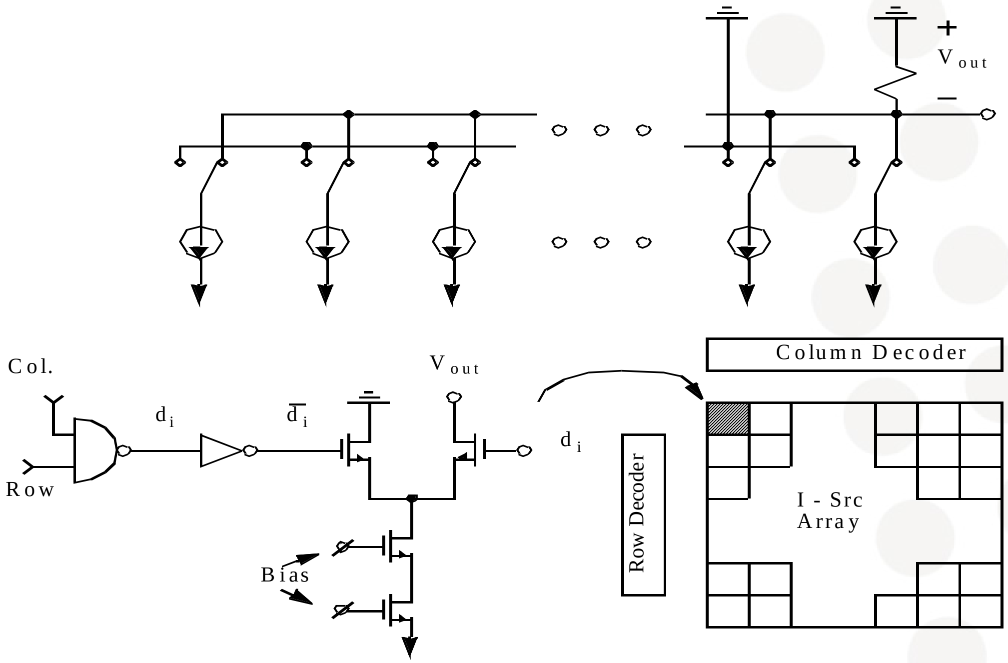
- Equal resistor sizes
- Equal switch sizes
- 2^N resistors required

Thermometer-Code Charge-Redistribution DAC (12.3) (Fig. 12.16)



- 2^N capacitors required

Thermometer-code Current-Mode D/A-Converter (12.3)



- Thermometer-code decoder in both row and column, for inherent monotonicity and good DNL
- Current is switched to the output when both row and column lines for a cell are high
- Cascode current source used for improved current matching
- Suited for high speed, with output fed directly into a resistor (50 or 75 Ohms), instead of an output opamp.
- The delay to all switches must be equal (suppress glitching)
- Important that the edges of d_i and d_i’ are synchronized

Thermometer-code Current-Mode DAC - example

IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. SC-21, NO. 6, DECEMBER 1986

An 80-MHz 8-bit CMOS D/A Converter

TAKAHIRO MIKI, YASUYUKI NAKAMURA, MASAO NAKAYA, SOTOJU ASAI, YOICHI AKASAKA, AND YASUTAKA HORIBA

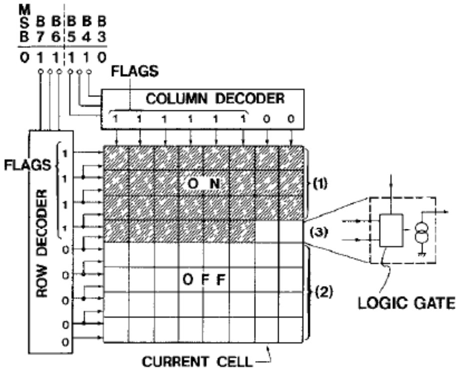


Fig. 2. Two-step decoding.

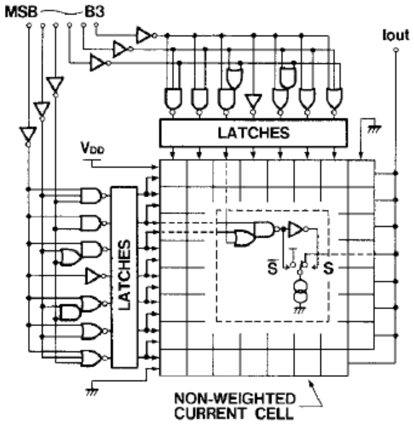


Fig. 3. High-speed decoding circuit.

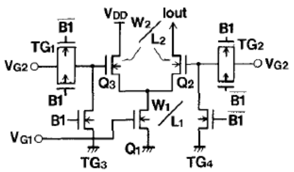


Fig. 4. Circuit diagram of the LSB current source.

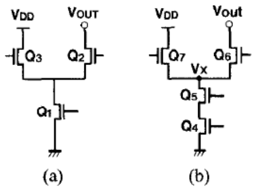


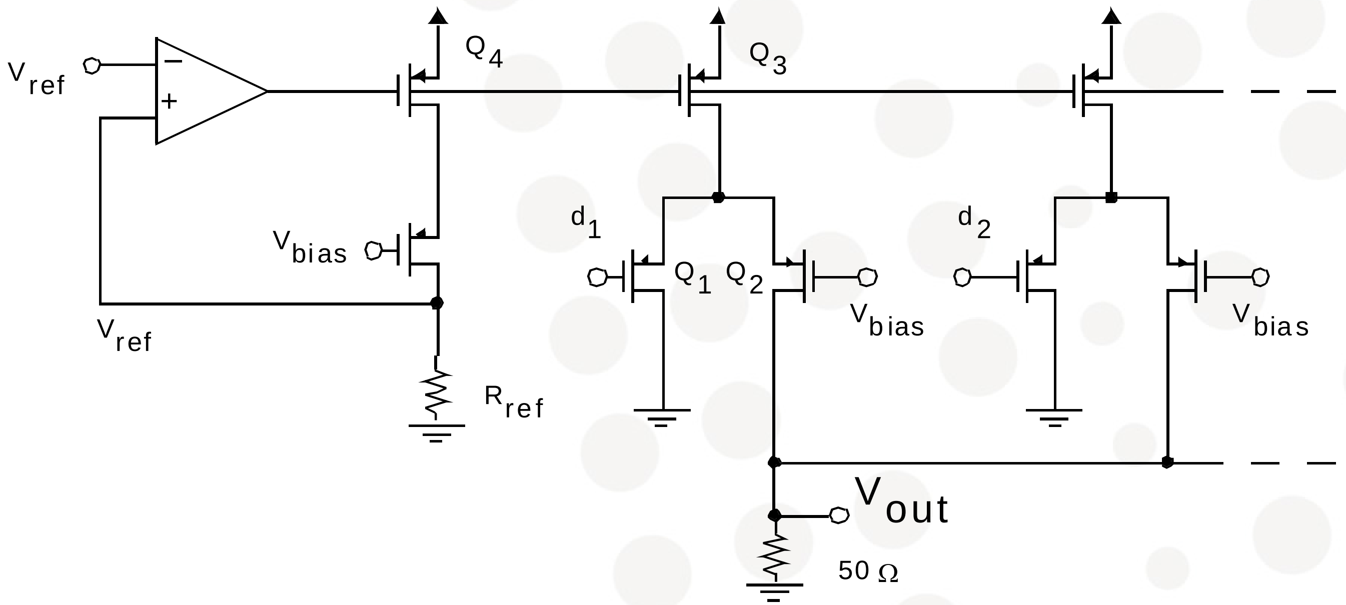
Fig. 5. Configuration of current source. (a) Single-transistor configuration. (b) Cascode configuration.

- Cascode current sources
- Latches connected to decoding
- One gate in the differential pair may be put to a dc level, to improve speed.

TABLE I
CHARACTERISTICS OF THE DAC

Resolution	8 bit
Settling Time	12.5 ns
Rise/Fall Time	5.5 ns
Integral Linearity Error (DC)	0.38 LSB (Typ.)
Differential Linearity Error (DC)	0.22 LSB (Typ.)
Glitch Energy	100 ps·V
Power Consumption	145 mW
Chip Size	1.85 mm x 2.05 mm

Single-Supply Positive-Output Converters



- For fast single-supply positive-output
- ***One side of each current-steering pair connected to V_{bias}, rather than the inversion of the bit signal***, to maintain current matching. When the current is steered to the output through Q2, the drain-source voltage across the current source, Q3, remains mostly constant if V_{out} stays close to zero, such that Q2 remains in the active region.
- Thus, Q2 and Q3 effectively form a cascode current source when driving current to the output.
- Does not need d_i and $d_{i'}$; reduces complexity and removes the need for precisely timed edges to avoid glitches.

Dynamically Matched Current Sources (12.3)

- for high resolution

IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. 23, NO. 6, DECEMBER 1988

A Low-Power Stereo 16-bit CMOS D/A Converter for Digital Audio

HANS J. SCHOUWENAARS, SENIOR MEMBER, IEEE, D. WOUTER J. GROENEVELD, AND HENK A. H. TERMEER

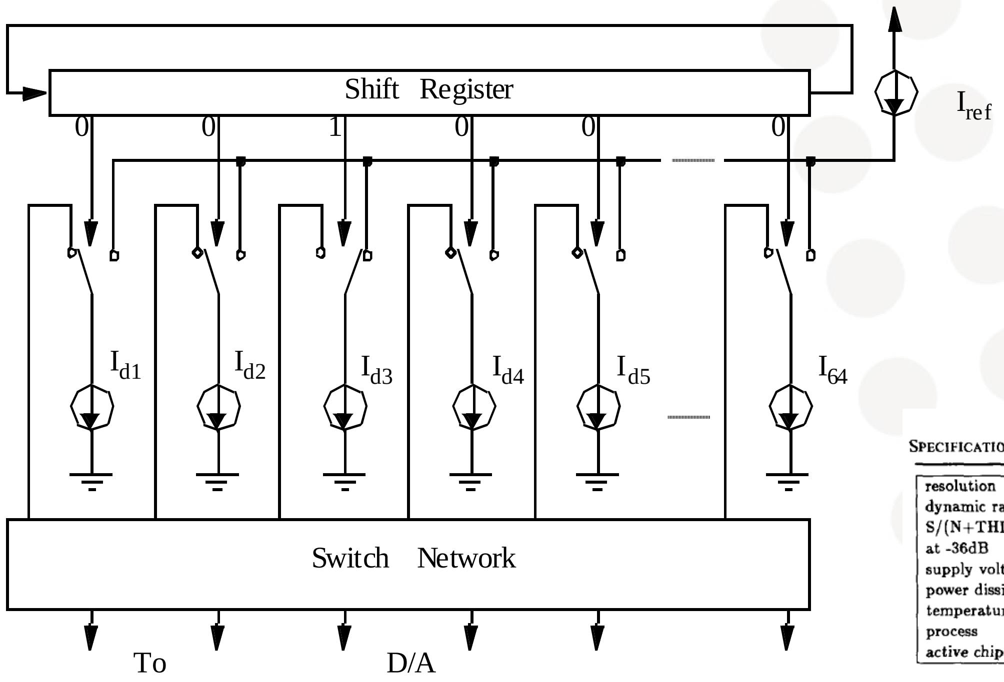
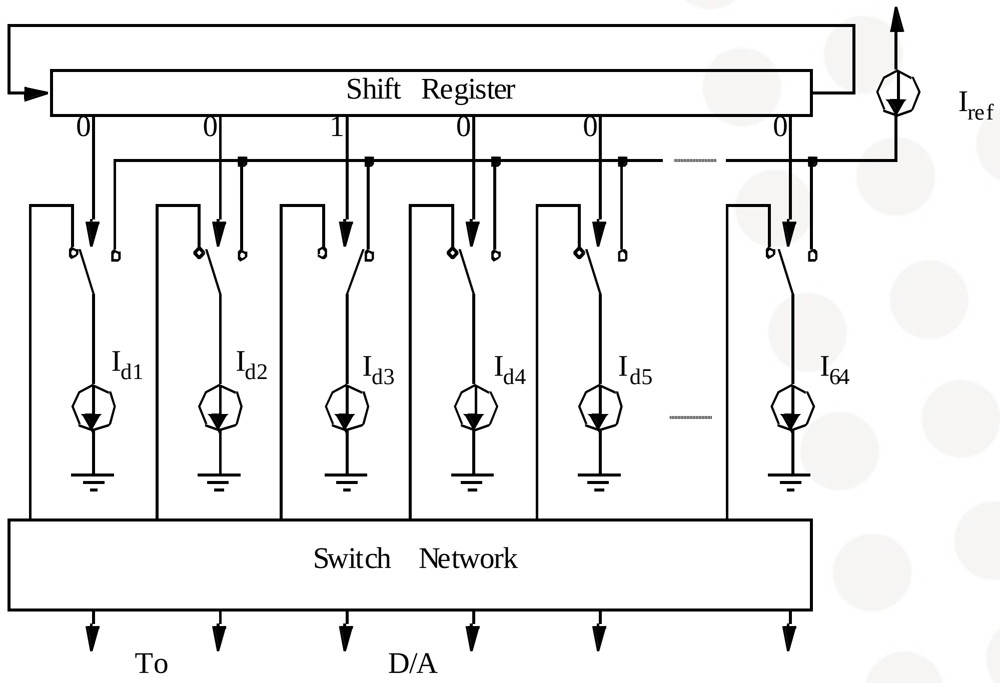


TABLE II
SPECIFICATIONS OF THE D/A CONVERTER

resolution	16 bit
dynamic range	95 dB
S/(N+THD) at 0dB	79 dB
at -36dB	59 dB
supply voltage range	2.5 to 5 V
power dissipation	15 mW at 5 V
temperature range	-20 to 85° C
process	2μm CMOS
active chip area	5 mm²

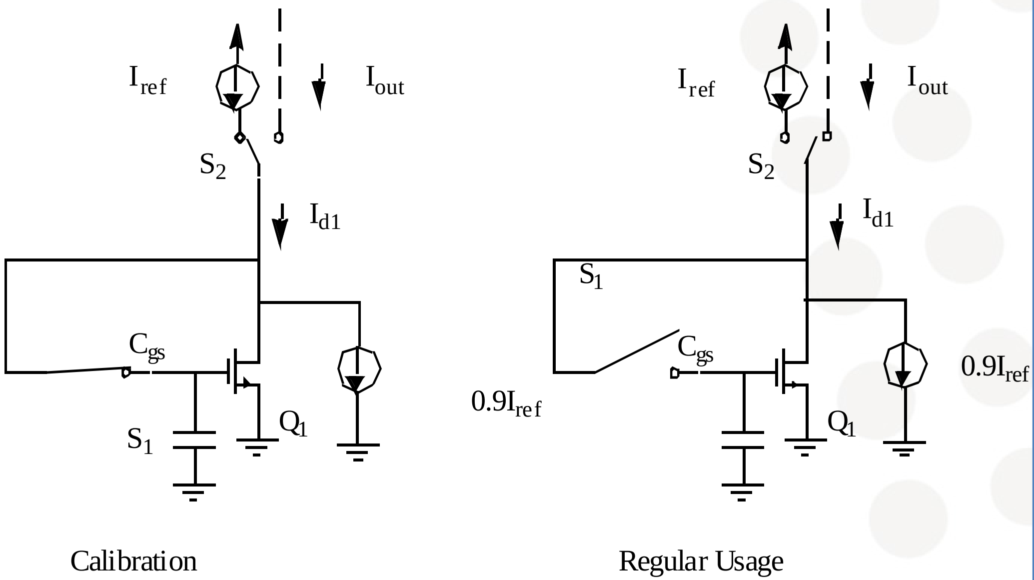
- Current sources are periodically being regulated to ideally the same value (matched) during normal operation, to ensure proper resolution.
- A "once and for all" matching of each current source is not enough due to mechanisms including temperature drift and gate leakage.

Dynamically Matched Current Sources
(12.3)



- 6 MSB realized using a thermometer code. (binary array for the remaining bits)
- All currents are matched against $I_{ref,}$ one after one, to get the same precise value on all Idi.
- One extra current source is included to provide continous operation, even when one of the sources is being calibrated.

Dynamic matched current sources – method for calibration



- I_{di} is connected to I_{ref} during calibration. This places whatever voltage is necessary across the parasitic C_{gs} so that I_{di} equals I_{ref} . When S_i is opened Idi remains nearly equal to I_{ref}.
- Major limitation in matching the 64 current sources is due to differences in clock feedthrough and charge injection of the switches S_i. → have relatively large C_{gs} and V_{gs} (large V_{gs} so that a certain voltage difference will cause a smaller current deviation.)
- Using $0.9I_{ref}$ in parallell makes Q_1 need only to source a current near 0.1 I_{ref}. With such an arrangement a large low-transconductance device can be used (ex.: W/L=1/8)

12.4 Hybrid Converters

- Combination of different techniques, like for example decoder based, binary scaled, and thermometer-code converters
- Hybrid converters combine the advantages of different approaches for better performance
- Example: Thermometer code used for MSBs, while using a binary-scaled technique for the lower LSBs to reduce glitching. Using binary scaled for the LSBs, where glitching requirements are reduced, may save valuable chip area.

Resistor-Capacitor Hybrid Converters (12.4)

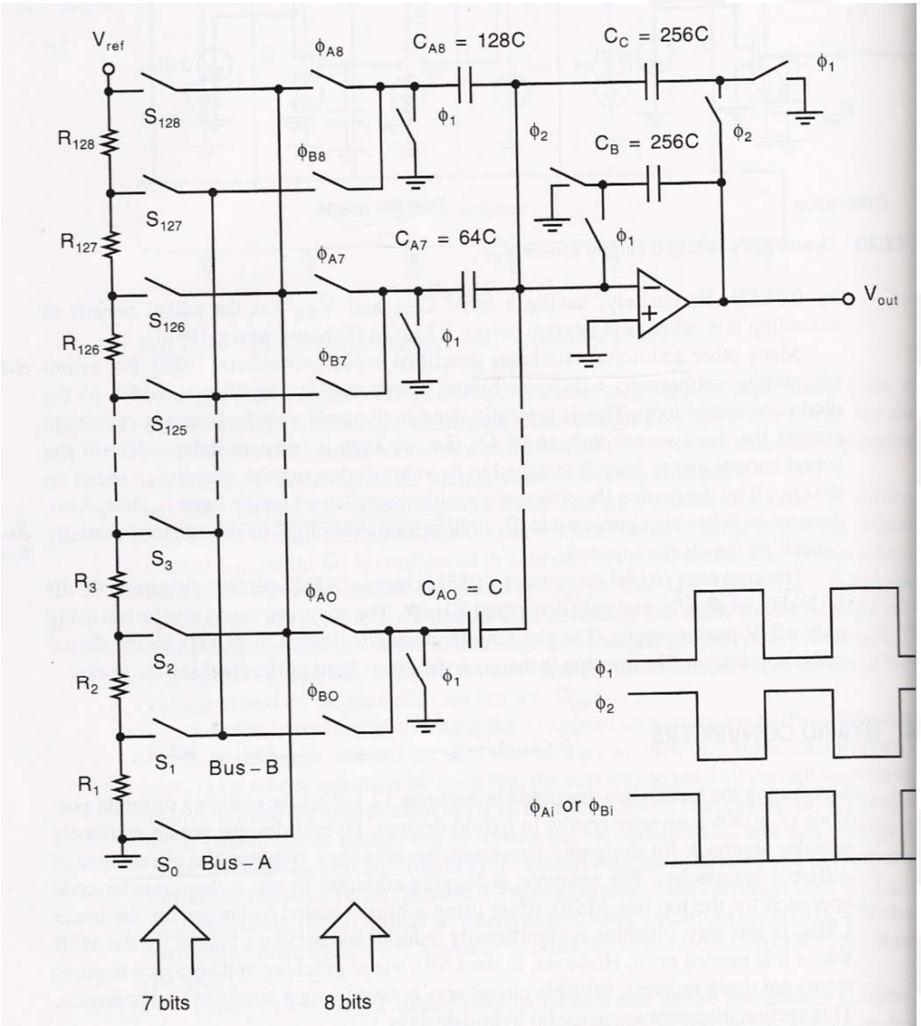


Fig. 12.21 One example of a 15-bit resistor-capacitor hybrid D/A converter.

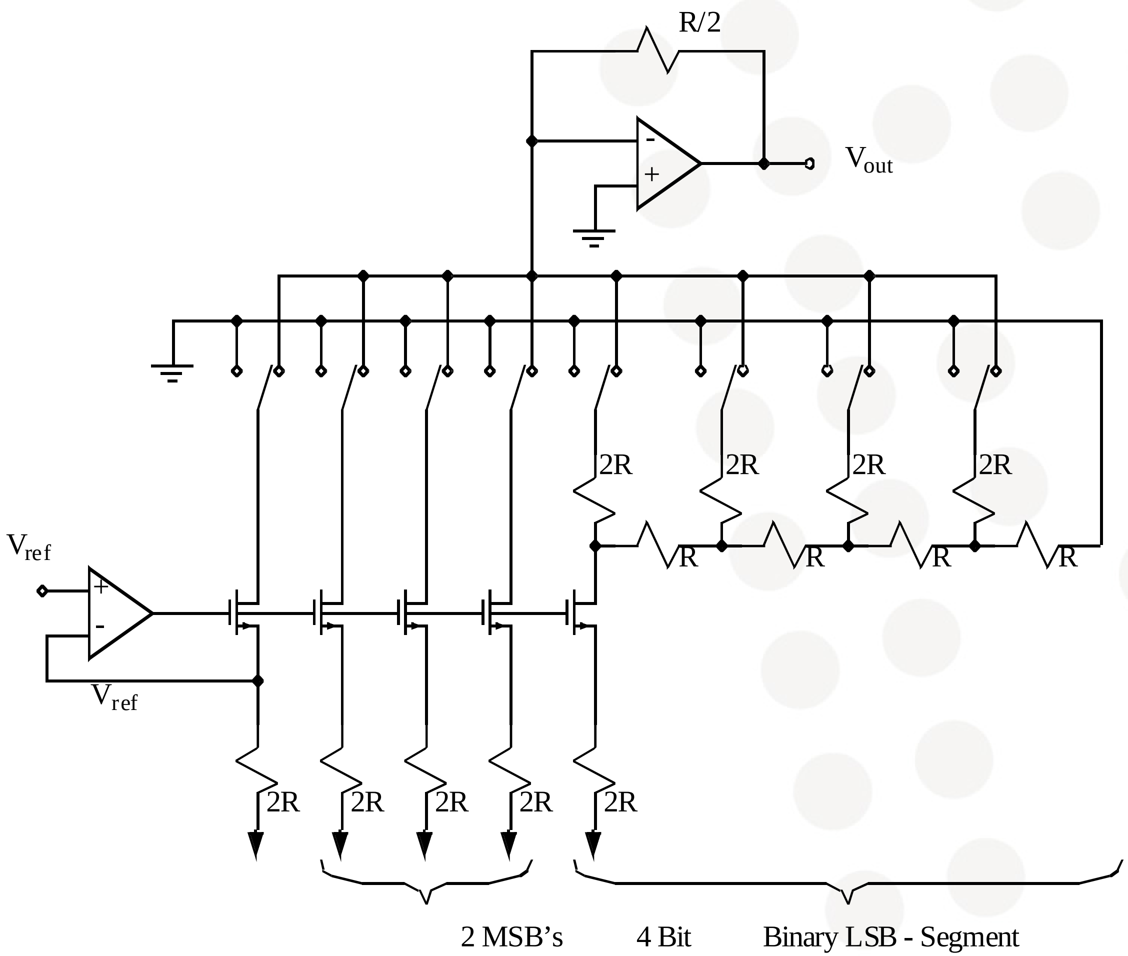
- Top 7 MSBs determine which pair of voltages across a single resistor is passed on to the 8-bit capacitor array.
- A 7-bit resistor-sting DAC is combined with an 8-bit SC binary-weighted DAC for a 15-bit converter
- 15-bit monotonicity, without trimming

High-Resolution Low-Power CMOS D/A Converter

JOHN W. YANG AND KENNETH W. MARTIN, SENIOR MEMBER, IEEE

Abstract —A very low-power, high-resolution, medium-speed D/A converter is described. The converter was realized using a standard analog CMOS technology. It achieved 15-bit monotonicity and less than 0.07-percent overall linearity at a clock frequency of 100 kHz, without requiring any trimming or calibration. The measured SNR was 85 dB, the power dissipation was less than 10 mW, and the distortion for a sinusoidal output was less than 0.04 percent. The D/A converter is intended for battery-powered speech and music synthesis applications where high dynamic range, low power, and low cost are all important.

Segmented Converters (12.4)



-

- Combination of thermometer- and binary
- 2 MSB's are thermometer (reduces glitches)
- 4 LSB's are binary
- High bits switched to the output, low bits to ground

A few published DACs

Publication year	SFDR @Nyquist [dB]	ENOB @ Nyquist	Nyquist update rate, [Ms/s]	Power consumpt. [mW]	Area [mm²]	Supply voltage [V]	Technology [nm]	other	Reference
2009	>60dB	9.7	1000	188			65	Current steering	Lin et al., ISSCC '09
2008	80	12.9	11	119	0.8	1.8	180	"current steering"	Radulov, APPCAS '08
2007	59	9.5	200 @3.3 V	56	2.25	3.3	180	"current steering"	Mercer, JSCC, Aug.'07
2004	40	6	250	23	0.14	1.8	180	"binary weighted"	Deveugele, JSCC, July '04
2001	61	9.84	1000	110	0.35	3.0	350	"current steering"	Van den Bosch, JSCC, Mar.'01
1988	95	15.45	0.044	15	5	2.5-5	2000		Schouwenaars, JSCC, Dec. '88

Next Tuesday (9/3-08):

- Chapter 13 Nyquist Analog-to-Digital Converters

Additional litterature

- Phillip E. Allen, Douglas R. Holberg: CMOS Analog Circuit Design, Holt Rinehart Winston, 1987.
- R. Gregorian, G. Temes: Analog MOS Integrated Circuits for Signal Processing, Wiley, 1986
- Leif Hanssen: High Speed Data Converters Fully Integrated in CMOS, dissertation for the dr. scient. Degree, University Of Oslo, 1990.
- A/D , D/A Conversion Handbook, Analog Devices.
- Lecture Notes, University of California, Berkeley, EE247 Analog Digital Interface Integrated Circuits, Fall 07;http://inst.eecs.berkeley.edu/~ee247/fa07/