Nyquist Rate Analog-to-Digital Converters

Tuesday 9th of March, 2009, 9:15 – 11:00

Snorre Aunet, sa@ifi.uio.no
Nanoelectronics Group, Dept. of Informatics
Office 3432

UNIVERSITETET I OSLO

Last time – and today, Tuesday 9th of March:

Last time:

12.1 Decoder-Based Converters
12.2 Binary-Scaled Converters
12.3 Thermometer-Code Converters
12.4 Hybrid Converters

Today – from the following chapters:

13.1 Integrating Converters
13.2 Successive-Approx. Converters
13.3 Algorithmic (or cyclic) A/D Converters
13.4 Flash (or parallel) converters
13.5 Two-Step A/D converters
13.6 Interpolating A/D Converters (16/3-10)
13.7 Folding A/D Converters (16/3-10)
13.8 Pipelined A/D Converters
13.9 Time-Interleaved A/D Converters

Different A/D Converter Architectures

Low-to-Medium Speed High Accuracy	**Medium Speed Medium Accuracy**	**High Speed Low-to-Medium Accuracy**
Integrating	Successive approximation	Flash
Oversampling	Algorithmic	Two-Step
		Interpolating
		Folding
		Pipelined
		Time-interleaved

Different ADCs depending on needs

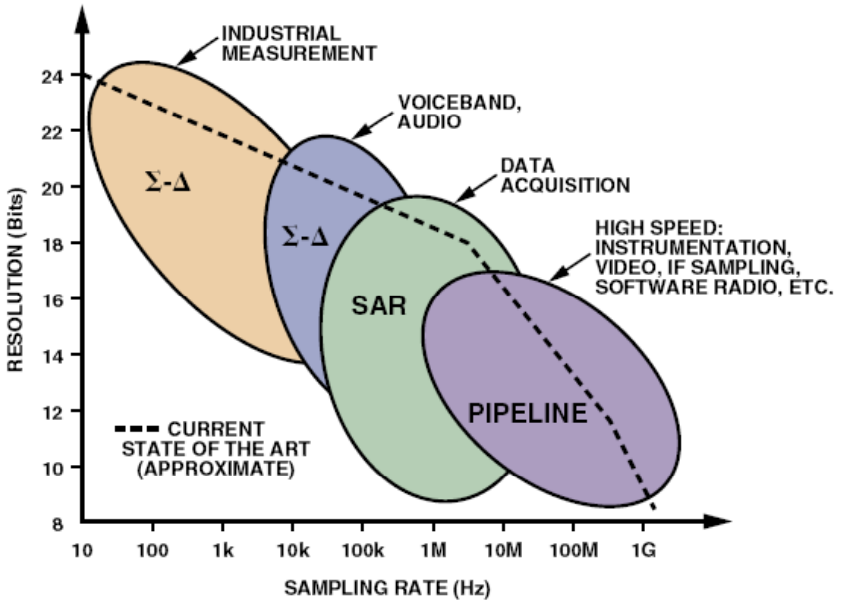


Figure 1. ADC architectures, applications, resolution, and sampling rates.

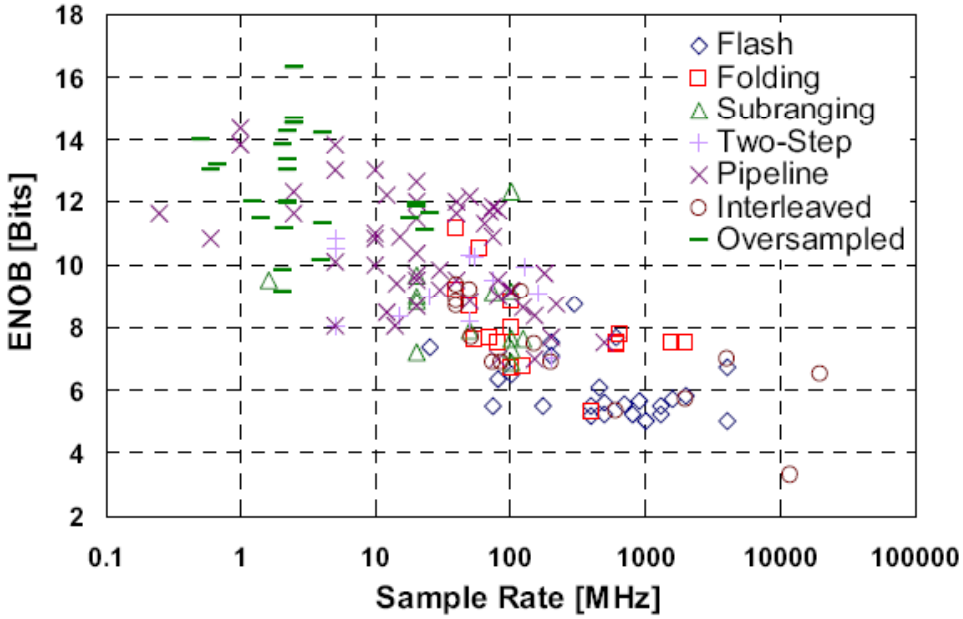


Fig. 2. ADC sample rate vs. ENOB from 1987 to 2005.

Which ADC Architecture Is Right for Your Application?

By Walt Kester [walt.kester@analog.com]

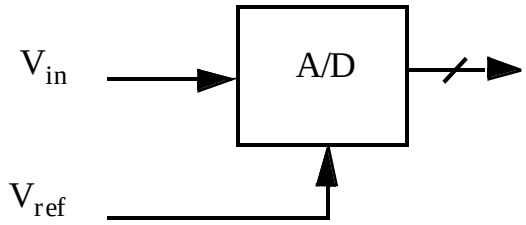
IEEE 2005 CUSTOM INTEGRATED CIRCUITS CONFERENCE

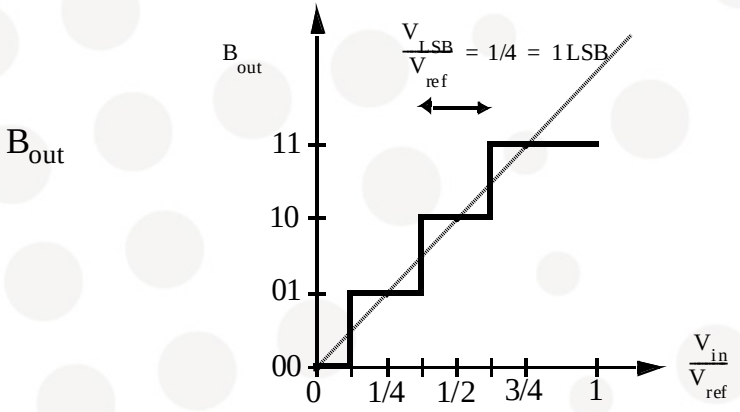
Scaling of Analog-to-Digital Converters into Ultra-Deep-Submicron CMOS

Y. Chiu [1], B. Nikolić [2], and P. R. Gray [2]

[1] Electrical and Computer Engineering, University of Illinois at Urbana-Champaign
[2] Electrical Engineering and Computer Sciences, University of California at Berkeley

A/D-conversion – Basic Principle



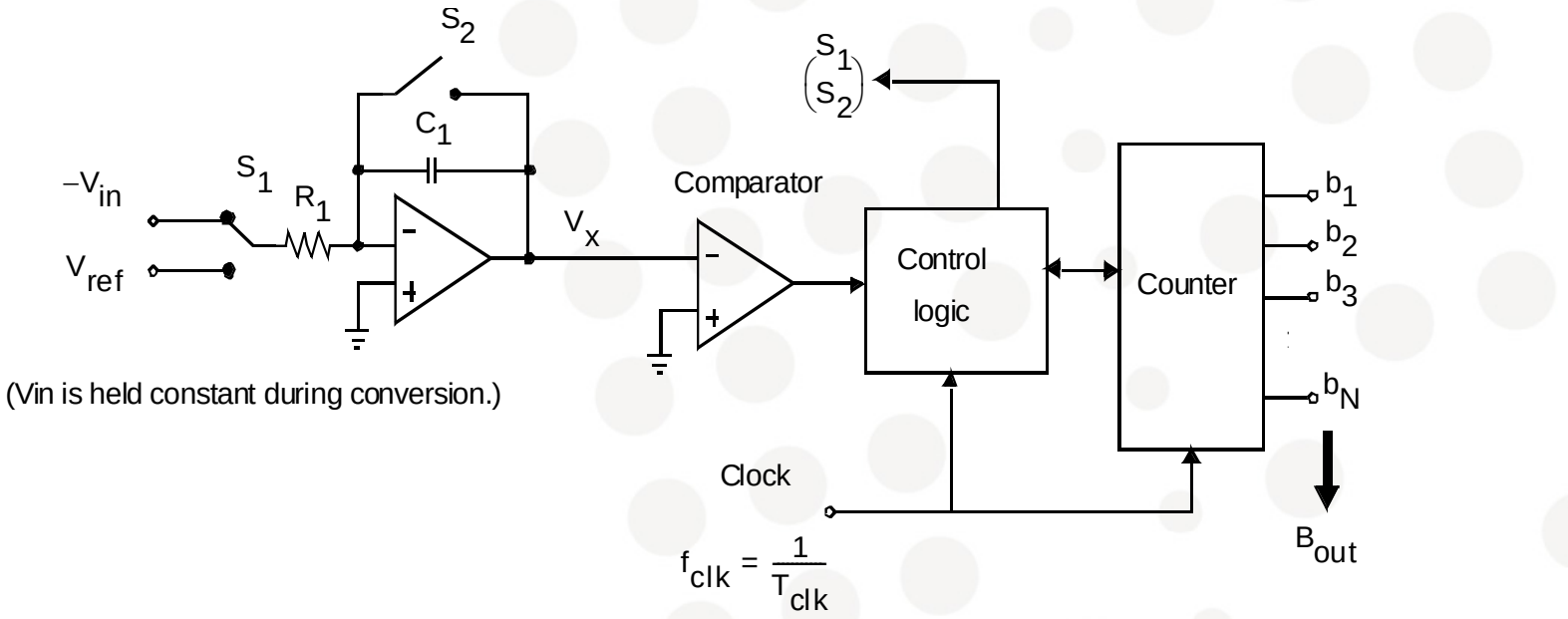


$$V_{ref}(b_1 2^{-1} + b_2 2^{-2} + \ldots + b_N 2^{-N}) = V_{in} \pm x$$

$$\text{where } \left(-\frac{1}{2}V_{LSB} < x < \frac{1}{2}V_{LSB}\right)$$

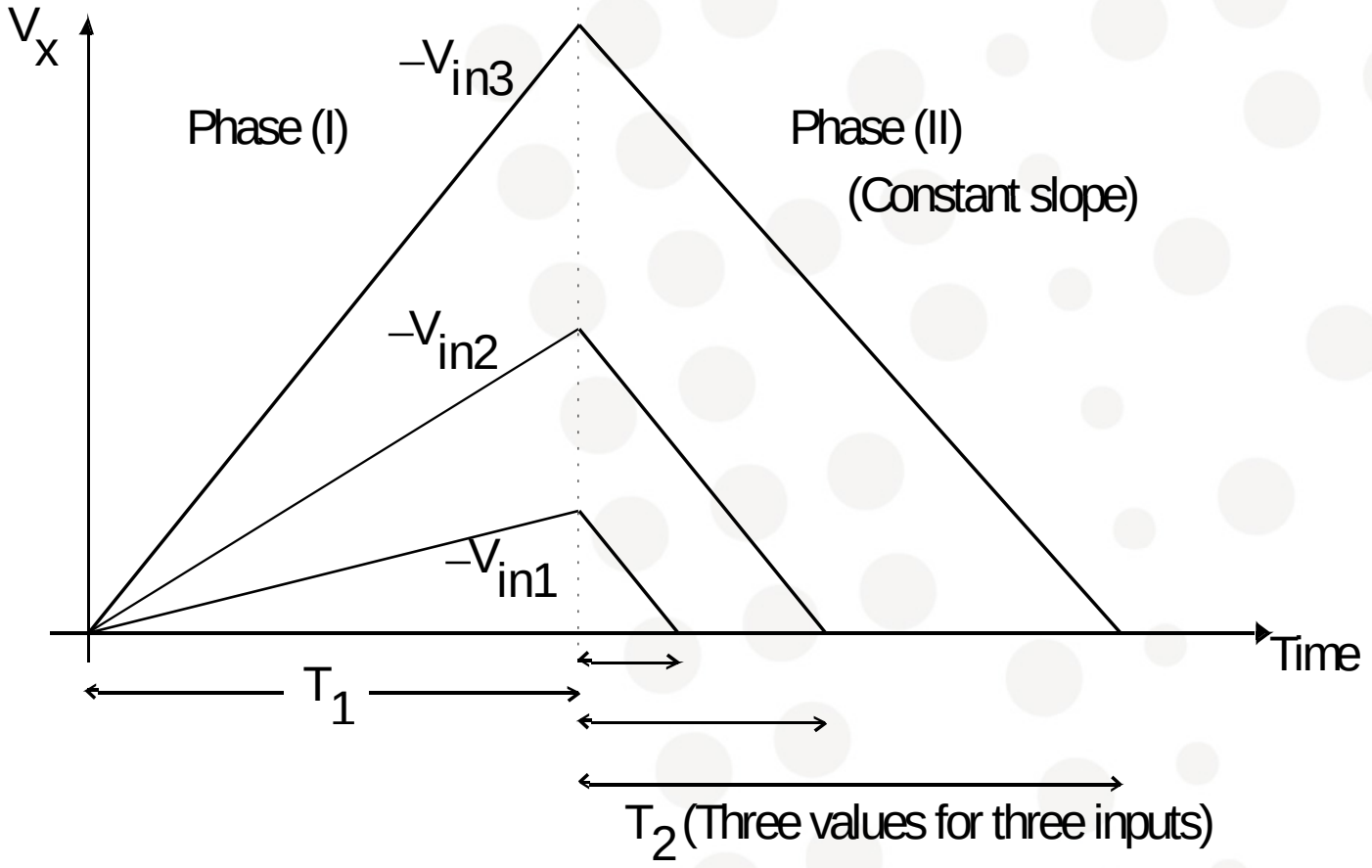
- The analog input value is mapped to discrete digital output value
  - Quantization error is introduced

Integrating Converters (13.1)



- $V_x(t) = V_{in}\ t / RC$ (V_x ramp derivative depending on V_{in})
- High linearity and low offset/gain error
- Small amount of circuitry
- Low conversion speed
  - $2^{N+1} * 1/T_{clk}$ (Worst case)

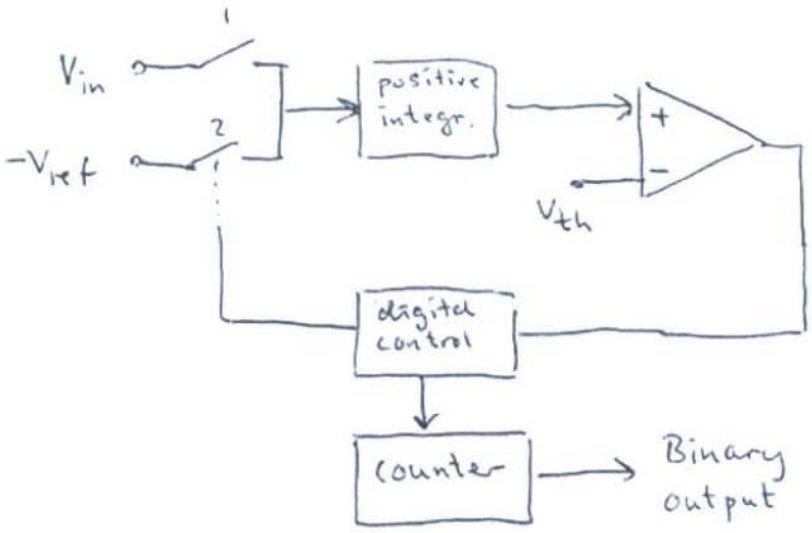
Integrating Converters

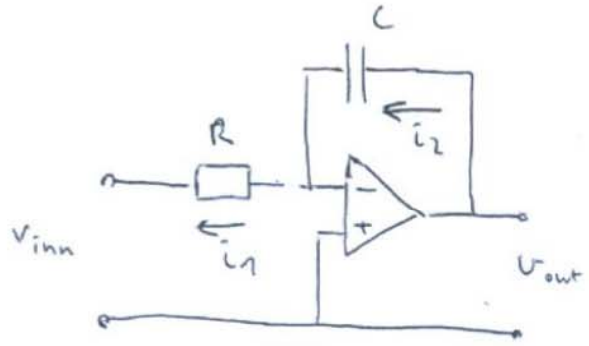


- The digital output is given by the count at the end of T_2
- The digital output value is independent of the time-constant RC

Dual slope ADC

POSITIVE INTEGRATOR USED IN DUAL-SLOPE ADCS





$$i_1 = i_2$$

$$\frac{v_{inn}}{R} = C\frac{dv_{out}}{dt}$$

$$\Updownarrow$$

$$\frac{dv_{out}}{dt} = \frac{v_{inn}}{RC}$$

$$v_{out} = \frac{1}{RC}\int_0^t v_{inn}\,dt$$

$$= \frac{V_{in}}{RC}\,t$$

Example: 16-bit two-slope ADC with $V_{in} = 3V$, $V_{x\,max} = 4V$ and $T_1 = 20ms$. RC-constant? Clock fr?

$$f_{clk} = \frac{1}{T_{clk}} = \frac{2^{16}}{20ms} \approx 3.28\,MHz$$

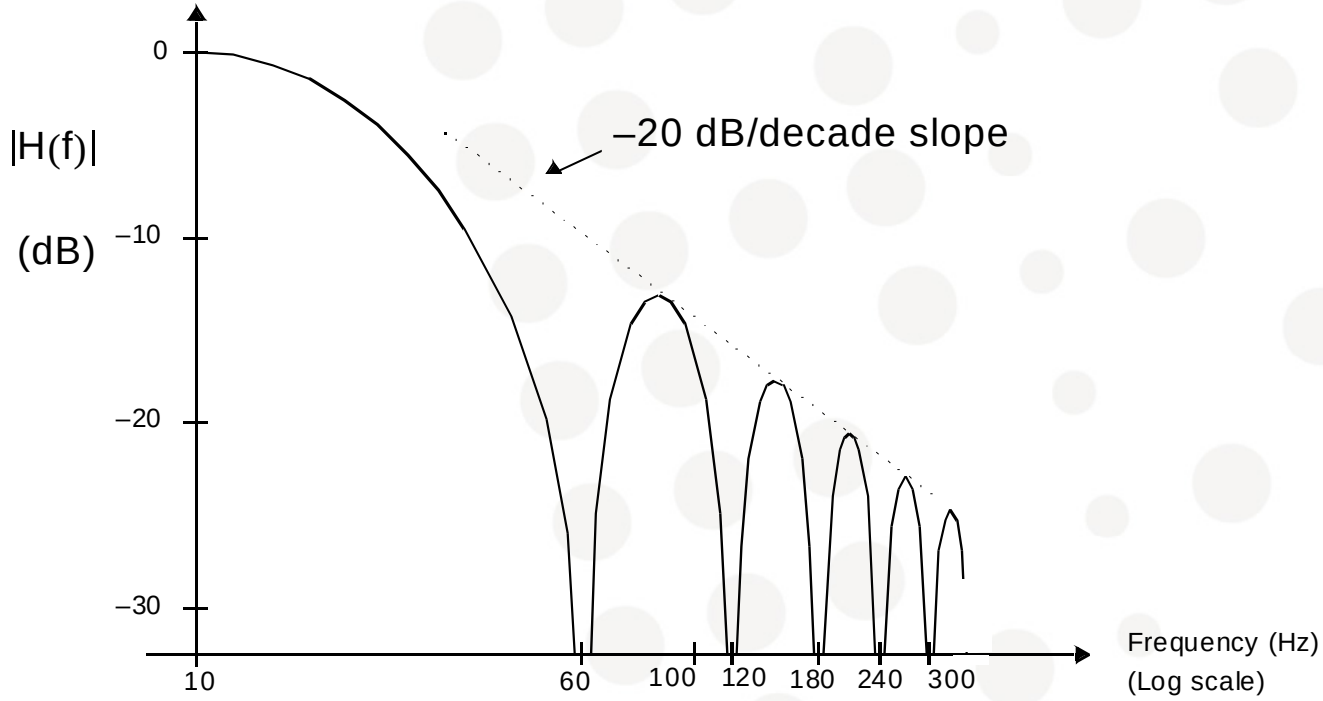
equation (13.15):

$$V_x = \frac{V_{in}\,T_1}{RC} \Leftrightarrow 4V = \frac{3V\,20ms}{RC}$$

$$\Updownarrow$$

$$RC = 15ms$$

Integrating Converters – careful choice of T1 can attenuate frequency components superimposed on the input signal



- In the above case, 60 Hz and harmonics are attenuated when T1 is an integer multiple of 1/60 Hz.
- Sinc-response with rejection of frequencies multiples of $1/T_1$

Successive approx ADC algorithm (13.2)

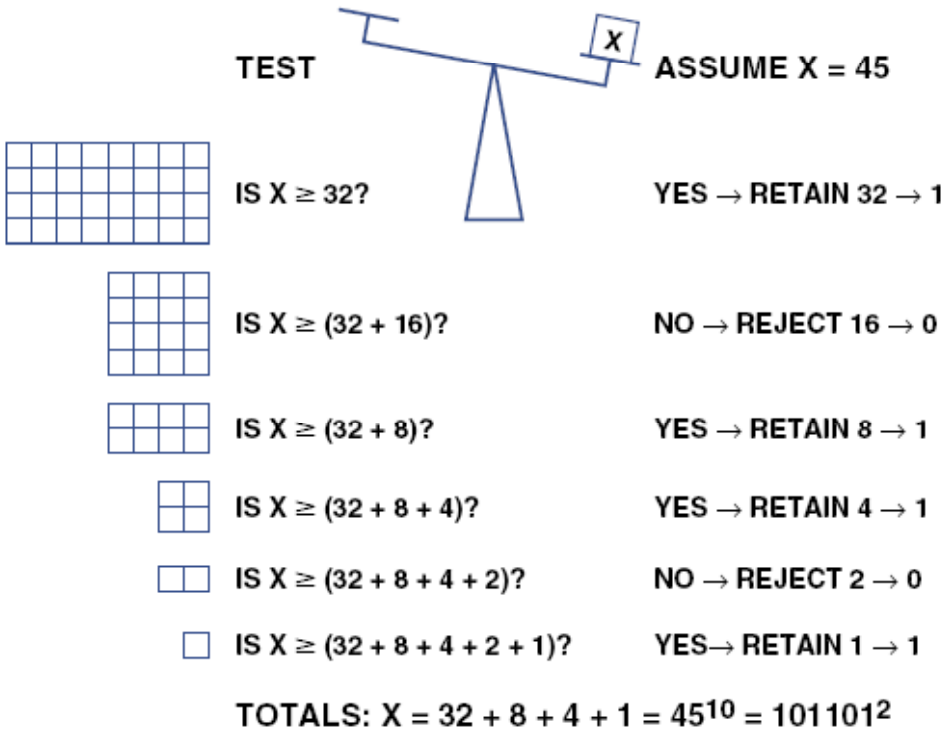


Figure 4. Successive-approximation ADC algorithm using balance scale and binary weights.

Which ADC Architecture Is Right for Your Application?

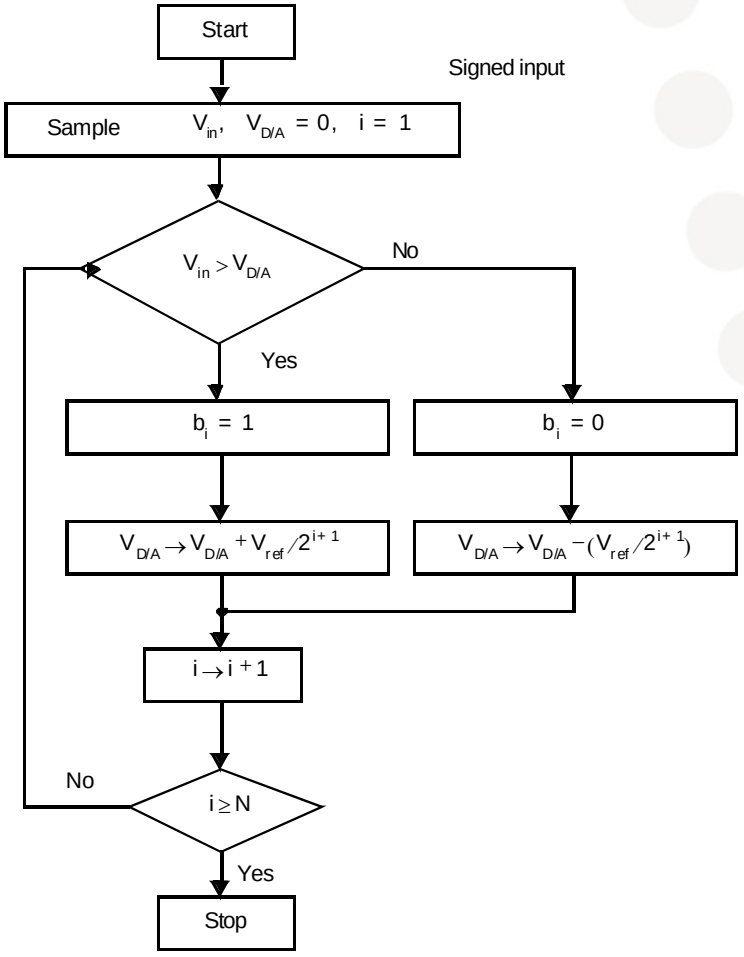
By Walt Kester [walt.kester@analog.com]

- If we have weights of 1 kg, 2 kg, 4 kg, 8 kg, 16 kg, 32 kg and will find the weight of an unknown X assumed to be 45 kg.
- 101101_2

$=1*32+0*16+1*8+1*4+0*2+1*1$

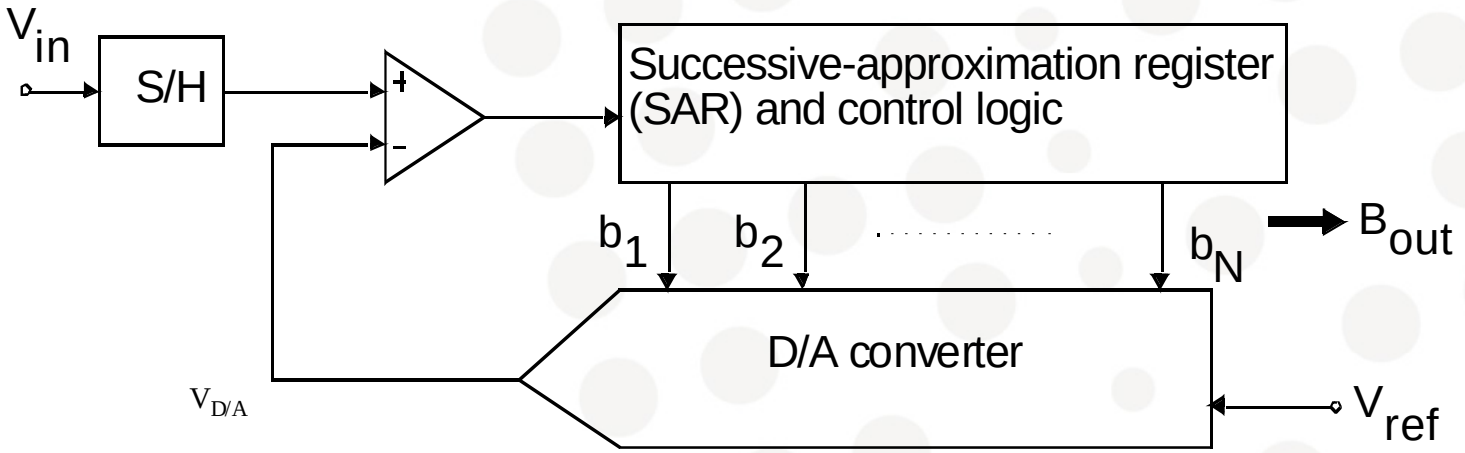
$= 45_{10}$

Successive-Approximation Converters



- Uses binary-search algorithm
- Accuracy of 2^N requires N steps
- The digital signal accuracy is within +/- 0.5 V_{ref}
- Medium speed
- Medium resolution
- Relatively moderate complexity

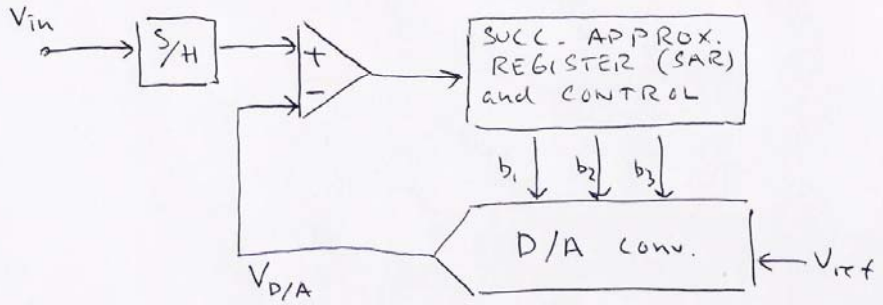
DAC-Based Successive Approximation

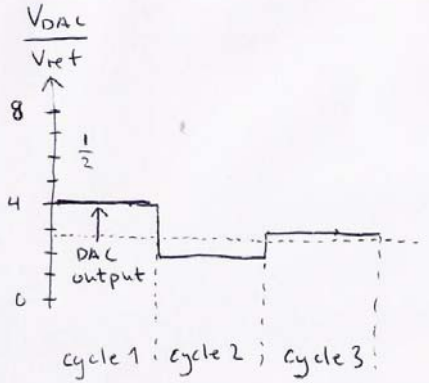


- $V_{D/A}$ is adjusted until the value is within 1LSB of V_{in}
- Starts with MSB and continues until LSB is found
- Requires DAC, S/H, Comparator and digital logic
- The DAC is typically limiting the resolution

Succ. Approx ADC, example 13.2

Example 13.2





$V_{ref} = 8\,V$

$V_{in} = 2.831\,V$

3-bit conversion

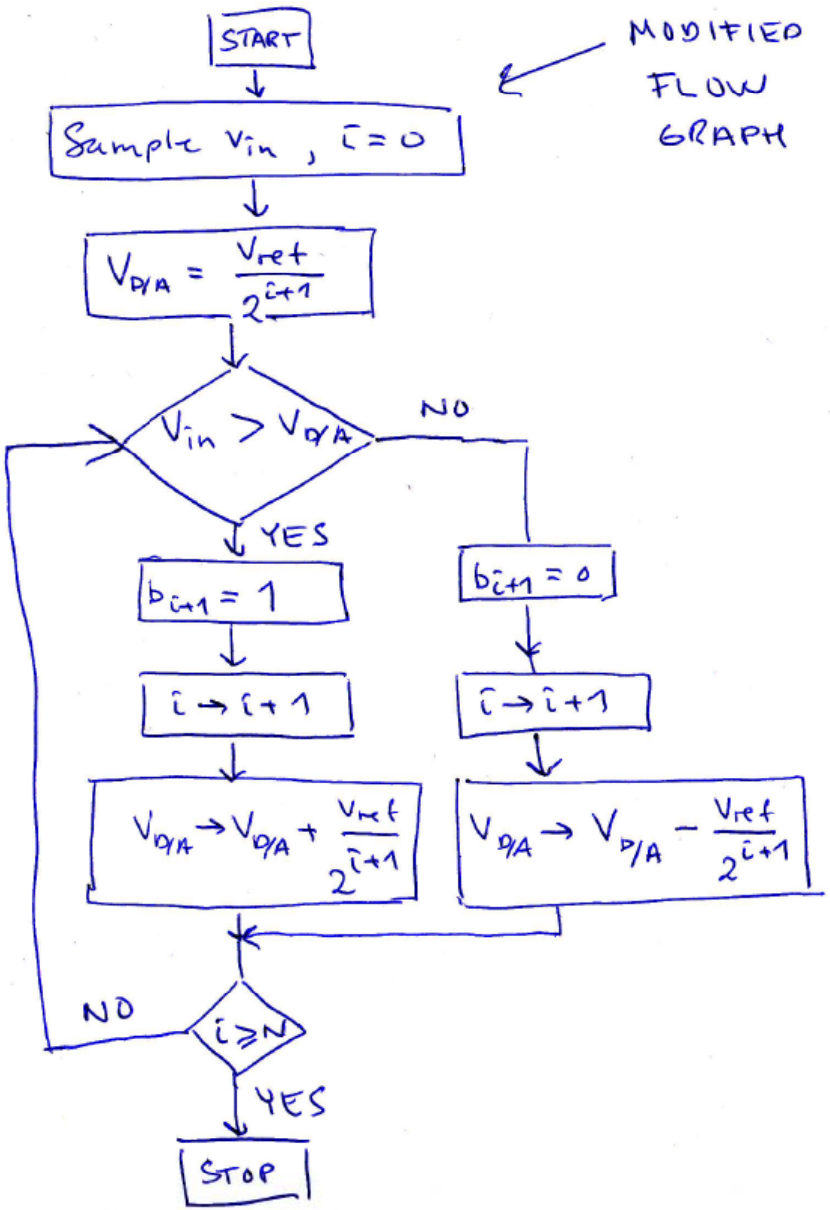
0	0	0	0
0	0	1	
0	1	0	
0	1	1	
1	0	0	
1	0	1	
1	1	0	
1	1	1	

cycle 1 : $B_{out} = 100$, so that $V_{D/A} = 4.0\,V$. Since $V_{in} < V_{D/A}$, $b_1 \to 0$

cycle 2 : $B_{out} = 010$, so that $V_{D/A} = 2.0\,V$. Since $V_{in} > V_{D/A}$, $b_2 \to 1$

cycle 3 : $B_{out} = 011$, — " — $3.0\,V$. Since $V_{in} < V_{D/A}$, $b_3 \to 0$

010



Ex. 13.2

$V_{ref} = 8V$, $V_{in} = 2.831\,V$

$V_{D/A} = \frac{V_{ref}}{2^{i+1}} = \frac{8V}{2^1} = 4V$

$V_{in} > V_{D/A} \iff 2.831\,V > 4V$? → NO!

$b_{i+1} = b_{0+1} = b_1 = 0$

$i \to i+1 = 0+1 = 1$

$V_{D/A} \to 4V - \frac{8}{2^2}V = 4V - 2V = 2V$

$i = 1 \geq 3$? → NO

$V_{in} > V_{D/A} \iff 2.831\,V > 2V$? → YES!

$b_{i+1} = b_{1+1} = 1$; $b_2 = 1$

$i \to i+1 = 1+1 = 2$

$V_{D/A} \to V_{D/A} + \frac{V_{ref}}{2^{i+1}} = 2V + \frac{8}{2^{2+1}}V = 2V + 1V = 3V$

$i = 2$, $2 \geq 3$? NO!

$V_{in} > V_{D/A} \iff 2.831\,V > 3V$? — NO!

$b_3 = 0$

$i \to 2+1$

$V_{D/A}$ update, $3 \geq 3 \Rightarrow$ STOP

Charge-Redistribution A/D-Converter (unipolar)

- Instead of using a separate DAC and setting it equal to the input voltage (within 1 LSB) as for the DAC based converter from figure 13.5, one can use the error signal equaling the difference between the input signal, V_{in}, and the DAC output, $V_{D/A}$

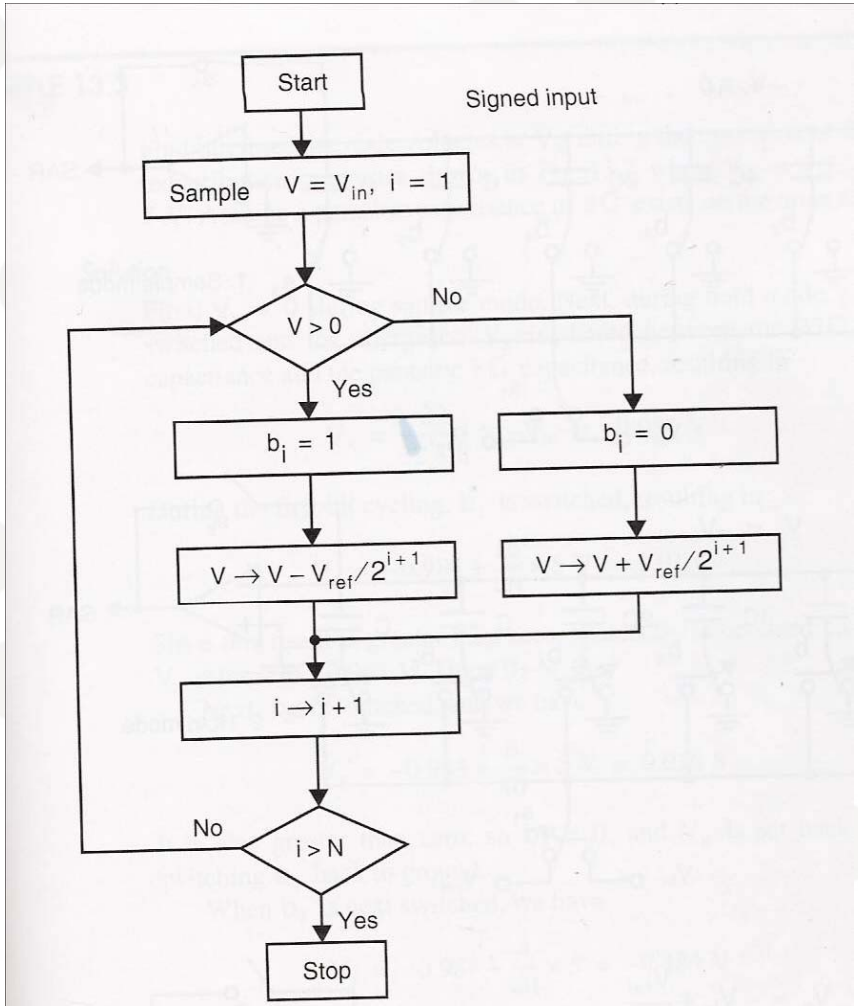


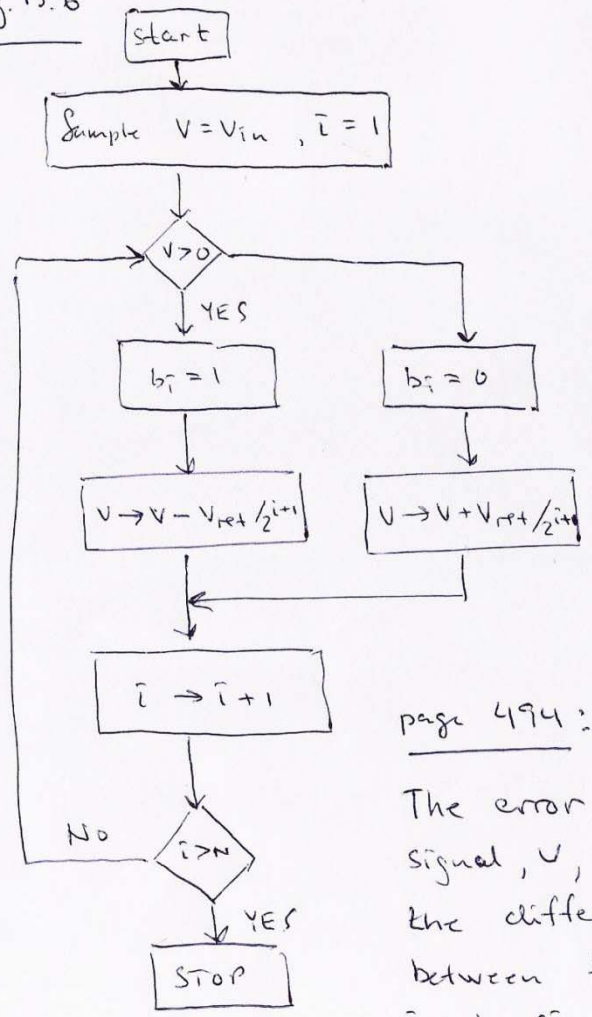
Fig. 13.6 Flow graph for a modified successive approximation (divided remainder).

Numbers from 13.2 setting an error signal V equal to $V_{in} - V_{D/A}$ – modified succ. approx as in fig. 13.6

EXAMPLE 13.2 USING MODIFIED SUCC. APPROX (DIVIDED REMINDER)

Error signal, $V = V_{in} - V_{DAC}$

Fig. 13.6



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The error signal, V, equals the difference between the input signal, V_{in}, and the D/A output

$V = +2.831V + 4V = -1.169V$

$-1.169 > 0$? NO, $b_1 = 0$

$V \rightarrow -1.169V + 2V = 0.831V$

$i = i + 1 = 2$

$i = 2 > 3$? NO

$0.831V > 0$?

YES

$b_2 = 1$

$V \rightarrow (0.831 - 8/8)V = -0.169V$

$i = 2 + 1 = 3$

$i > 3$?

NO

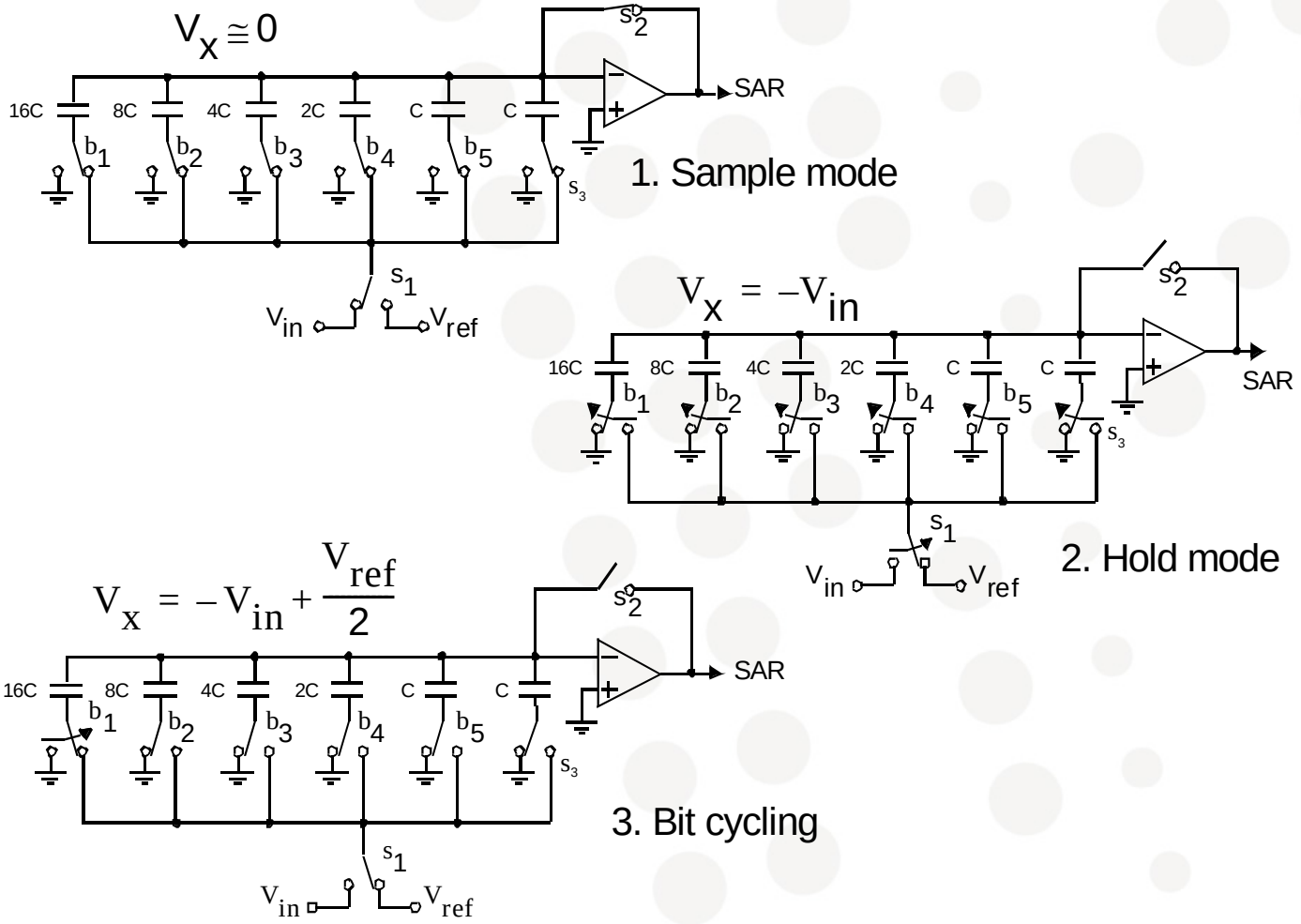
$-0.169V > 0$?

NO → $b_3 = 0$

$b_1 b_2 b_3 = 010$

(like in ex. 13.2)

Unipolar Charge-Redistribution A/D-Converter



Charge-Redistribution A/D-Converter

- Sample mode:
  - All capacitors charged to Vin while the comparator is reset to its threshold voltage through S_2. The capacitor array is performing S/H operation.
- Hold mode:
  - The comparator is taken out of reset by opening S_2, then all capacitors are switched to ground. V_x is now equal to $-V_{in}$. Finally S_1 is switched so that V_{ref} can be applied to the capacitors during bit-cycling.
- Bit-cycling:
  - The largest capacitor is switched to V_{ref}. V_x goes to $-V_{in} + V_{ref}/2$. If V_x is negative, then V_{in} is greater than $V_{ref}/2$ and the MSB capacitor is left connected to V_{ref}. Otherwise the MSB capacitor is disconnected and the same procedure is repeated N times

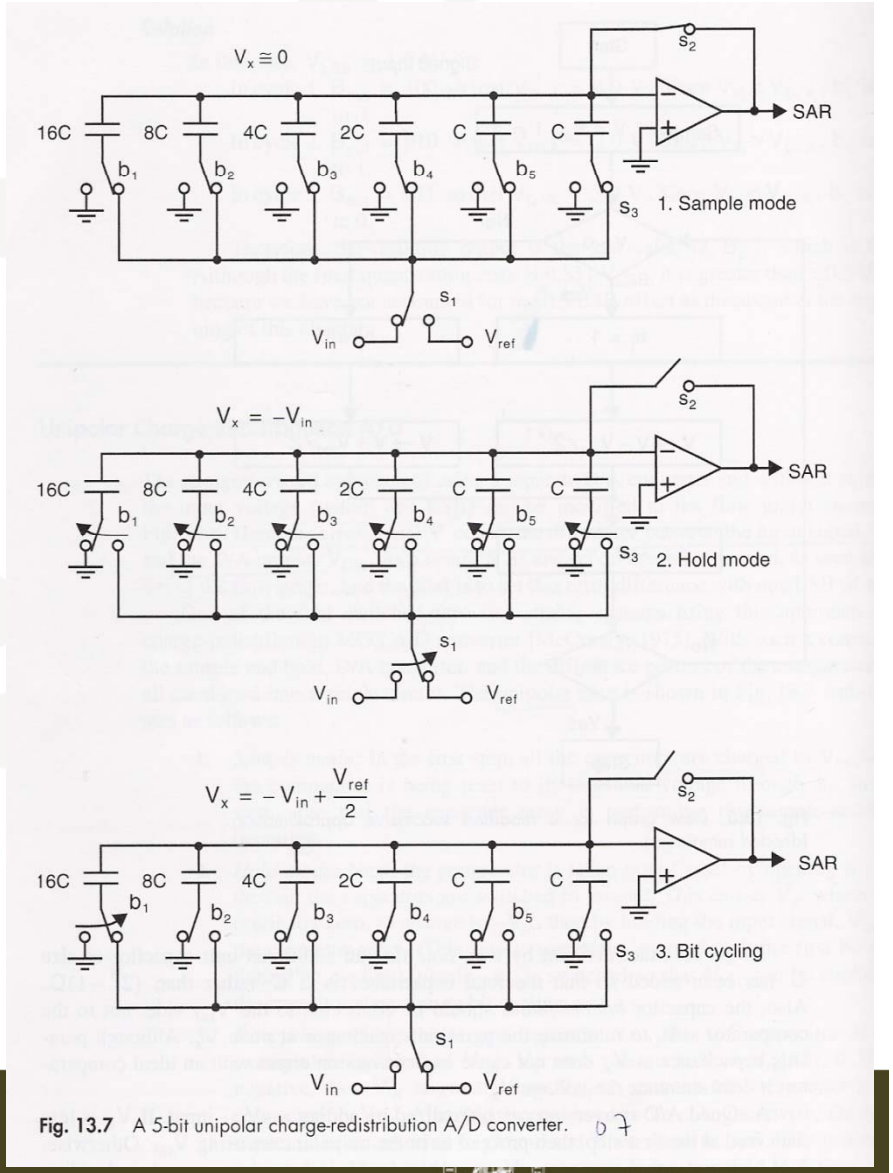


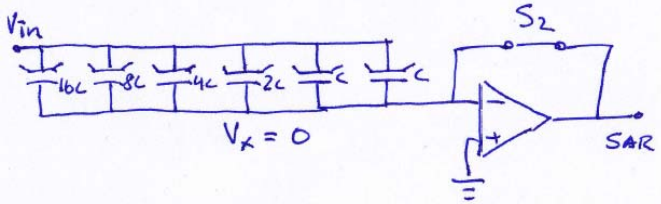
Fig. 13.7 A 5-bit unipolar charge-redistribution A/D converter.

Ex. 13.3 pp. 497

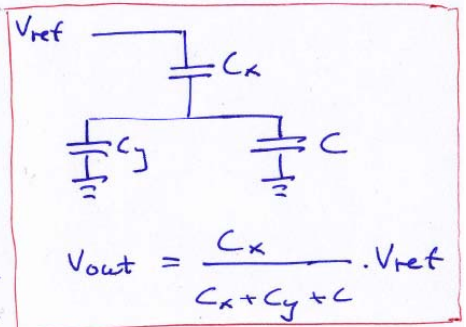
Find intermediate node voltages at V_x during the operation of the 5-bit charge-redistribution converter shown in fig. 13.7. Assume 8C as a parasitic cap. at V_x

$V_{ref} = 5V$, $V_{in} = 1.23V$

SAMPLE MODE:



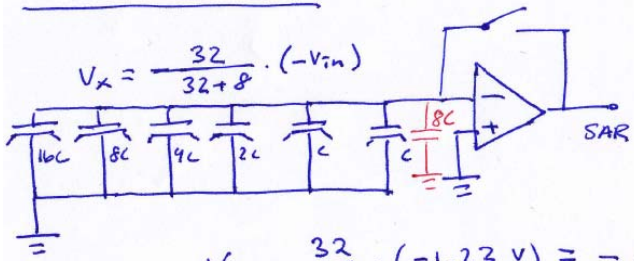
Top-plates to V_-, to minimize parasitic capacitance at node V_x.



$$V_{out} = \frac{C_x}{C_x + C_y + C} \cdot V_{ref}$$

C_x and C_y functions of digital word/switching

HOLD MODE:



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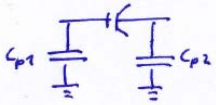
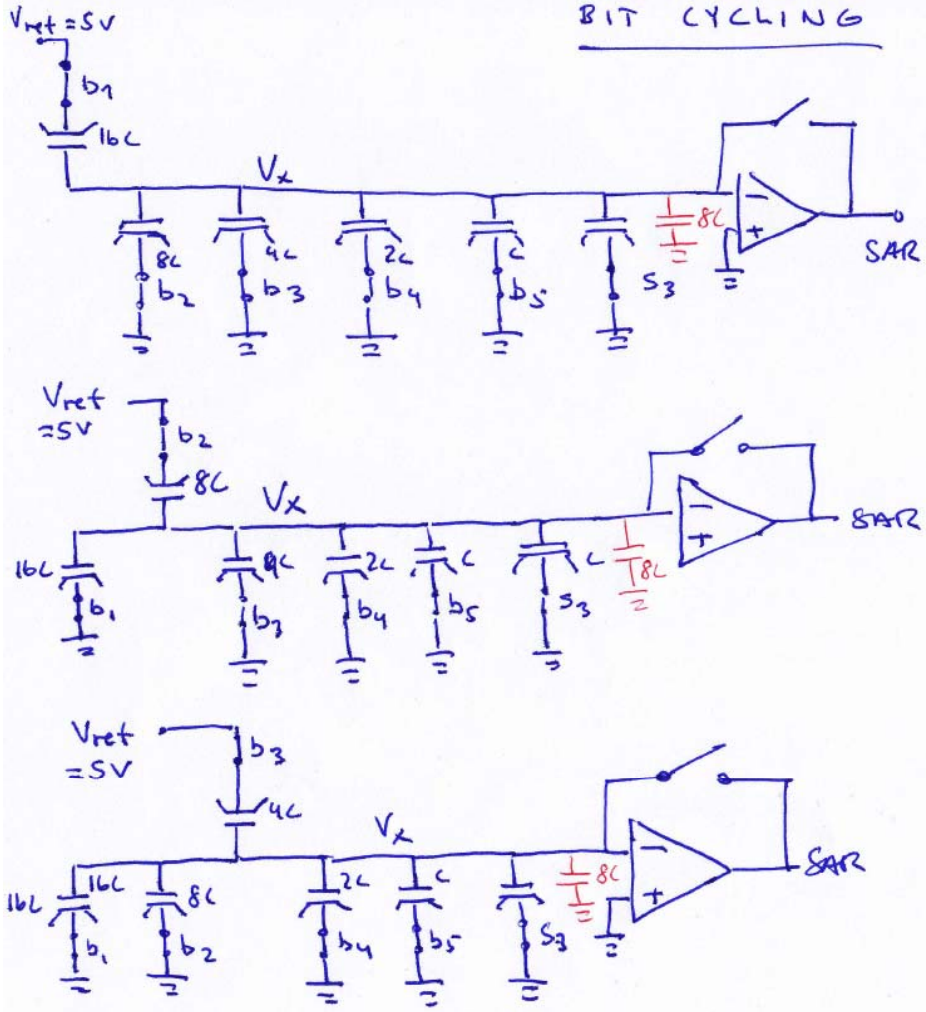


$C_{p1} < C_{p2}$

1) Sample mode
2) Hold mode
3) Bit-cycling

$$V_x = \frac{32}{40} \cdot (-1.23\,V) = -0.984\,V$$



- b_1 is switched, controlling the 16C capacitor:

$$V_x = -0.984V + \frac{16}{(32+8)} \cdot 5V$$

$$= -0.984\,V + 2V = 1.016V$$

$V_x > 0 \Rightarrow b_1 = 0$

- $V_x = -0.984V + \frac{8}{(32+8)} \cdot 5V$

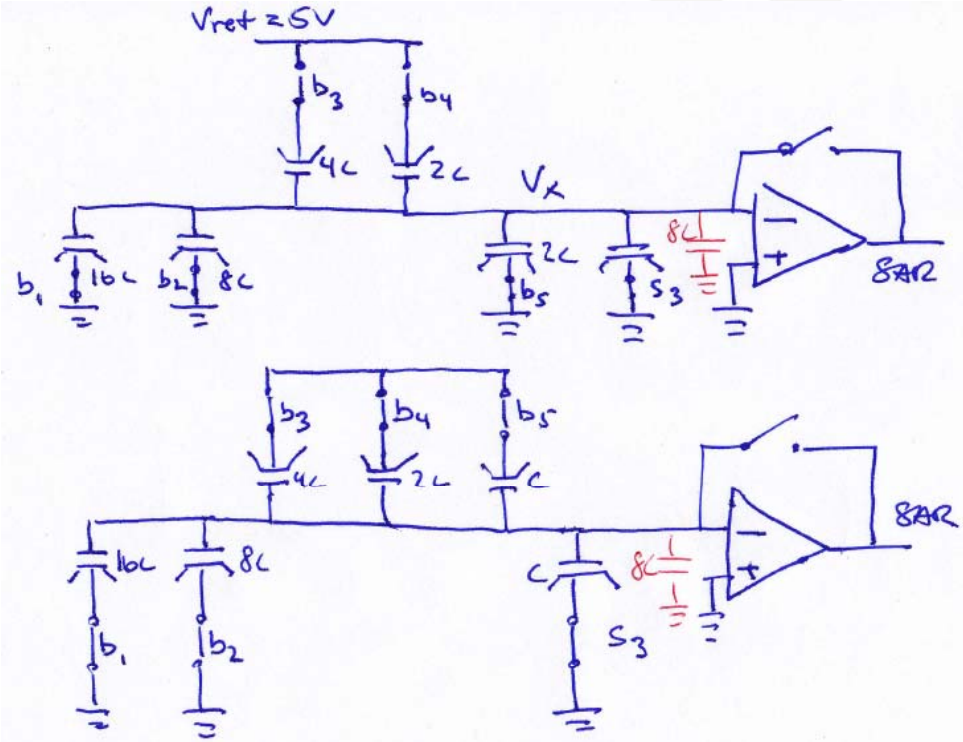
$V_x = -0.984V + 1V = 0.016V$

When b_2 is switched $V_x > 0$, so $b_2 = 0$ and V_x is set back to -0.984 V by switching b_2 back to gnd.

- b_3 is switched:

$V_x = -0.984\,V + \frac{4.5}{40}V = -0.484V$

V_x is now $< 0 \Rightarrow b_3 = 1$ and b_3 left connected to V_{ref}.



- b_4 is switched:

$$V_x = -0.984V + \frac{6}{40} \cdot 5V =$$

$$-0.984V + 0.75V = -0.234V$$

$V_{x_4} < 0 \Rightarrow b_4 = 1$

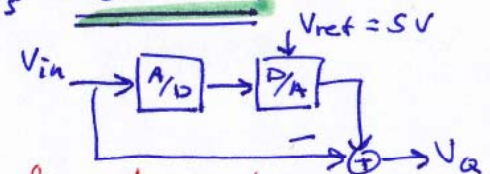
- b_5 is switched:

$$V_{x_5} = -0.234V + \frac{1}{40} \cdot 5V = -0.109V$$

$V_{x5} < 0 \Rightarrow b_5 = 1$

$B_{out} = b_1 b_2 b_3 b_4 b_5 = 00111$

$$\frac{5V}{2^5} = \frac{5V}{32} = 0.15625\,V$$



DAC: $V_{out} = V_{ref}\left(b_1 2^{-1} + b_2 2^{-2} + b_3 \cdot 2^{-3} + b_4 \cdot 2^{-4} + b_5 \cdot 2^{-5}\right)$

$= 5V\,(0.125V + 0.0625V + 0.03125V) = 5V\,(0.21875) = 1.09375\,V$

May also be expressed from the drawing and the ops.

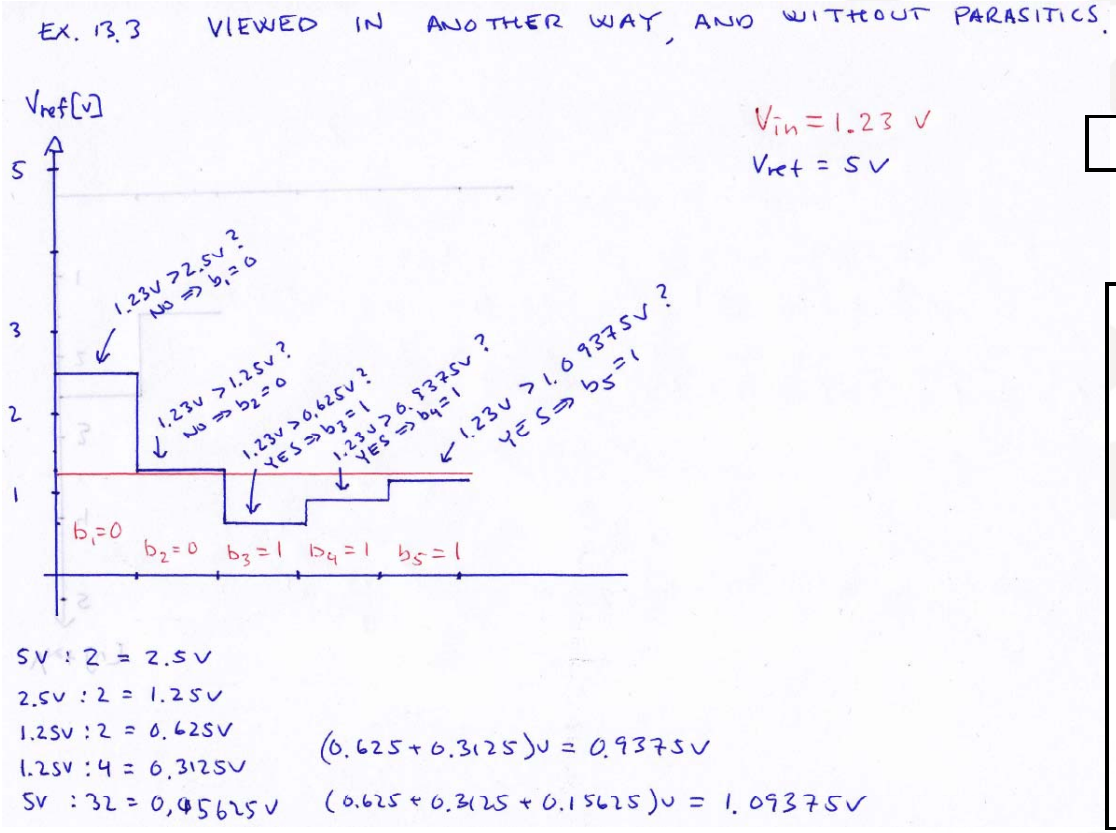
Sampled volt.:

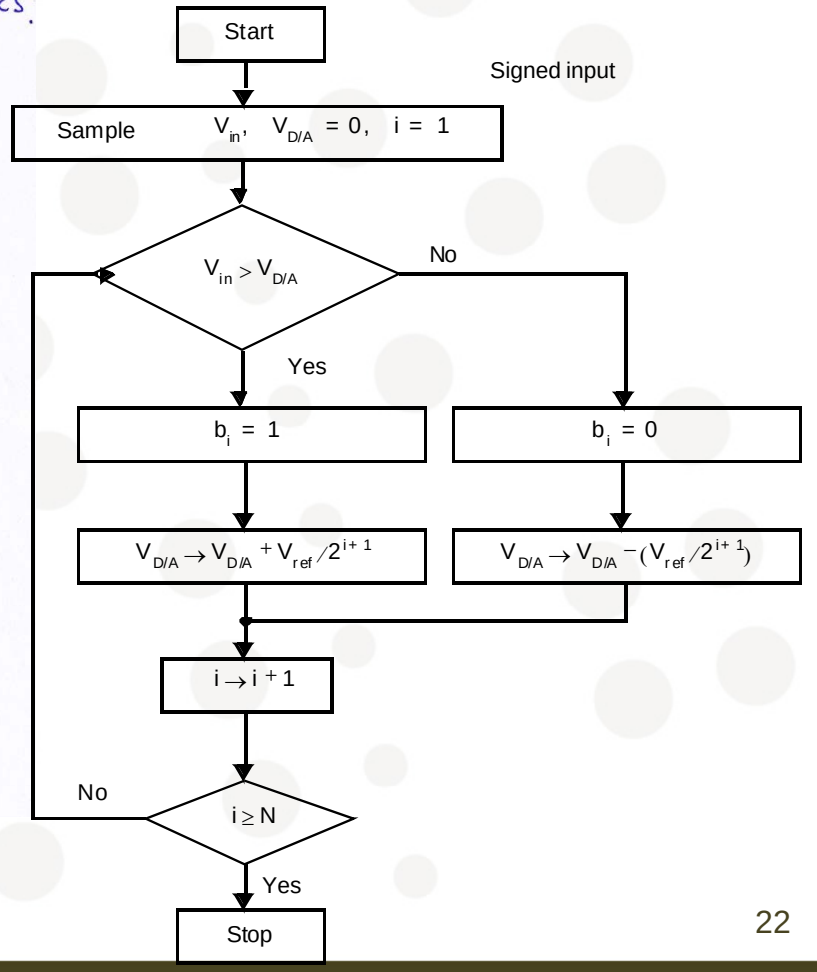
$$\frac{32}{32+8}(-V_{in}) + \frac{7}{32+8} \cdot 5V =$$

$$-0.984V + 0.875V = -0.109V$$

$V_Q = 1.09375V \div 1.23V = -0.13625$

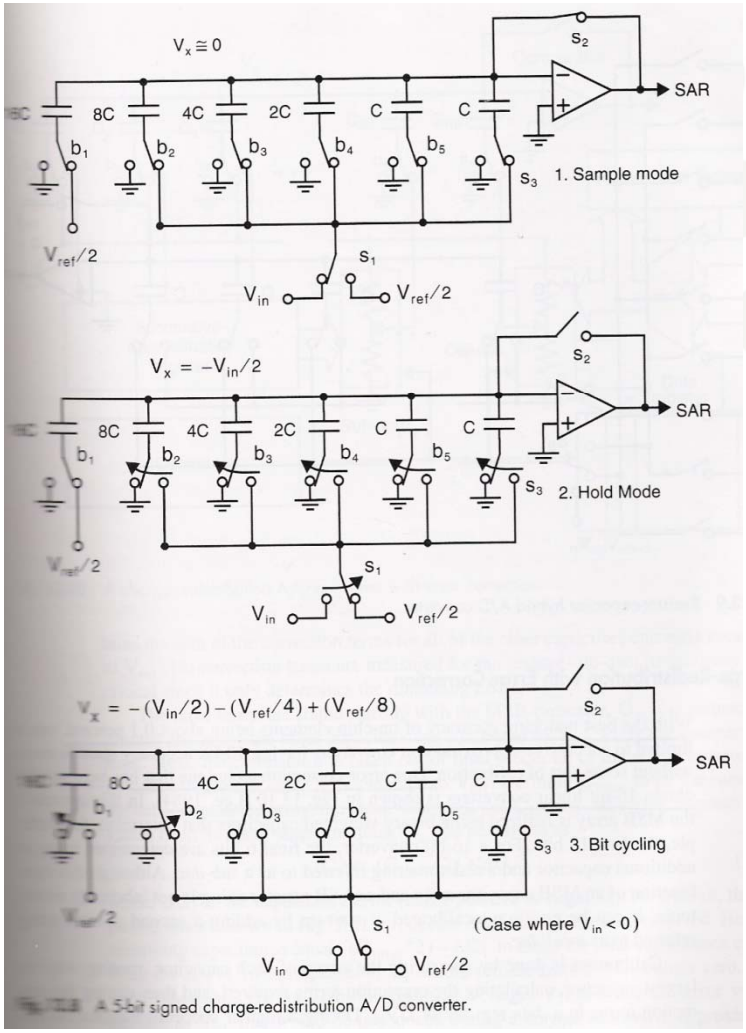
Succ. Approx. Approach flow graph





Signed Charge redistribution A/D

(Fig. 13.8)



A 5-bit signed charge-redistribution A/D converter.

- Resembling the unipolar version (Fig. 13.7)
- Assming V_{in} is between +/- $V_{ref}/2$
- Disadvantage: V_{in} attenuated by a factor 2, making noise more of a problem for high resolution ADCs
- Any error in the MSB capacitor causes both offset and a sign-dependent gain error, leading to INL errors

Resistor-Capacitor Hybrid (figure 13.9 in ”J & M”)

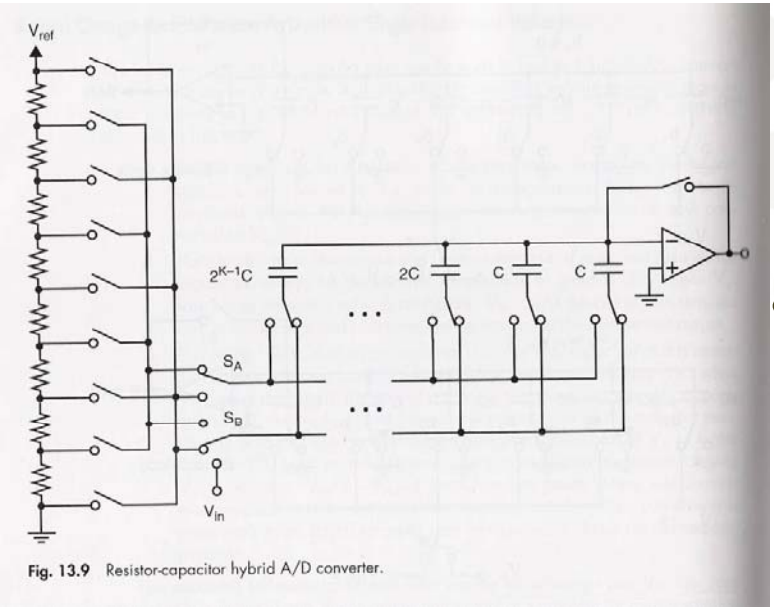


Fig. 13.9 Resistor-capacitor hybrid A/D converter.

- First all capacitors are charged to V_{in} before the comparator is being reset.
- Next a succ. approx. conversion is performed to find the two adjacent resistor nodes having voltages larger and smaller than V_{in}
- One bus will be connected to one node while the other is connected to the other node. All of the capacitors are connected to the bus having the lower voltage.
- Then a successive approximation using the capacitor-array network is done, starting with the largest capacitor…

Speed estimate for charge-redistribution converters

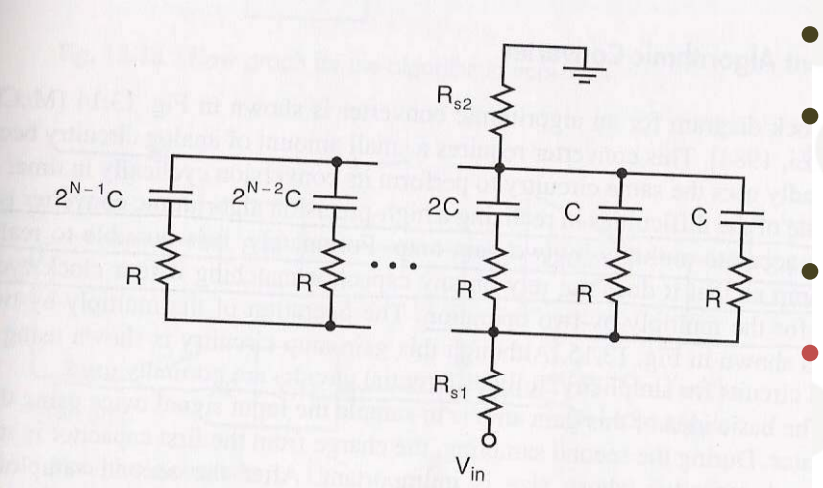


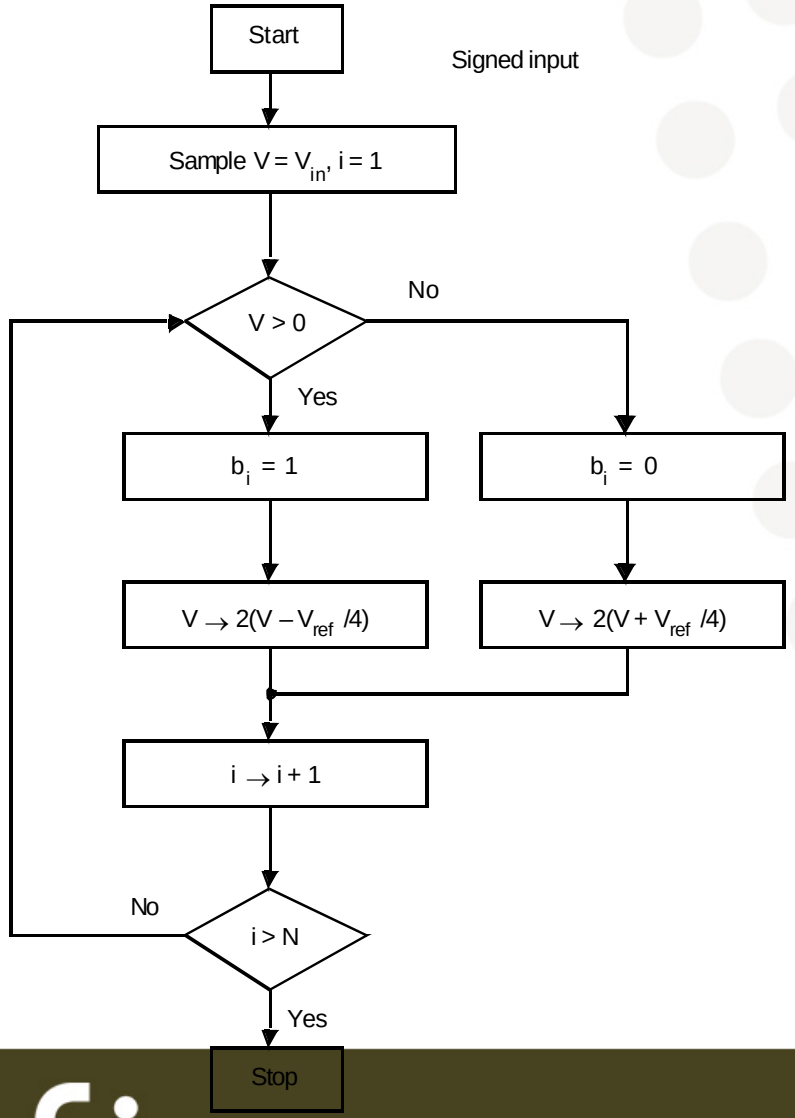
Fig. 13.12 Simplified model of a capacitor array during the sampling time.

- RC time constants often limit speed
- Individual time constant due to the 2C cap.: $(R_{s1}+R+R_{s2})2C$
- (R ; bit line)
- $Tau_{eq}=(R_{s1}+R+R_{s2})2^{N}C$, for the circuit in fig. 13.12
- For better tha 0.5 LSB accuracy: $e^{-T/Taueq} < 1/(2^{N}+1)$, T = charging time
- $T > Tau_{eq}\ (N+1)\ \ln 2$

  $= 0.69(N+1)Tau_{eq}$

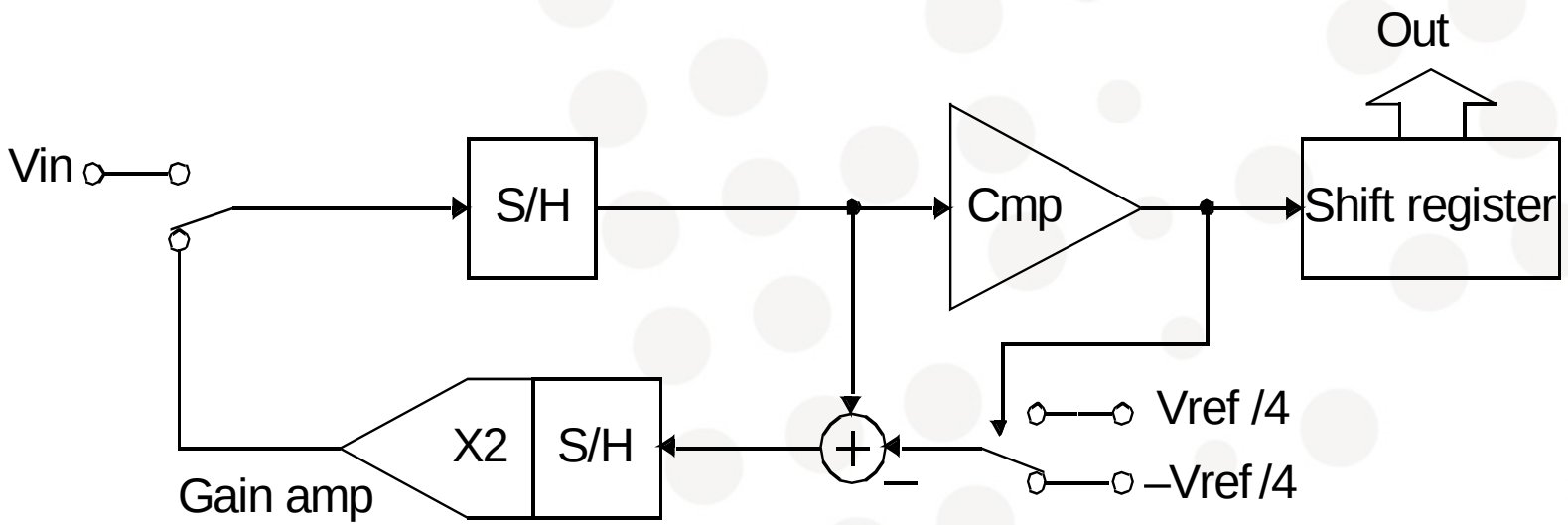
- 30 % higher than from Spice simulations (”J & M”)

Algorithmic (or Cyclic) A/D Converter (13.3)



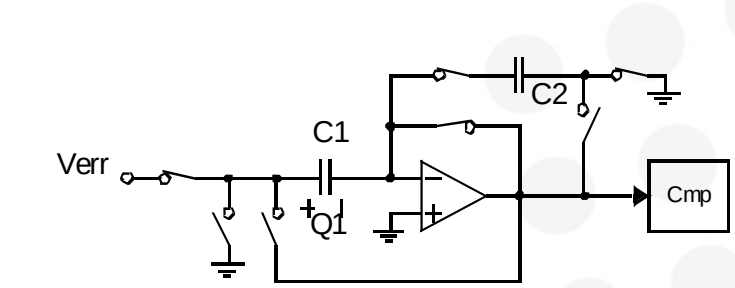
- Similar to the Successive approximation converter
- Constant V_{ref}
- Doubles the error each cycle, instead of halving the reference voltage in each cycle, like succ. approx. conv.
- Requires an accurate multiply-by-2 amplifier
- Accuracy can be improved by operating in four cycles (instead of two)
- compact

Ratio-Independent Algorithmic Converter

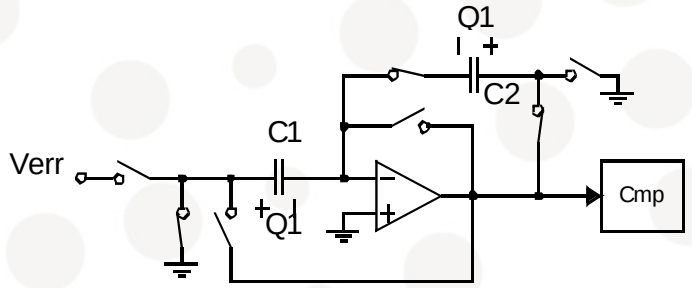


- Simple circuitry
- Due to the cyclic operation the circuitry are reused in time
- Fully differential circuits normally used

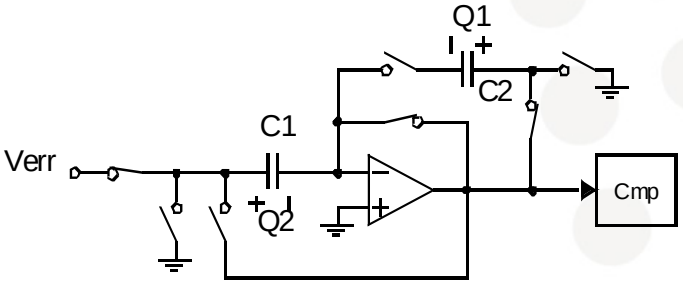
Ratio-Independent Algorithmic Converter



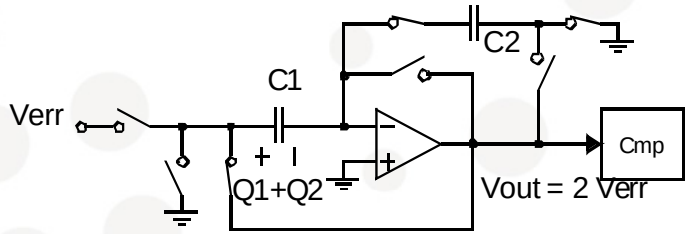
1. Sample remainder and cancel input-offset voltage.



2. Transfer charge Q_1 from C_1 to C_2.



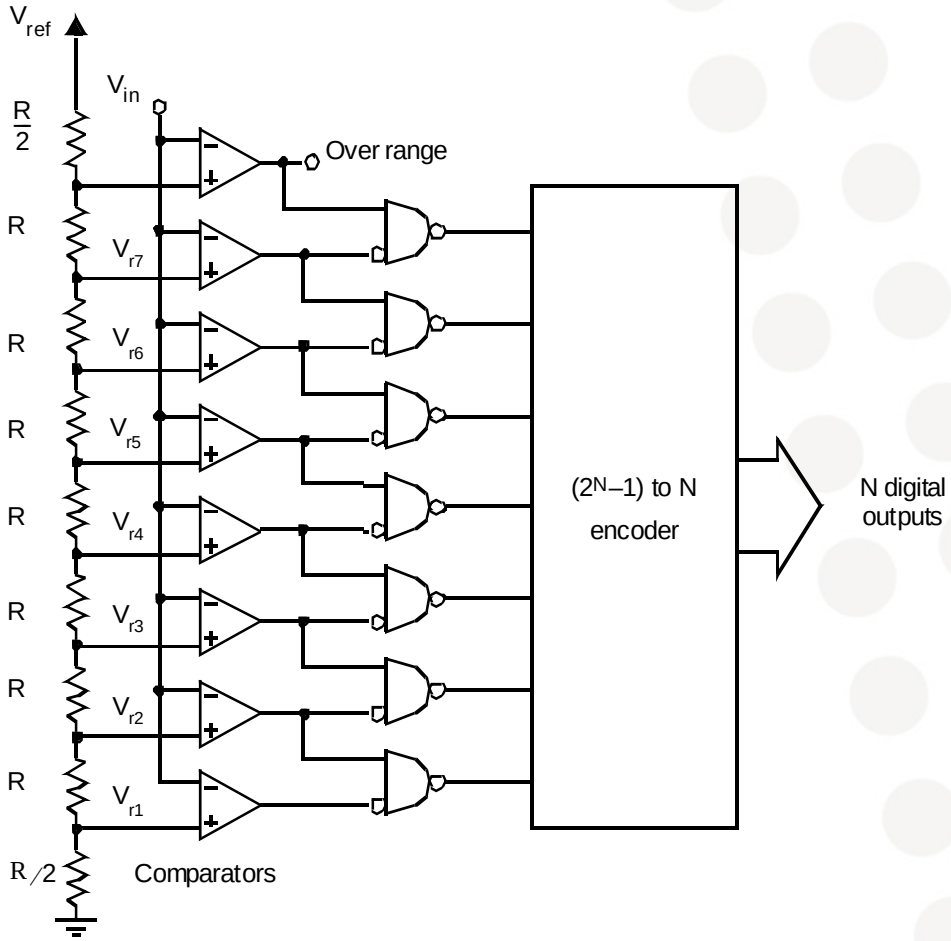
3. Sample input signal with C_1 again after storing charge Q_1 on C_2.



4. Combine Q_1 and Q_2 on C_1, and connect C_1 to output.

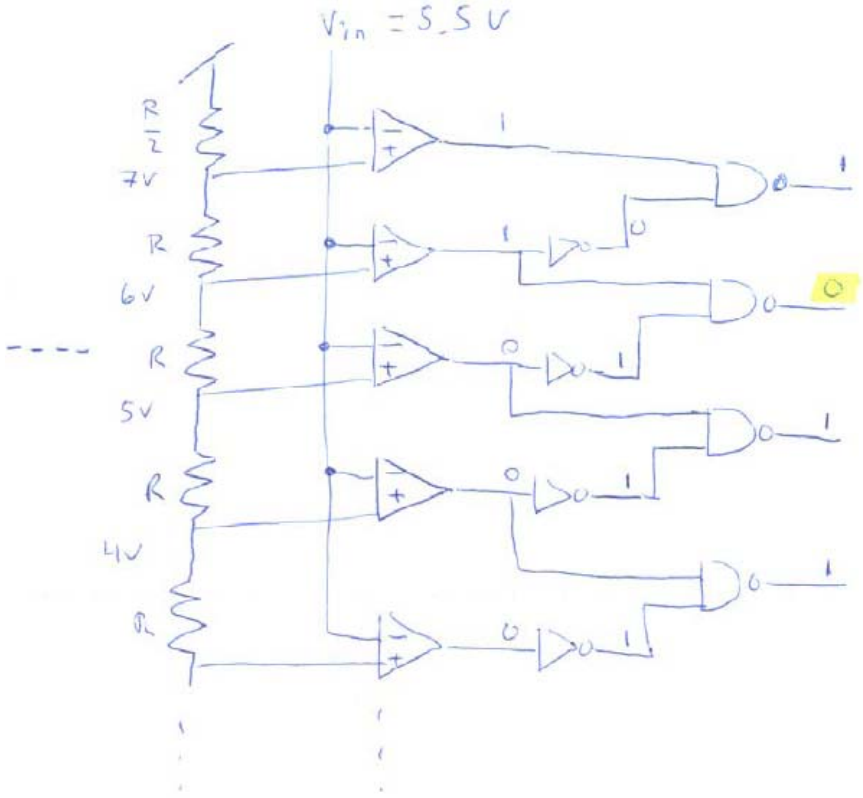
- The basic idea is to sample the input signal twice using the same capacitor. During the 2nd sampling the charge from the 1st capacitor is stored on a 2nd capacitor whose size is unimportant. After the 2nd sampling both charges are recombined into the 1st capacitor which is then connected between the opamp input and output.
- Does not rely on capacitor matching, is insensitive to amplifier offset.

Flash (Parallel) Converters (13.4)



- High speed – among the fastest
- 2^N comparators in parallel, each connected to different nodes – area consuming
- High power consumption
- Thermometer-code output fed into decoder
- Nands used for simpler decoding and error detection (bubble error)
- Differential comparator required to ensure sufficient PSSR
- Top and bottom resistors chosen to create the 0.5 LSB offset in an A/D converter

Flash converter



Any comparator connected to a resistor string node where V_{ri} is larger than V_{in} will have a 1 output.

One NAND-gate will have a 0 output. All other NAND-gate outputs will be 1.

This also allows for error checking by checking for more than one 0 output.

(See fig. 13.16 page 508)

Clocked CMOS comparator

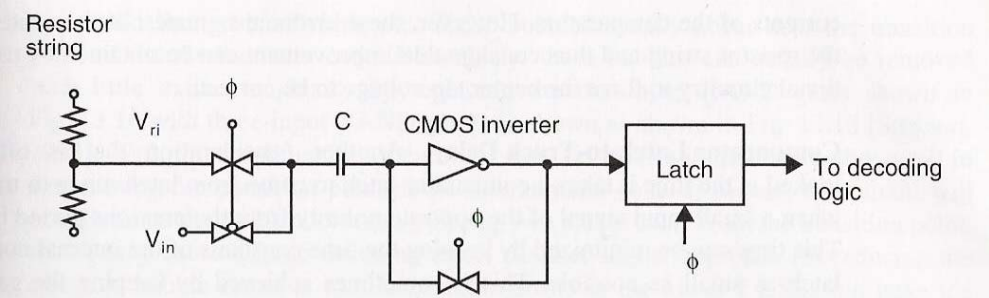


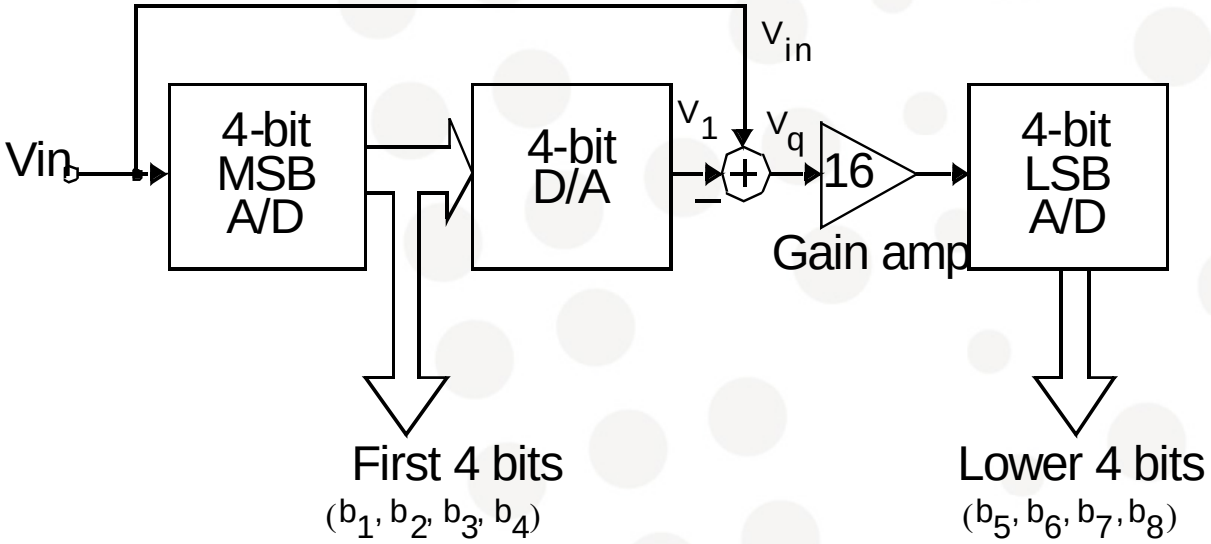
Fig. 13.17 A clocked CMOS comparator.

- When the clock (”phi”) is high, the inverter is set to its bistable point, Vin = Vout (= Vdd/2). The other (left) side of C is charged to V_{ri}.
- When the clock (”phi”) goes low, the inverter switches, depending on the voltage difference between V_{ri} and V_{in}. ($V_{ri} > V_{in}$; 1 output, $V_{ri} < V_{in}$; 0 output from inv.)
- Differential inverters helps poor PSRR with this simple comparator solution.

Issues in Designing Flash A/D Converters

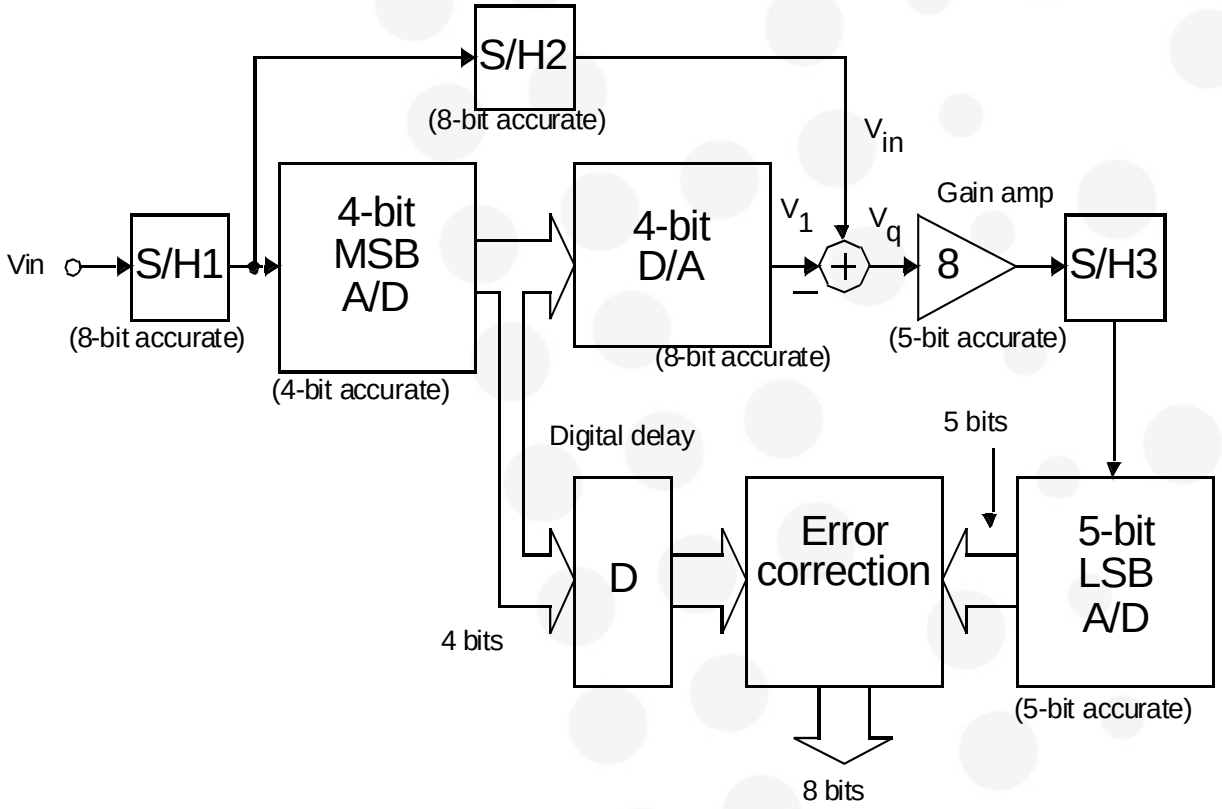
- **Input Capacitive Loading:** The large number of comparators connected to Vin results in a large capacitive load on at the input node which increases power and reduces speed
- **Comparator Latch-to-Track Delay:** The internal delay in the comparator when going from latch to track mode
- **Signal and/or Clock Delay:** Differences in signal/clock delay between the comparators may cause errors. Example: A250-MHz, 1-V peak input-sinusoid converted with 8-bit resolution requires a precision of 5ps. Can be reduced by matching the delays and capacitive loads on the signal/clock.
- **Substrate and Power-Supply Noise:** For a 8-bit converter with Vref=2V only 7.8mV of noise injection is required to introduce an error of 1LSB. The problem can be reduced by proper layout (Shielding, Differential clocks, Separate power supplies, and symmetrical layout)
- **Bubble Error Removal:** Comparator metastability may introduce wrong thermometer code (a single 1 or 0 in between opposite values)
- **Flashback:** Caused by latched comparators. When the comparator is switched from track to latch mode a charge glitch is introduced at the input. The problem is reduced by using a preamplifier and input impedance matching

Two-Step (Subranging) A/D Converters (13.5)



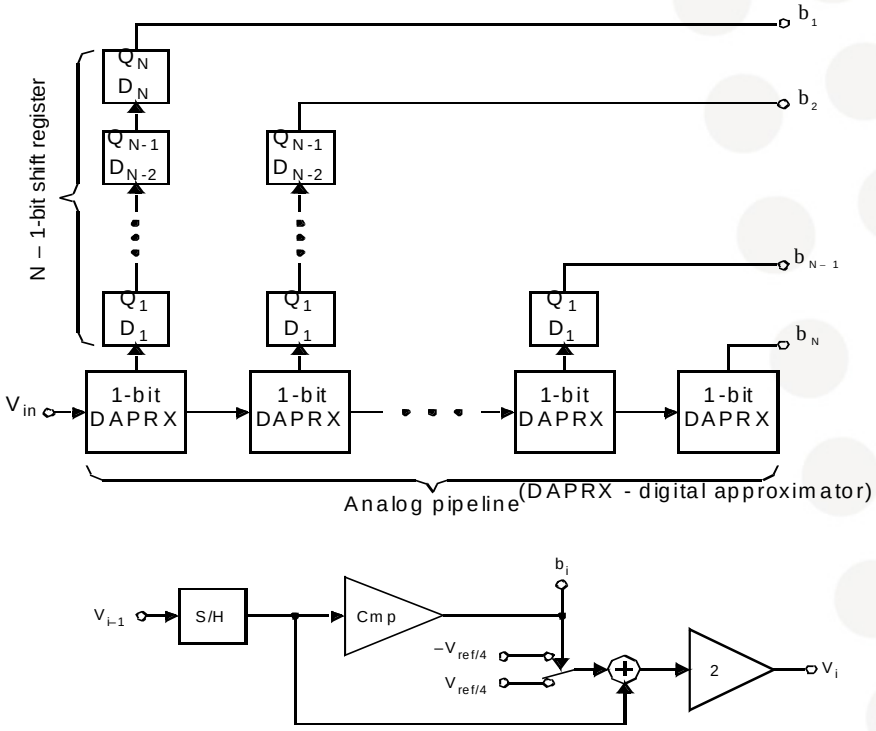
- Popular choice for high-speed medium accuracy converters (8-10 b)
- Less area and power consumption than a Flash ADC
- The MSB's are converted during the first step. In the next step the remaining error is converted into the LSB's
- Speed is limited by the Gain Amplifier
- Requires N-bit accuracy for all components (May be relaxed by using Digital Error Correction)

Digital Error Correction for two-step A/D



- The accuracy requirements on the input ADC is relaxed due to the error corr.. 4-bit for MSb converter

Pipelined ADCs (13.5) Once the first stage has completed it's work it immediately starts working on the next sample



- Small area

The pipelined ADC has its origins in the *subranging* architecture, first used in the 1950s. A block diagram of a simple 6-bit, two-stage subranging ADC is shown in Figure 11.

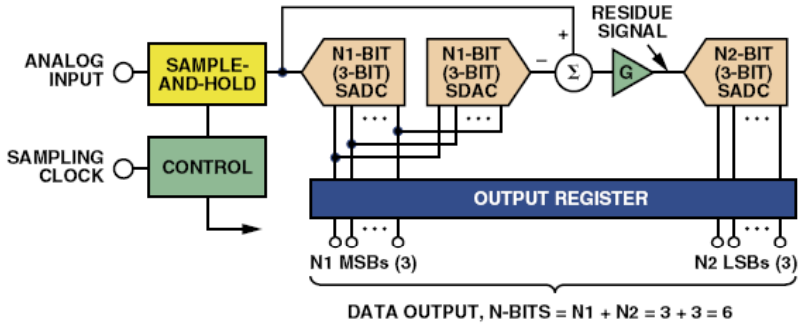
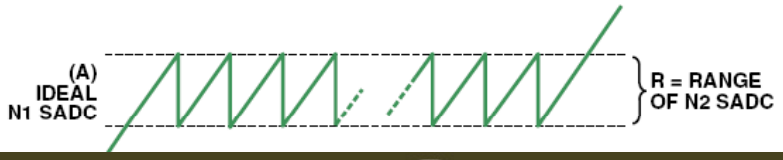


Figure 11. 6-bit, two-stage subranging ADC.

The output of the SHA is digitized by the first-stage 3-bit sub-ADC (SADC)—usually a flash converter. The coarse 3-bit MSB conversion is converted back to an analog signal using a 3-bit sub-DAC (SDAC). Then the SDAC output is subtracted from the SHA output, the difference is amplified, and this "residue signal" is digitized by a second-stage 3-bit SADC to generate the three LSBs of the total 6-bit output word.

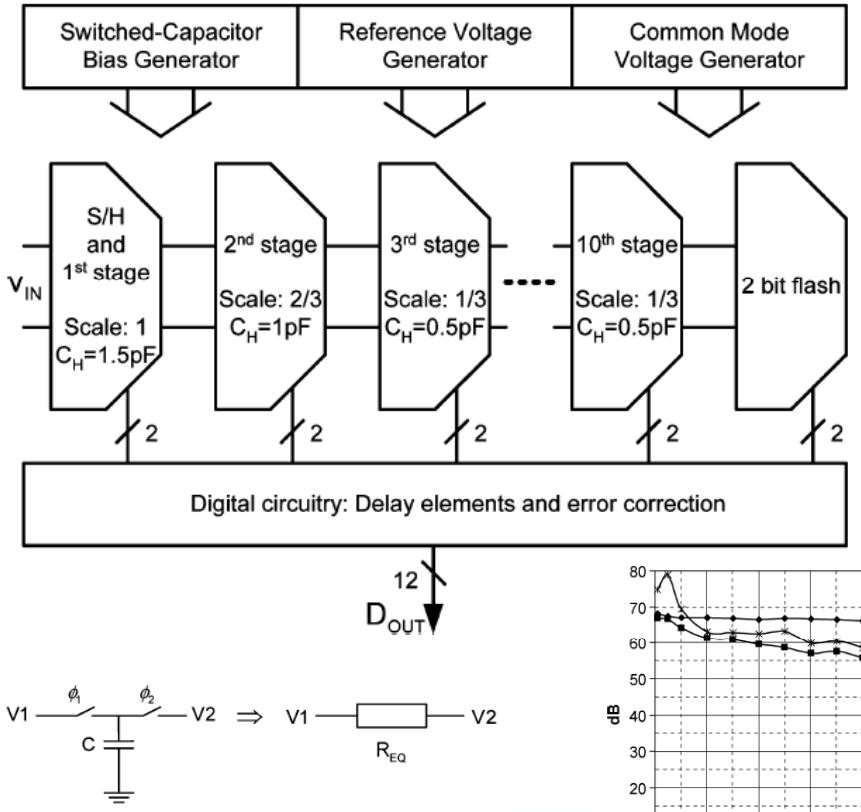


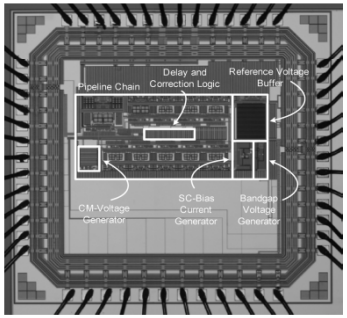
Pipelined ADC -example

IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. 40, NO. 7, JULY 2005

A Cost-Efficient High-Speed 12-bit Pipeline ADC in 0.18-μm Digital CMOS

Terje Nortvedt Andersen, Bjørnar Hernes, *Member, IEEE*, Atle Briskemyr, Frode Telstø, Johnny Bjørnsen, *Member, IEEE*, Thomas E. Bonnerud, and Øystein Moldsvor





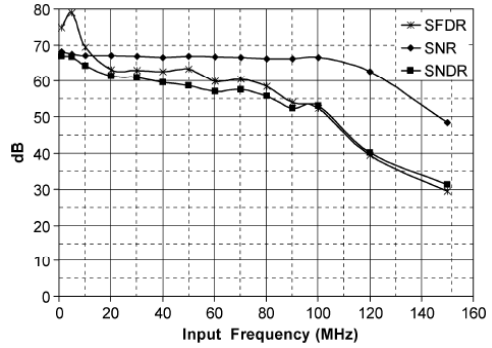


Fig. 9. SFDR, SNR, and SNDR versus input frequency. The conversion rate and signal swing are 110 MS/s and $2V_{P-P}$, respectively.

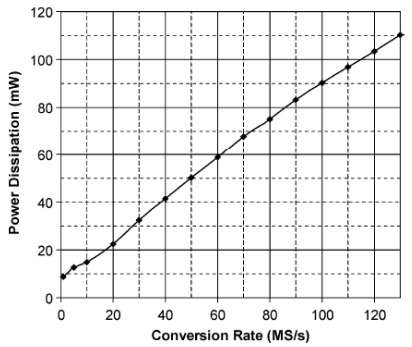


Fig. 7. Power dissipation versus conversion rate. The input frequency and signal swing is 10 MHz and $2V_{P-P}$, respectively.

Nominal sampling rate	110MS/s
Technology	0.18µm digital CMOS
Nominal supply voltage	1.8V
Resolution	12bit
Full scale analog input	$2V_{P-P}$
Area	$0.86mm^2$
Power consumption	97mW
DNL	±1.2 LSB
INL	-1.5/+1 LSB
SNR (f_{in}=10MHz)	67.1 dB
SNDR (f_{in}=10MHz)	64.2 dB
SFDR (f_{in}=10MHz)	69.4 dB
ENOB (f_{in}=10MHz)	10.4 bit

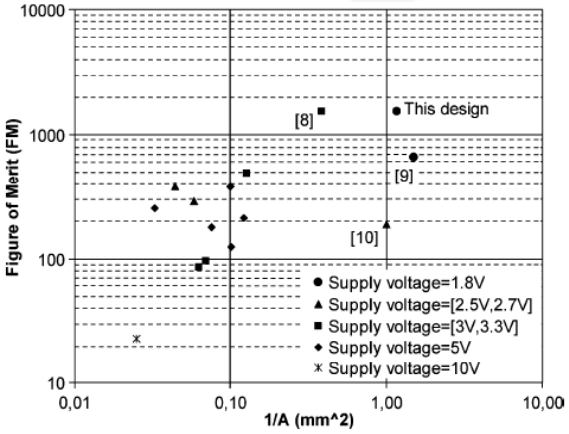
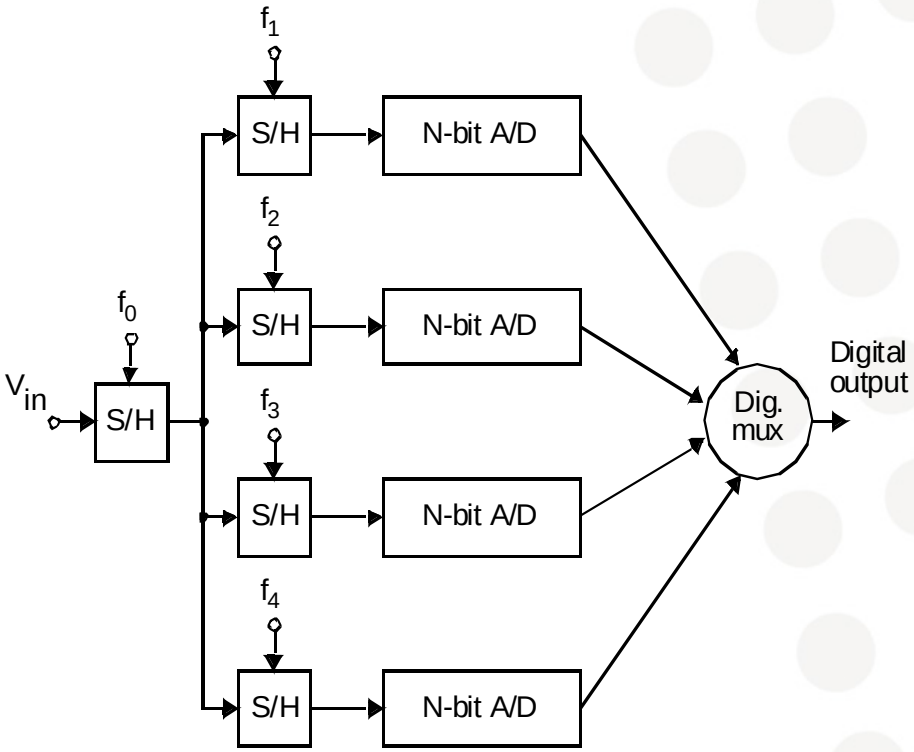


Fig. 12. Figure of Merit (FM) versus $1/A$ for 12-bit ADCs. f_{CR} is given in MS/s, A is given in mm² and P_{SUP} is given in mW.

Time-Interleaved A/D-converter (13.9)



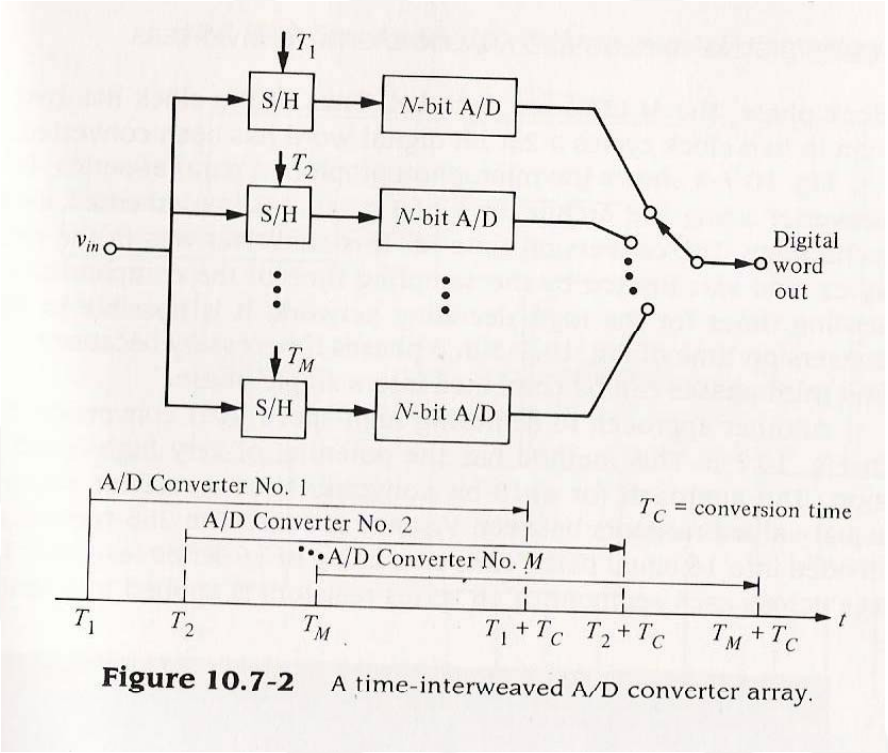


Figure 10.7-2 A time-interweaved A/D converter array.

- Very high speed (figure to the right from “Allen & Holberg”)
- f_0 is four timer higher than f_1 – f_4, which in addition is slightly delayed
- Only the S/H and the MUX must run on the highest frequency
- Tones are introduced at multiples of f_0/N

Time-Interleaved – best compromise between complexity and sampling rate – may be used for different architectures [Elbjornsson '05]

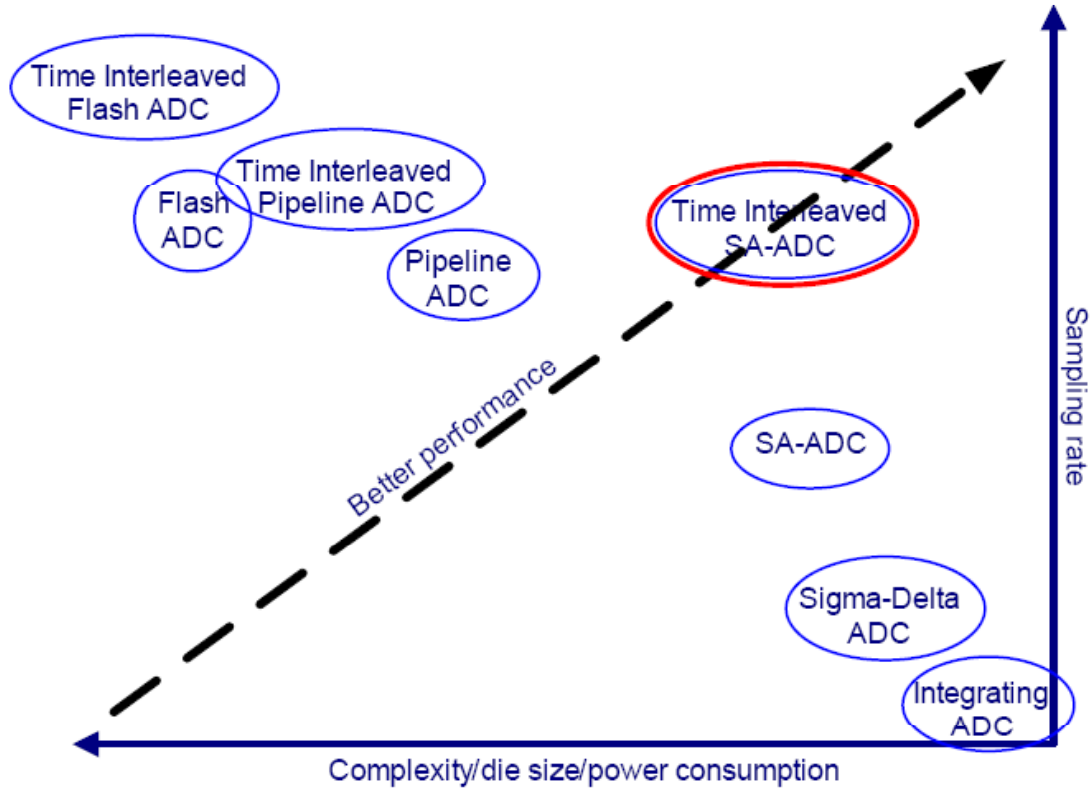
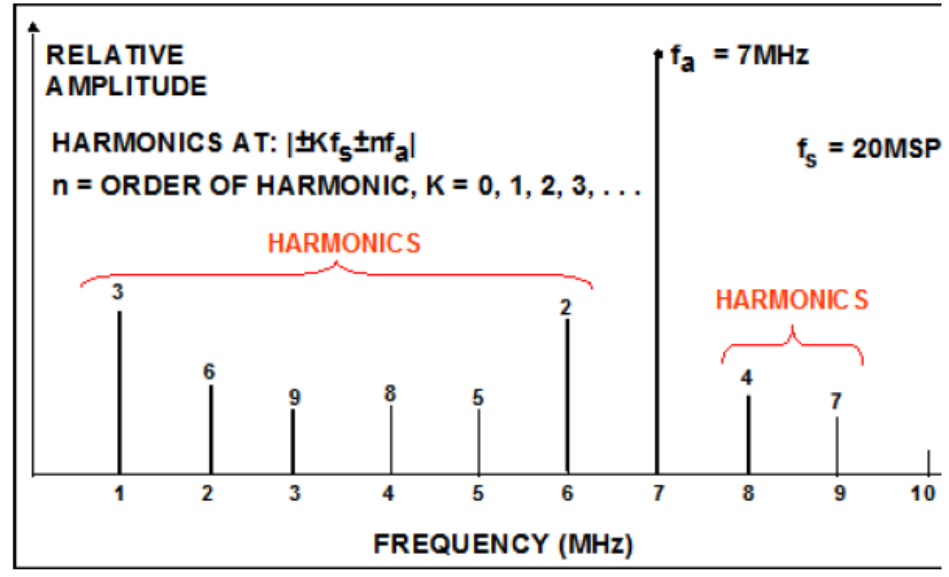


Figure 7 Comparison between ADC architectures. The time interleaved successive approximation ADC gives the best compromise between complexity and sampling rate.

Dynamic range

- Dynamic range is defined as the power of the maximum input signal range divided by the total power of the quantization noise and distortion
- Often referred to as Signal-to-Noise-and-Distortion range
- S/(N+D)
- SINAD



Analog and digital supply voltages are reduced as technology scales

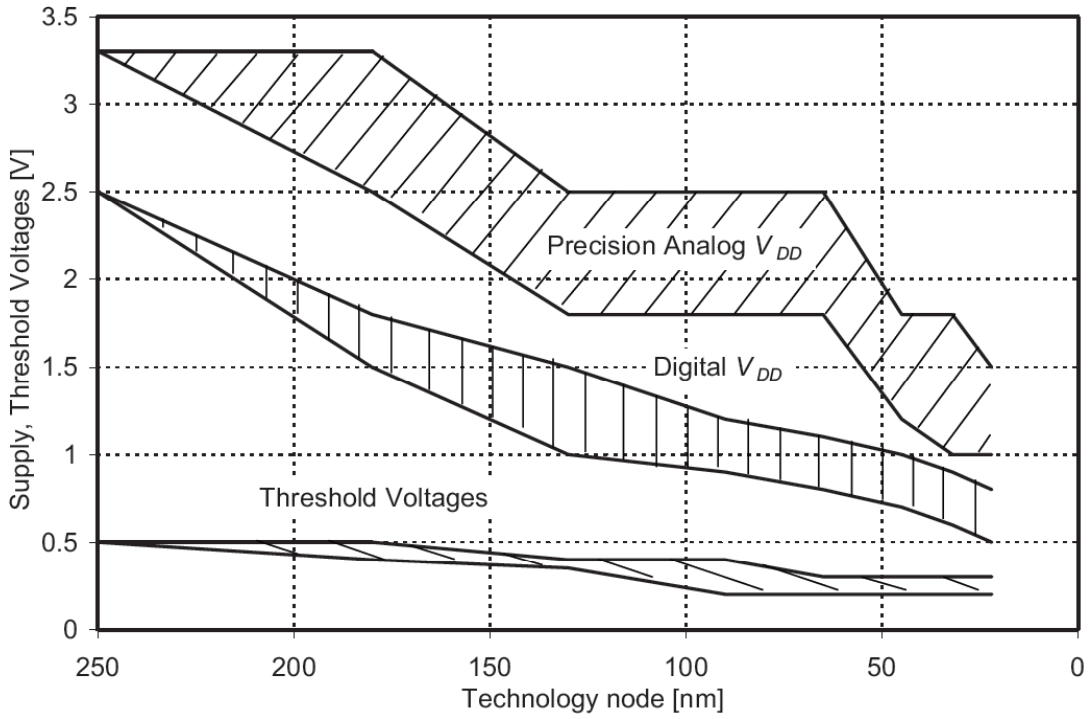


Fig. 1. Scaling of supply and threshold voltages.

Some ADC trends:

- Limited dynamic range at low supply voltages remains the utmost challenge for high-resolution Nyquist converters.
- Oversampling converters will dominate this arena in the future
- Linearity correction with digital correction is becoming prevalent

IEEE 2005 CUSTOM INTEGRATED CIRCUITS CONFERENCE

Scaling of Analog-to-Digital Converters into Ultra-Deep-Submicron CMOS

Y. Chiu [1], B. Nikolić [2], and P. R. Gray [2]

[1] Electrical and Computer Engineering, University of Illinois at Urbana-Champaign
[2] Electrical Engineering and Computer Sciences, University of California at Berkeley

Nyquist ADCs at ISSCC; FOM, Effective Number of Bits

$$\mathrm{FOM} = \frac{P}{2^{2\mathrm{ENOB}} f_s}.$$

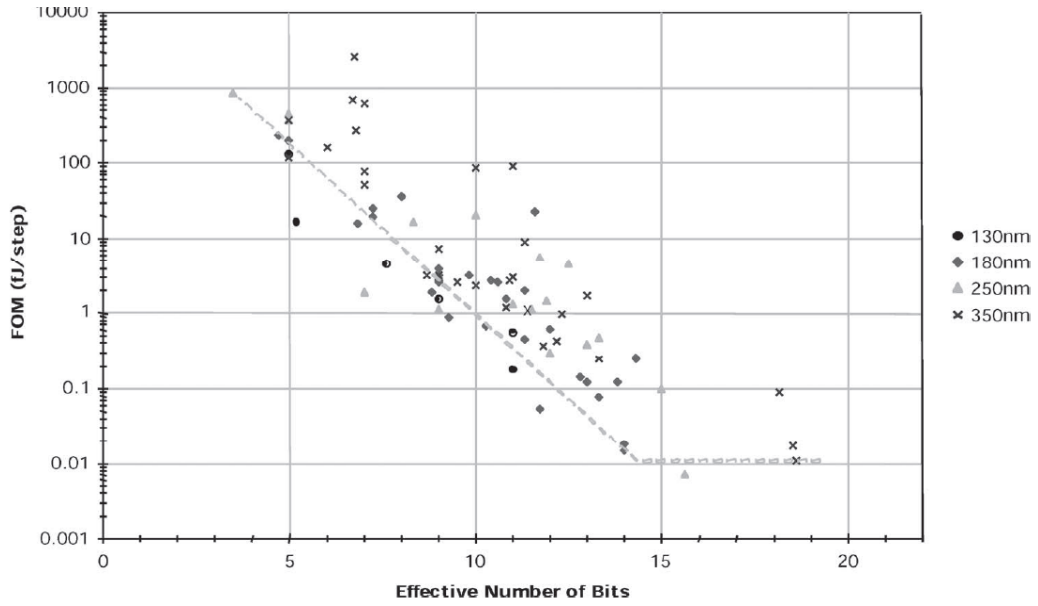


Fig. 22. ***FOM as a function of effective number of bits and technology.***

Analog Circuit Design in Nanoscale CMOS Technologies

Classic analog designs are being replaced by digital methods, using nanoscale digital devices, for calibrating circuits, overcoming device mismatches, and reducing bias and temperature dependence.

By Lanny L. Lewyn, *Life Senior Member IEEE*, Trond Ytterdal, *Senior Member IEEE*, Carsten Wulff, *Member IEEE*, and Kenneth Martin, *Fellow IEEE*

- FOM: Figure of Merit
- High-resolution conv.: FOM minimum at about 10^{-17}J/step
- 6-bit ADCs : FOM about 4 orders of magnitude worse than 14 bit converters, suggesting that there is much to be gained by designing more effecient 6-bit ADCs
- Better ENOB reported for 350 nm than 250 nm, 180 nm and 130 nm
- Data from ISSCC up to 2005.

Nyquist ADCs at ISSCC; FOM, Sampling rate

$$\mathrm{FOM} = \frac{P}{2^{2\mathrm{ENOB}} f_s}.$$

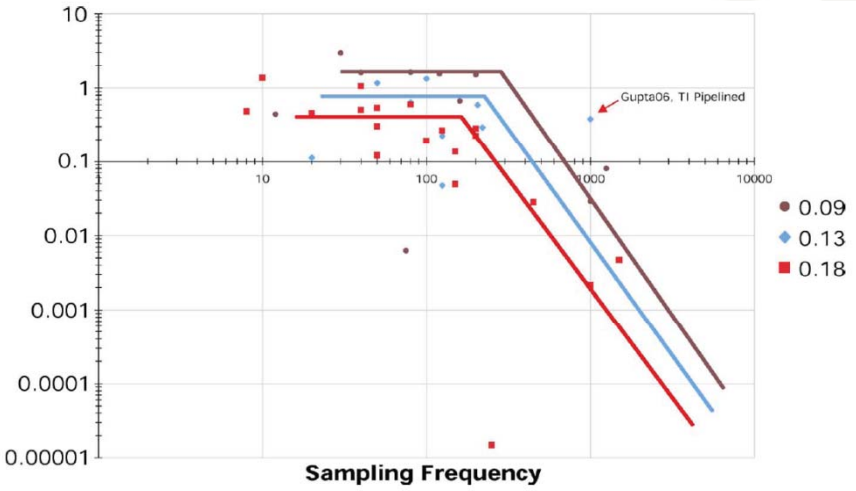


Fig. 23. *FOM cliff for Nyquist ADCs in ISSCC 2000–2007.*

Vol. 97, No. 10, October 2009 | PROCEEDINGS OF THE IEEE

- Maximum Sampling frequency (Usually faster is better) and FOM.
- ISSCC 2000-2007 (90 nm, 130 nm, 180 nm technologies)
- Small improvement in sampling frequency in going to finer technologies, mainly due to reduced capacitance.

Analog Circuit Design in Nanoscale CMOS Technologies

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Publication year	SFDR @Nyquist [dB]	ENOB @ Nyquist	Nyquist update rate, [Ms/s]	Power consumpt. [mW]	Area [mm^2]	Supply voltage [V]	Technology [nm]	other	Reference
2006	55	8.5	1000	250	3.5	1.2	130	Time interleaved	Gupta et al IEEE JSSC '06
2007		4	2500	24	0.057	1.2	130	"Pipelined flash"	Wang et al, IEEE Trans. Instr. Meas.
2007		5	500	6	0.9	1.2	65	Time interleaved succ. approx	Ginsburg et al IEEE JSSC '07
2007		8	100	30	2.04	1.0	180	Switched opamp pipelined	Wu et al, IEEE JSSC '07
2008		10	30	22	0.7	1.8	180	pipelined	Li et al, IEEE JSSC '08
2009	81	13		0.073		0.7	180	Delta-sigma	Chae, JSSCC Feb.09
2009	27.5	4.3	1750	2.2	0.02	1.0	90	"folding flash"	Verbruggen, JSSCC, Mar. '09
2009	10		1.2	12.2	0.354	3.3	350	Continous time sigma delta	TCAS-II, Jan. '09

Sampling-time uncertainty

•Variation in output voltage caused by variations in the time of sampling

Consider the following input signal: $V_{in} = \frac{V_{ref}}{2} \sin(2\pi f_{in} t)$

If the variation in sampling time is Δt , following equation must be satisfied to keep ΔV less than 1LSB

$$\Delta t < \frac{V_{LSB}}{\pi f_{in} V_{ref}} = \frac{1}{2^N \pi f_{in}}$$

Additional litterature

- Phillip E. Allen, Douglas Holberg: CMOS Analog Circuit Design, Holt Rinehart Winston, 1987.
- Jonas Elbornsson: White paper on parallel successive approximation ADC, Mathcore Engineering AB, 2005.
- R. Gregorian, G. Temes: Analog MOS Integrated Circuits for Signal Processing, Wiley, 1986
- D. M.Gingrich Lecture Notes, University of Alberta, Canada http://www.piclist.com/images/ca/ualberta/phys/www/http/~gingrich/phys395/notes/phys395.html
- Walt Kester: Which ADC is right for your application?
- Y. Chiu, B. Nicolic, P. R. Gray: Scaling of Analog-to-Digital Converters into Ultra-Deep-Submicron CMOS, Proceedings of Custom Integrated Circuits Conference, 2005.
- Lecture Notes, University of California, Berkeley,

  EE247 Analog Digital Interface Integrated Circuits, Fall 07;http://inst.eecs.berkeley.edu/~ee247/fa07/
- Lanny L. Lewyn, Trond Ytterdal, Carsten Wulff, Kenneth Martin: ”Analog Circuit Design in Nanoscale CMOS Technologies”, Proceedings of the IEEE, October 2009.
- James L. McCreary, Paul R. Gray: ”All-MOS Charge Redistribution Analog-to-Digital Conversion Techniques – part 1”, IEEE Journal of Solid-State circuits, December 1975.


IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. 40, NO. 7, JULY 2005

A Cost-Efficient High-Speed 12-bit Pipeline ADC in 0.18-μm Digital CMOS

Terje Nortvedt Andersen, Bjørnar Hernes, *Member, IEEE*, Atle Briskemyr, Frode Telstø, Johnny Bjørnsen, *Member, IEEE*, Thomas E. Bonnerud, and Øystein Moldsvor

Next Tuesday (10/3-08):

Rest of chapter 13.

- Chapter 14 Oversampling Converters

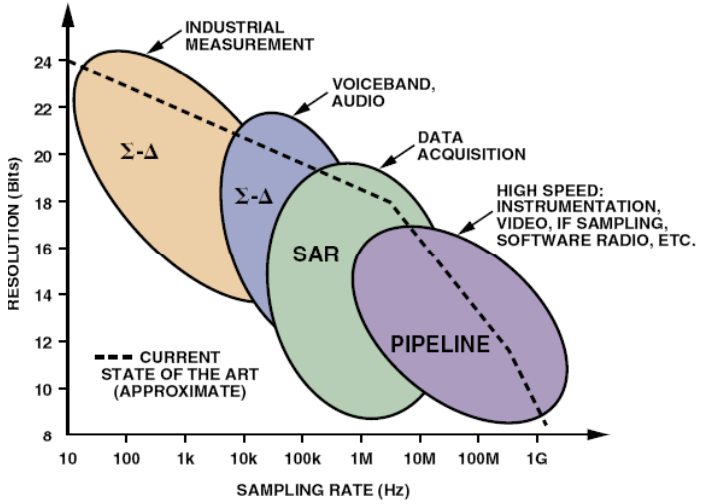


Figure 1. ADC architectures, applications, resolution, and sampling rates.

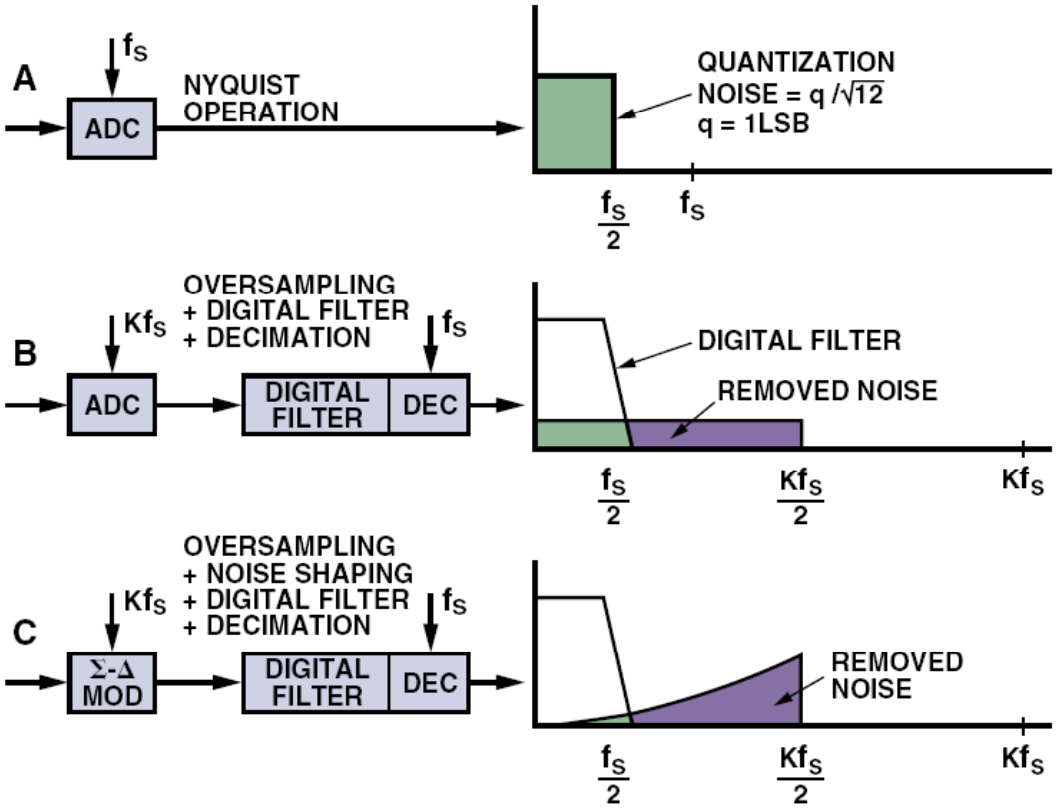
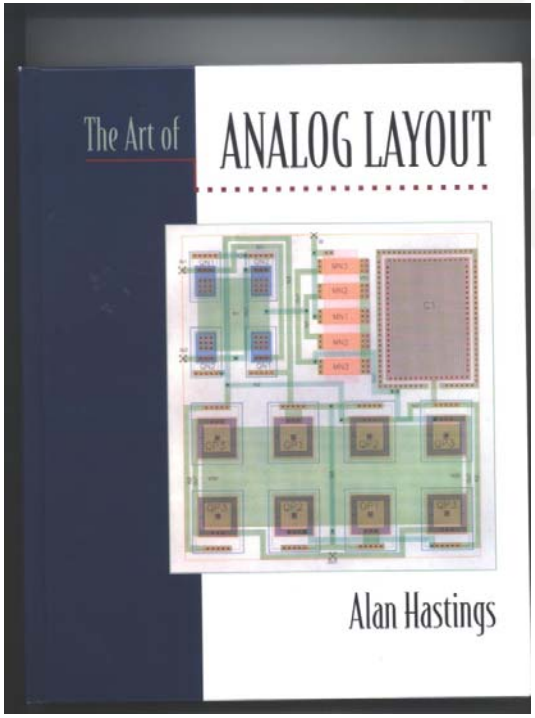
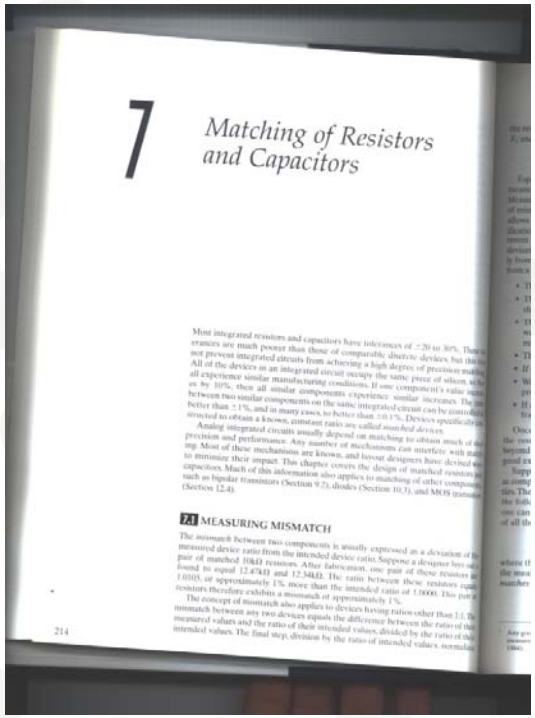


Figure 6. Noise-spectrum effects of the fundamental concepts used in Σ-Δ: oversampling, digital filtering, noise shaping, and decimation.

Analog Layout - mismatch

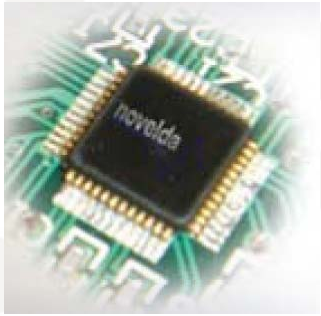




- *"…The ratio between two similar components on the same integrated circuit can be controlled to better than +/- 1 %, and in many cases, to better than +/- 0.1 %. Devices specifically constructed to obtain a known, constant ratio are called matched devices.*"
- "Matching – the Achilles Heel of Analog" (Chris Diorio)

Some companies located in Norway, doing (or that have done) full custom data converter designs:

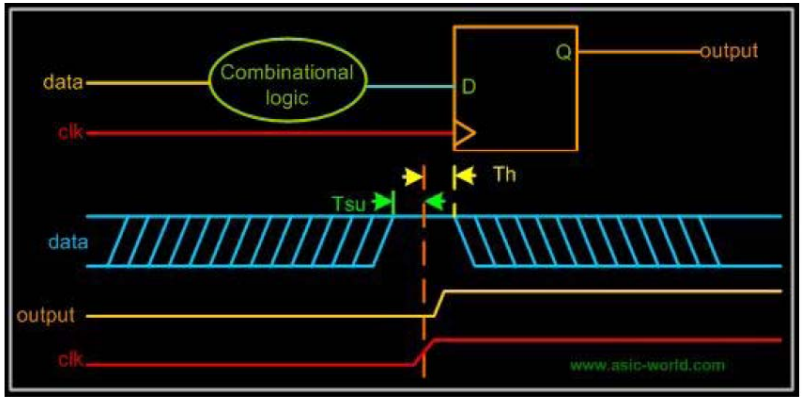
- Analog Concepts (Trondheim)
- Arctic Silicon Devices (Trondheim)
- Atmel Norway (Trondheim)
- Energy Micro (Oslo)
- GE Vingmed Ultrasound (Horten)
- Nordic Semiconductors (Trondheim, Oslo)
- Novelda (Oslo)
- Micrel (Oslo)
- Sintef (Trondheim, Oslo)
- Texas Instruments (Oslo)



Metastability in FFs (http://www.asic-world.com/tidbits/metastablity.html) To avoid M. in comparators: Make gain high, increase current levels.

What is metastability?

Whenever there are setup and hold time violations in any flip-flop, it enters a state where its output is unpredictable: this state is known as metastable state (quasi stable state); at the end of metastable state, the flip-flop settles down to either '1' or '0'. This whole process is known as metastability. In the figure below Tsu is the setup time and Th is the hold time. Whenever the input signal D does not meet the Tsu and Th of the given D flip-flop, metastability occurs.



When a flip-flop is in metastable state, its output oscillate between '0' and '1' as shown in the figure below (here the flip-flop output settles down to '0') . How long it takes to settle down, depends on the technology of the flip-flop.

The approximate equation which describes the output voltage, $V_O(t)$ is given by:

$$V_O(t) = \Delta V_{IN} A e^{t/\tau}, \qquad \text{Eq. 1}$$

where ΔV_{IN} = the differential input voltage at the time of latching, A = the gain of the preamp at the time of latching, τ = regeneration time constant of the latch, and t = the time that has elapsed after the comparator output is latched (see References 2 and 3).

For small differential input voltages, the output takes longer to reach a valid logic level. If the output data is read when it lies between the "valid logic 1" and the "valid logic 0" region, the data can be in error. If the differential input voltage is exactly zero, and the comparator is perfectly balanced at the time of latching, the time required to reach a valid logic level can be quite long (theoretically infinite). However, comparator hysteresis and input noise makes this condition highly unlikely. The effects of invalid logic levels out of the comparator are different depending upon how the comparator is used in the actual ADC.

From a design standpoint, comparator metastability can be minimized by making the gain (A) high, minimizing the regeneration time constant (τ) by increasing the gain-bandwidth of the latch, and allowing sufficient time (t), for the output of the comparator to settle to a valid logic level. It is not the purpose of this discussion to analyze the complex tradeoffs between speed,