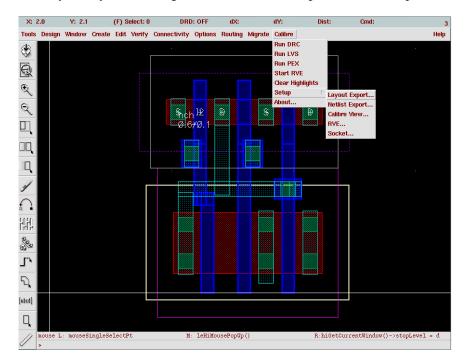
## Some Remarks about LVS

If you are using the resistor/capacitor models provided by TSMC in your schematic design you can't generate the complete netlist without adding an additional source file, see below and read the "README\_calibre" in the lvs folder for more information.



1) In your layout editor, go to 'Calibre' -> 'Setup' -> 'Netlist Export', see the following figure.

 Add the "source\_added" file (which is inside the lvs folder) to the item "Include File", see the following figure. To be safe, put the whole path here, for example, "/ifi/utgard/a27/iam ABC/cadence/test123/Calibre/lvs/source\_added"

Calibre Netlist Export Set	up X
OK Cancel	Help
Template File:	Ĭ.
	Load Save
View Name	schematiď
Simulator	auCdlį
View List	auCdl schematig
Stop List	auCdl
Equivalents	Į.
Connects	<u>                                     </u>
Include File	YOUR PROJECT FOLDER DIRECTOY/Calibre/lvs/source_added
Check LDD	

"/ifi/utgard/a27/iamABC/cadence/test123/Calibre/lvs/source\_added"

3) Run the LVS.

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