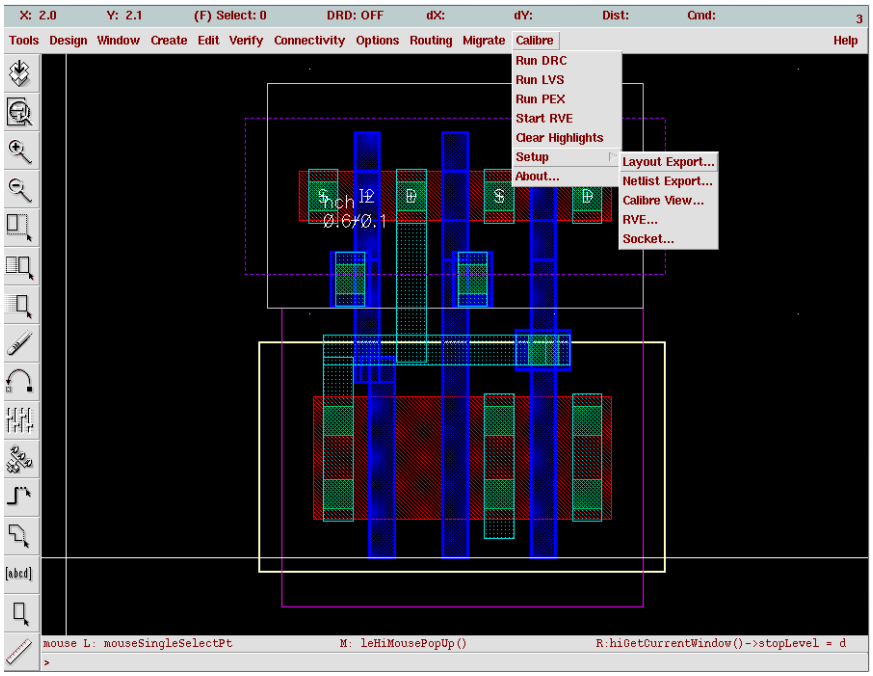
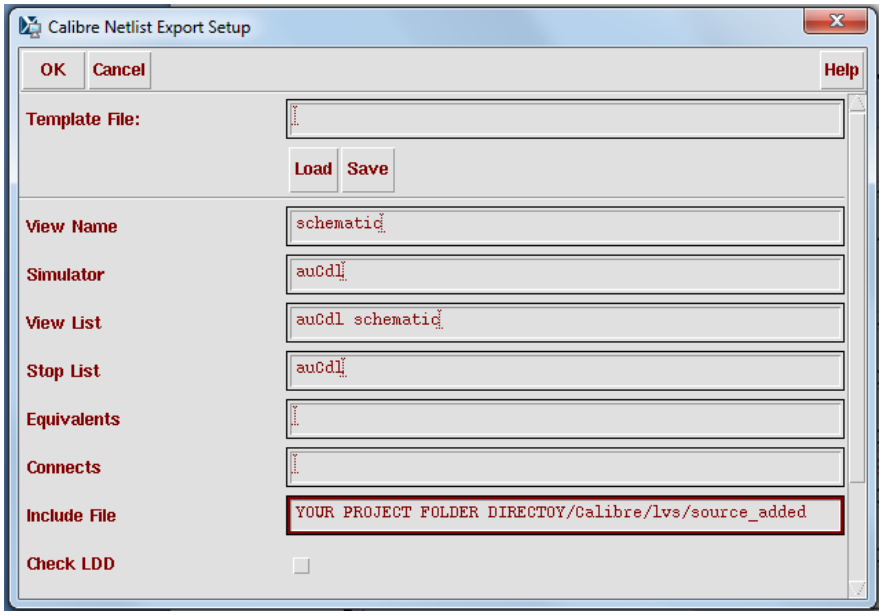
Some Remarks about LVS

If you are using the resistor/capacitor models provided by TSMC in your schematic design you can't generate the complete netlist without adding an additional source file, see below and read the "README_calibre" in the lvs folder for more information.

1) In your layout editor, go to ‘Calibre’ -> ‘Setup’ -> ‘Netlist Export’, see the following figure.



2) Add the “source_added” file (which is inside the lvs folder) to the item “Include File”, see the following figure. To be safe, put the whole path here, for example, “/ifi/utgard/a27/iamABC/cadence/test123/Calibre/lvs/source_added”



3) Run the LVS.

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