UiO : Department of Informatics
University of Oslo

INF4420

Introduction

Spring 2012

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Outline

Practical information about the course.

Context (placing what we will learn in a larger context)

Outline of the curriculum.

Lectures

Jørgen Andreas Michaelsen
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Lectures on mondays in OJD 2453, Perl

Problem solving class

Kin Keung Lee (Kody)
Room: 5122, Phone: 22840136
Email: kklee@ifi.uio.no

Assignments for each week (not mandatory)
Fridays in OJD 2465, Prolog

Labs

Weekly labs to learn design tools

Details are not yet available ...

Webpage

Course webpage:
http://www.uio.no/studier/emner/matnat/ifi/INF4420/v12/

important mesages will be posted on the course webpage. Slides for the lectures and assigments for the problem solving class are posted.

Teaching and examination

Lectures (2-3 hours)
Problem solving class (2 hours)
Lab exercises (2 hours)

4 hour written exam (60 %)
Project (design, layout, 40 %)

Course content

From the course webpage:

"The course provides the know-how and skills needed to design analogue and mixed-signal integrated circuit modules using modern program tools. The main focus of the course is complex systems such as data converters (A/D, D/A) and phase-locked loops (PLL). An introduction is given to CMOS technology and methods in order to implement passive components such as transistors, condensers and coils. In addition, matching, optimisation and noise deflection are all key aspects. The execution of project tasks will be a central part of the teaching."

Learning outcomes

From the course webpage:

"Students will have the skills needed to design an integrated mixed-signal circuit in CMOS using modern design tools."

Student reference group

1 or 2 students

What is expected of you?

Basic understanding of analog CMOS (INF3410). We will build on this for most of the circuits and systems we discuss. Linear circuits (transfer functions, Laplace).

Important to ask questions.

Integrated circuits

Integrated circuits are found everywhere in our daily lives.

Cost is a driver. Reduced feature size, smaller dies, CPF decreases, more features on the same die (SoC). Larger wafers.

Reduced feature size also helps performance. Is scaling good for analog?

Mixed-signal in DSM

Digital content dominate. Process development is geared towards reducing cost-per-function (CPF).

Analog and RF functions have to keep up (cost benefits of placing all functions on one die)

Mixed-signal circuits

What are mixed-signal circuits?

Analog + Digital?

Time/Value	Discrete	Continuous
Discrete	Digital	?
Continuous	?	Analog

Why mixed-signal circuits?

Digital circuits are more robust and can be designed more systematically. Usually, most of the system and signal processing will be digital content.

We need circuits for regulating supply voltage, clocking digital circuits, interfacing with the (analog) world (filtering and converting to/from digital), communication circuits.

Uses of mixed-signal

Analog and mixed-signal circuits are prevalent even in "digital" systems

- clocking and timing circuits
- digital i/o (high speed bus)
- supply voltage regulation
- wireless communication
- sensor interfacing
- ...

Mixed-signal in DSM

New ideas and different designs are needed to keep up with new process technology, and new trends (e.g. portable applications).

Important to have a good understanding of analog and mixed-signal circuits. Know what the limitations are and what can be improved.

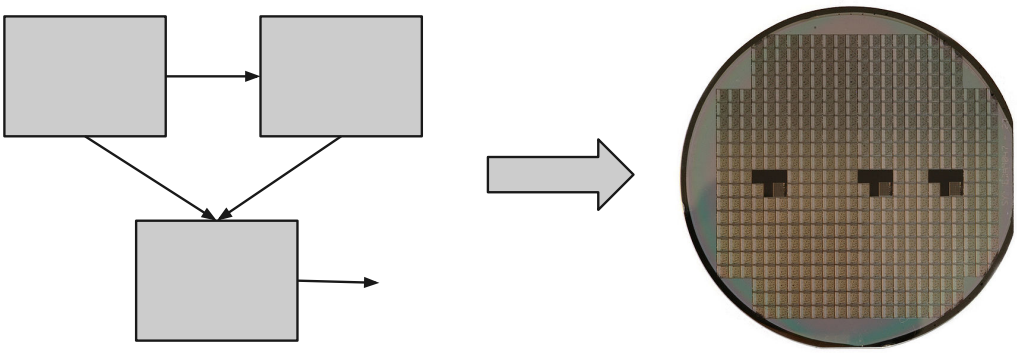
DALLAS, Aug. 23 /PRNewswire/ -- Texas Instruments Incorporated (TI) (NYSE: TXN) today introduced a dual-channel, single-lane serial-ATA (SATA) redriver and signal conditioner, featuring the lowest active power and lowest automatic low-power (ALP) mode of any 6-Gbps redriver/equalizers available today. The SN75LVCP601 has a maximum active power consumption of 290 mW, or approximately 50 percent less than the nearest competitor, extending critical battery life in portable electronics, such as notebook PCs. ...

Design flow

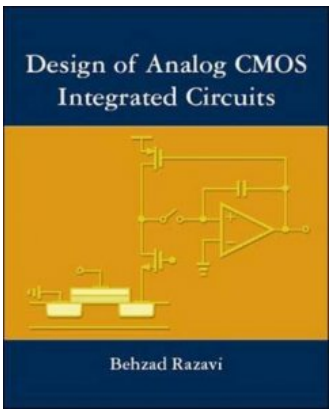
Top-down design
Specification + different levels of abstraction
Meeting specs accross PVT with min power
Usually, big savings are in the architecture

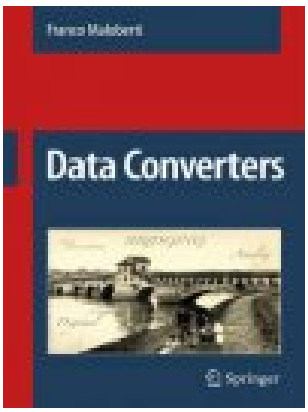
Levels of abstraction

System level (block diagrams, MATLAB)
Schematics (SPICE)
Layout (CAD, DRC, ERC, LVS)



Curriculum

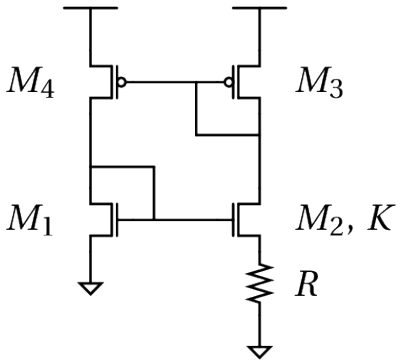


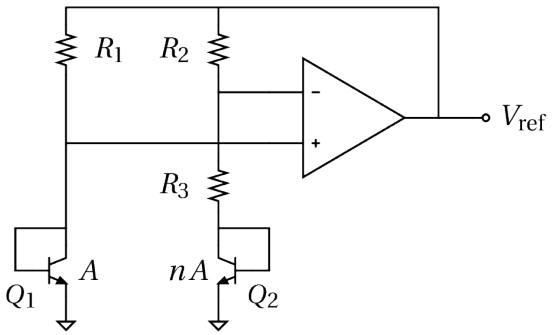


http://www.springerlink.com/content/l30184/#section=342950&page=1

Reference circuits

Every analog and mixed signal circuit needs biasing and/or a reference independent of PVT.





Layout and mismatch

Drawing layout needs careful attention in order to get predictable results.

Ensuring drawn layout is manufactureable (DRC).

Ensuring drawn layout is coherent with schematics (LVS, post layout simulation, but this does not reveal every problem, assumptions made by schematics)

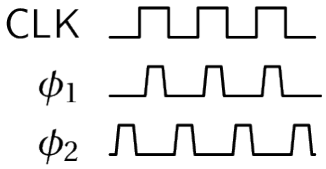
Ensuring drawn layout is robust against manufacturing imperfections.

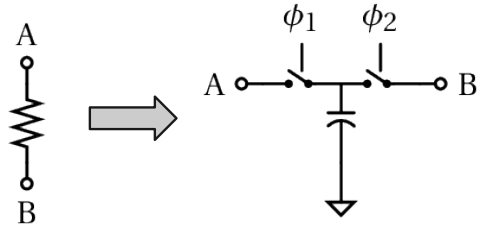
Switched capacitor

Very important technique for analog signal processing. Discrete time, continuous value.

$$I_{\text{avg}} = C \cdot \frac{V_A - V_B}{T}$$

$$R_{\text{eq}} = \frac{T}{C}$$





Data converters

Converting between analog and digital representations of the signal.

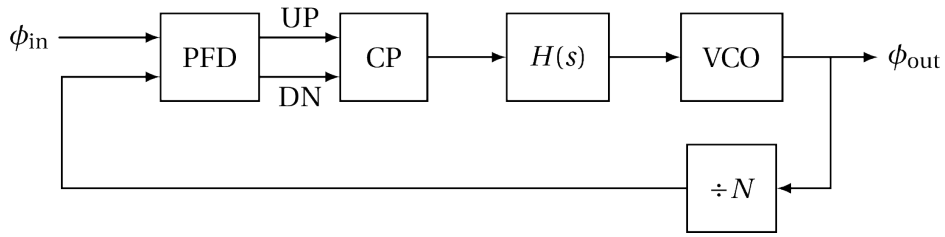
General data converter considerations

Different architectures suited to different specifications (speed, resolution).

Oversampling and noise shaping

Oscillators and PLLs

Clock and data recovery (from serial data)
Clock generation (from external crystal reference)
Demodulation (e.g. frequency modulated signals)



Project

Counts 40 % towards the final grade
Final report is *very* important

Last year: SAR ADC
This year: Bandgap + Current steering DAC

Work in groups of two
Kody will follow up on the project
More details to follow

Design tools

Hands on with high quality IC design tools in the labs and for completing the project.

Virtuoso IC6.1.4 (Cadence)
Virtuoso Spectre 7.2.0 (Cadence)
Calibre 2010.3 (Mentor Graphics)

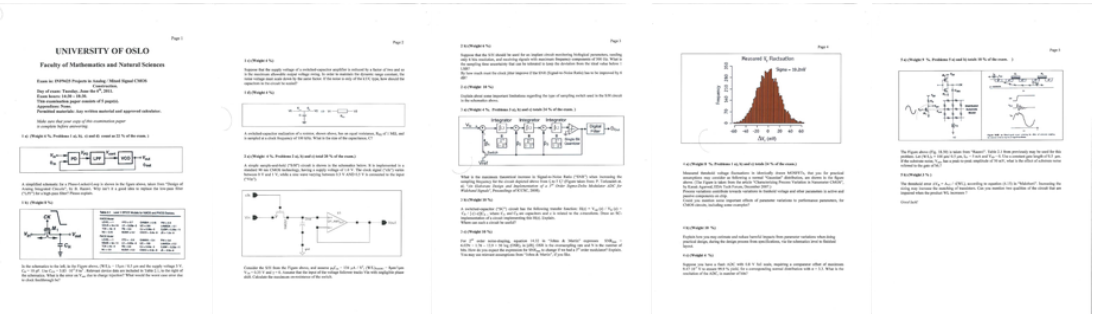
Process design kit (PDK)

TSMC 90 nm MS/RF LP 1.2 V with 2.5 V I/O
http://www.europractice-ic.com/technologies_TSMC.php?tech_id=90nm

Provides simulation models
PCells for generating component layout
Rule decks for DRC, ERC, and LVS

Final exam

7. June, 14:30, 4 hours written exam
Counts 60 % towards the final grade.



Schedule

Dato	Undervises av	Sted	Tema	Kommentarer / ressurser
16.01.2012	Jørgen	OJD 2453 Perl	Introduction	
23.01.2012	Jørgen	OJD 2453 Perl	Reference circuits	
30.01.2012	Jørgen	OJD 2453 Perl	Short-channel and layout	
06.02.2012	Jørgen	OJD 2453 Perl	Short-channel and layout	
13.02.2012	Jørgen	OJD 2453 Perl	Mismatch and non-linearity	
20.02.2012	Jørgen	OJD 2453 Perl	Switched capacitor	
27.02.2012	Jørgen	OJD 2453 Perl	Switched capacitor	
05.03.2012	Jørgen	OJD 2453 Perl	Data converters	
12.03.2012	Jørgen	OJD 2453 Perl	Data converters (DAC)	
19.03.2012	Jørgen	OJD 2453 Perl	Data converters (ADC)	
26.03.2012	Jørgen	OJD 2453 Perl	Data converters (Oversampling)	
02.04.2012				Easter (no lecture)
16.04.2012	Jørgen	OJD 2453 Perl	Data converters	
23.04.2012	Jørgen	OJD 2453 Perl	Oscillators	
30.04.2012	Jørgen	OJD 2453 Perl	PLLs	
07.05.2012	Jørgen	OJD 2453 Perl	Project presentations	
14.05.2012	Jørgen	OJD 2453 Perl	Repetition	

References

In addition to the curriculum, these references have been consulted when preparing the lectures.

CMOS: Circuit design, Layout, and Simulation (Baker, IEEE Press).

Analog Design Essentials (Willy Sansen, Springer).

IDESA (www.idesa-training.org/About.html)

Analog Integrated Circuit Design (Johns and Martin, Wiley).

Next lecture

23. January

Reference circuits ("Bandgaps")