UiO : Department of Informatics
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Short-channel effects and models

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Outline

MOSFET scaling

Short-channel effects

MOSFET models

Introduction

Scaling continues for the benefit of digital.

For analog this is not neccessarily beneficial, but desirable to have everything on one die (SoC).

Designing ananlog and mixed-signal circuits, we need to be aware of the implications so that we can design circuits that perform well despite short-channel effects.

Why CMOS scaling?

Reducing feature size is very attractive for digital circuits

- Higher density (lower cost)
- Reduced power consumption
- Faster (less capacitance)

Why CMOS scaling?

Can be beneficial for analog, depending on the application

- Reduced Vdd, increased current
- Gain is low because because output resistance is decreased
- Higher speed (ft) opens up for new applications in CMOS (e.g. mm-wave)

Short- vs long-channel

A loose definition: Typically, a long-channel device will behave according to the square-law model

$$I_D = \frac{\mu_n C_{\text{ox}}}{2} \frac{W}{L} (V_{\text{GS}} - V_{\text{TH}})^2 (1 + \lambda V_{\text{DS}}) \quad \text{(sat.)}$$

The behaviour of a short-channel device will not be accurately predicted by the square-law model

Long-channel transistor

Gate has good control over channel

Square-law equations are sufficiently accurate for predicting drain current.

Short-channel transistor

Drain region has more influence on channel behaviour

Short-channel effects become significant.

Constant field scaling

Parameter	Scaling
W	α^{-1}
L	α^{-1}
V	α^{-1}
$\mathbf{E}$	1
t_{ox}	α^{-1}
N_a	α
C_{ox}	α
I_{on}	α^{-1}
t_d	α^{-1}
P	α^{-3}

Constant field (E)

Full-node $\alpha \approx \sqrt{2}$

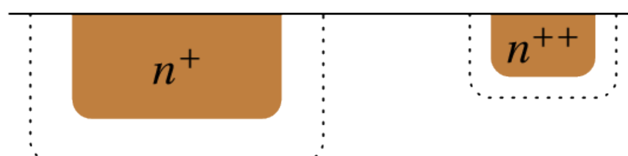
Constant field scaling

P=F*C*Vdd^2

Similar for SD depletion capacitance

$$I_{D,\alpha} = \frac{\mu_n C_{ox}}{2\alpha} \frac{W}{L} (V_{GS} - V_{TH})^2$$

$$C_{ch,\alpha} = \frac{W L C_{ox}}{\alpha}$$



Constant field scaling

Implications for analog. gm and ro does not change.

However, kT/C is the noise floor. Lower Vdd requires larger C to maintain SNR. Larger current needed to drive C.

$$g_{m,\alpha} = \mu_n C_{\text{ox}} \frac{W}{L} (V_{\text{GS}} - V_{\text{TH}})$$

$$r_{O,\alpha} = \frac{1}{\lambda I_D}$$

Constant voltage scaling

Parameter	Const. field Scaling	Const. volt Scaling
W	α^{-1}	α^{-1}
L	α^{-1}	α^{-1}
V	α^{-1}	1
$\mathbf{E}$	1	α
t_{ox}	α^{-1}	α^{-1}
N_a	α	α
C_{ox}	α	α
I_{on}	α^{-1}	α
t_d	α^{-1}	α^{-2}
P	α^{-3}	α^{-1}

Practical scaling

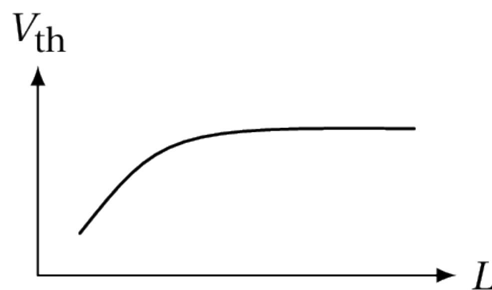
Practical issues makes scaling less than ideal

tox scaling leads to reliability concerns and gate current tunneling.

Practical limit to reducing Vdd and Vth, and Vdd/Vth-ratio decreases

Devices must handle higher fields

Charge sharing



HALO implants

Used to make threshold voltage more constant vs. gate length. Non-uniform channel doping. Reverse short channel effect (RSCE). Overcompensating droop in threshold voltage results in increasing threshold voltage with shorter gate lengths.

Trade-off Ion/Ioff (digital) vs. gain (analog). Halo reduces Ro. DITS (Drain-Induced Threshold Shift)

Vertical field

Higher gate channel field pulls carriers closer to the oxide interface.

Degrades effective mobility.

Effective mobility becomes a function of Vgs (mobility reduces with increasing Vgs)

Velocity saturation

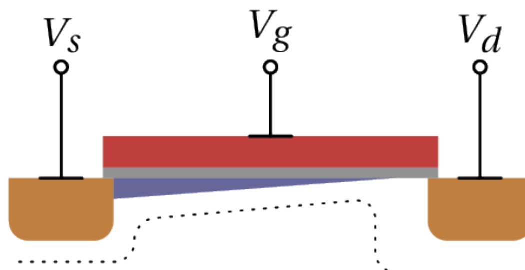
Increasing Vds will increase the electric field in the channel. If field is too large, velocity will saturate (vsat = 10^7 cm/s).

$$v = \mu_n E \quad \left[\frac{\text{m}}{\text{s}}\right]$$

$$I_D = W C_{\text{ox}} v_{\text{sat}} (V_{\text{GS}} - V_{\text{TH}})$$

Channel length modulation

Channel length modulation (CLM) is present even in long-channel transistors, but less prominent. Pinch-off changes with Vds.



DIBL

Drain induced barrier lowering

Drain voltage (Vd) contributes to inverting the channel, effecively reducing Vth. Increasing current with increasing Vd

Hot carriers

Velocity overshoot due to high electric field from source to drain.

Impact ionization near drain, electron hole pair.

Carriers may get trapped in the gate oxide.

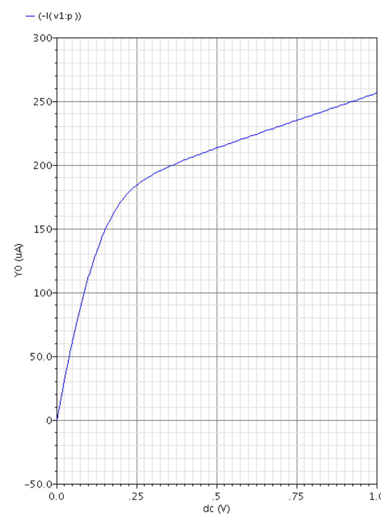
SCBE

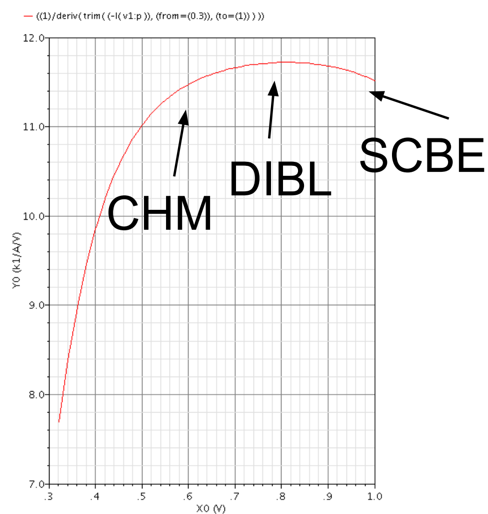
Substrate current induced body effect

Electron hole pair from impact ionization generates a drain substrate current. Current will increase exponentially with drain voltage

Substrate resistance IR drop.

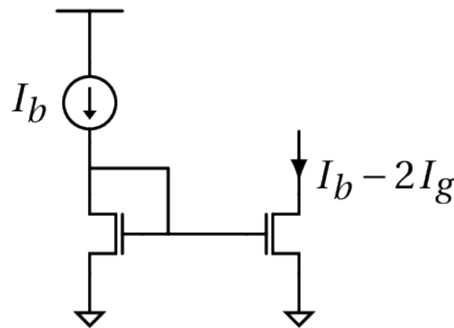
Short channel Ro





Gate tunneling current

Thinner gate oxide increases probability of carriers tunneling through the oxide. Also GIDL (Gate induced drain leakage) ...



MOSFET device models

As circuit designers we need to accurately predict circuit performance. Circuit simulators can use much more sophisticated device models than we use for hand calculation and analysis.

As technology scale, models evolve to take new effects into account in order to predict device behaviour with sufficient accuracy.

Shichman Hodges Model

Also known as a "level 1 model" because of SPICE.

Approximately the simple equations we use for hand analysis of circuits. (Id and capacitance).

Usually not sufficiently accurate, except for several um gate length techology.

BSIM

Berkeley Short-Channel IGFET Model

BSIM3v3 1995
BSIM4 2000 (currently BSIM4.7.0, 2011)

BSIM4 includes all short channel effects we have discussed. Significantly better Ro prediction (which has been a problem).

BSIM

Increasing number of non-physical parameters to fit measured device characteristics.

Finding parameters to accurately model devices is challenging.

Currently more than 200 parameters (binning, and several transistor flavours in one process).

Binning and corners

Different sets of parameters for different device sizes (binning). Simulator selects parameter set automatically.

Different sets of parameters for process corners (FF, SS, FS, SF). Statistical parameters for monte-carlo analysis.

EKV model

Charge-based compact model. Not widespread adoption for simulation, but can be useful for hand analysis.

Possible to extract parameter set e.g. from BSIM parameters supplied by the foundry.

PSP MOSFET model

From http://pspmodel.asu.edu/downloads/psp103p1_summary.pdf

"PSP is a surface-potential based MOS Model, containing all relevant physical effects (mobility reduction, velocity saturation, DIBL, gate current, lateral doping gradient effects, STI stress, etc.) to model present-day and upcoming deep-submicron bulk CMOS technologies."

- accurate higher order derivatives
- more physics based modelling rather than threshold voltage

Models

Device modeling is difficult. Parameter extraction is difficult. Do not blindly trust models.

Sophisticated device models offer little intuition for design. Square law equations can not be used for design. Instead, chart based design (gm/Id).

Corner simulation also helps robustness against model parameters.

Online resources

As usual, not curriculum:

- BSIM manual: http://www-device.eecs.berkeley.edu/~bsim3/BSIM4/BSIM470/BSIM470_Manual.pdf
- BSIM parameter fitting: http://ewh.ieee.org/r5/denver/sscs/References/2003_03_Assenmacher.pdf
- Check list for device models: http://effectiveelectrons.com/whitepapers/Determine%20Foundry-Model%20Problems%20Without%20Touching%20A%20Wafer.pdf
- Chart based design: http://www.ewh.ieee.org/r6/scv/ssc/May1905.pdf