

# INF4420

## Random mismatch

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## Outline

Systematic vs. random mismatch

Hand calculation of random mismatch

Sources of random mismatch

Offset and calibration

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# Matching

Previously we have discussed systematic mismatch. Systematic mismatch can be minimized by careful layout or trimming. Binning is also used.

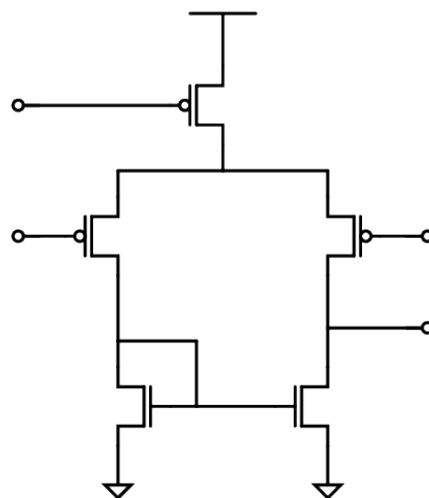
When "identical" devices are manufactured, random fluctuations cause electrical parameters of devices on the same die to have a statistical distribution. (Random mismatch)

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# Matching

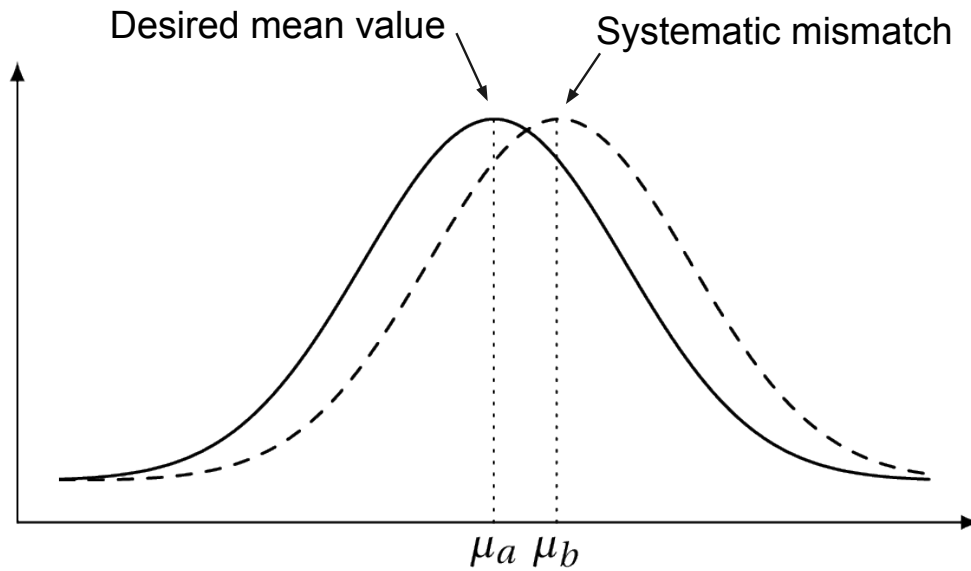
Need good matching between devices in input pair. And devices in current mirror.

Both systematic and random. Trimming can help both. Typically want to minimize inherent effect of both.



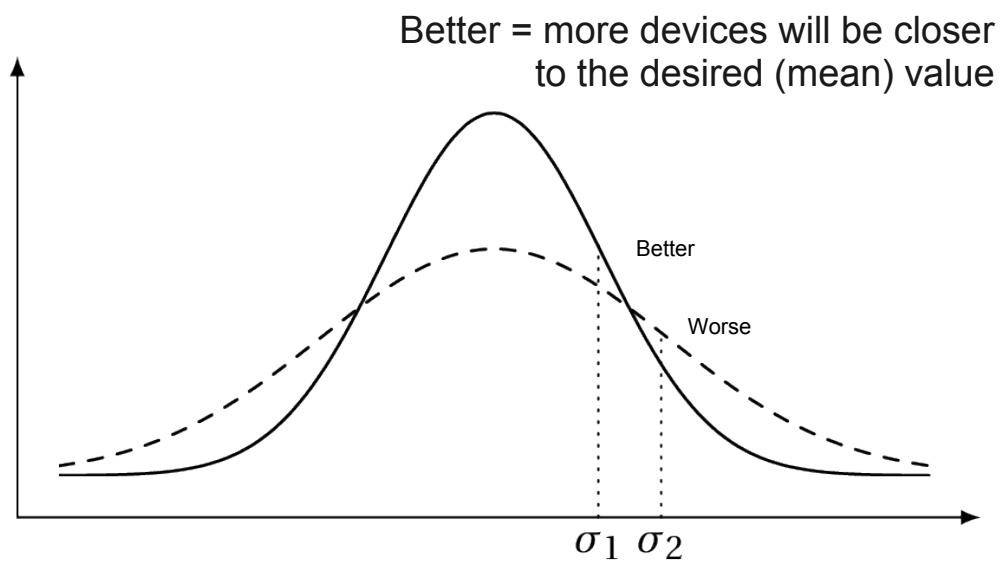
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# Systematic mismatch



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# Random mismatch



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# Worst-case analysis

Assuming a normal distribution (reasonable assumption from central limit theorem).

Worst case minimum value:  $\mu - 3\sigma$

Worst case maximum value:  $\mu + 3\sigma$

$3\sigma$  would capture 99.73 %

$6\sigma$  would capture 99.9999998 %

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# Monte-carlo simulation

Fab provides statistical parameters for device models.

Run a large number of simulations with different permutations of parameters.



Does not necessarily give insight into which devices are causing problems, or how to improve yield.

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# Hand calculation

IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. 24, NO. 5, OCTOBER 1989

1433

## Matching Properties of MOS Transistors

MARCEL J. M. PELGROM, MEMBER, IEEE, AAD C. J. DUINMAIJER,  
AND ANTON P. G. WELBERS

*Abstract*—The  $\beta$  factor, and current factor of MOS transistors have been analyzed and measured. Improvements to the existing theory are given, as well as extensions for long-distance matching and rotation of devices. Matching parameters of several processes are compared. The matching results have been verified by measurements and calculations on several basic circuits.

Manufacturing devices with different W/L, distance, orientation to see how this affects matching.

A systematic study of mismatch between parameters of two identical MOSFETs.

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# Hand calculation

Matching of parameter, P, between two identically drawn devices

$$\sigma_{\Delta P}^2 = \frac{A_P^2}{WL} + S_P^2 D_x^2$$

Area proportionality constant

Distance

Size

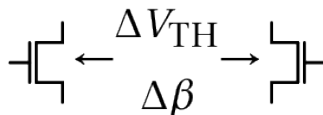
Variation with spacing

SpDx can be made small with good layout

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# Hand calculation

Mismatch between *two* identically drawn transistors. Will do hand calculation to find  $\Delta V_{th}$  and  $\Delta\beta/\beta$ . Use this to find  $\Delta I_D/I_D$ ,  $V_{os}$ , etc.



$$I_D = \frac{\mu_n C_{ox}}{2} \frac{W}{L} (V_{GS} - V_{TH})^2 = \frac{\beta}{2} (V_{GS} - V_{TH})^2$$

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# Sources of randomness

- Line edge roughness (LER)
- Random dopand fluctuation (RDF)
- Gate oxide thickness
- ...

Some effects due to the manufacturing process may not be truly random, but will appear random to us as designers, because it's outside our control. We will count this as "random".

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# Line edge roughness

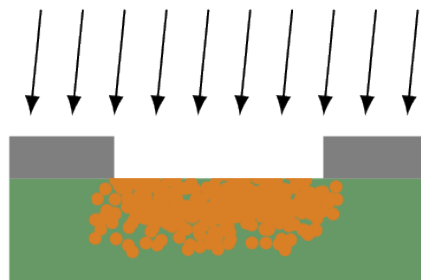
"LER is caused by a number of statistically fluctuating effects at these small dimensions such as shot [noise](http://spie.org/x32401.xml) (photon flux variations), statistical distributions of chemical species in the resist such as photoacid generators, the random walk nature of acid diffusion during chemical amplification, and the nonzero size of resist polymers being dissolved during development. It is unclear which process or processes dominate in their contribution to LER." [<http://spie.org/x32401.xml>]



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# Random dopant fluctuation

As features scale, fewer dopant atoms in the channel. The relative contribution of one atom increases. Single atom affects electrical parameters.



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# Basic rule of matching

Big devices match better. Randomness averages out more over a larger area.

Big devices, more capacitance, more area.  
Reducing random mismatch comes at a cost.  
Important to know how much mismatch we can live with to avoid costly overdesign.

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# Threshold voltage

Important contributions are  $t_{ox}$  and dopant concentration in channel region

Improves with scaling in  $t_{ox}$

$$\sigma_{\Delta V_{TH}} = \frac{A_{V_{TH}}}{\sqrt{WL}} \quad \leftarrow \text{Technology parameter}$$

Best guess  $\rightarrow$

$$\frac{A_{V_{TH}}}{t_{ox}} \approx \frac{\text{mV} \cdot \mu\text{m}}{\text{nm}}$$

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# Beta variability

Relative current factor mismatch,  $\Delta\beta/\beta$  [%]

$$\frac{\sigma_{\Delta\beta}^2}{\beta^2} = \frac{A_{\mu}^2}{WL} + \frac{A_{\text{COX}}^2}{WL} + \frac{A_W^2}{W^2L} + \frac{A_L^2}{WL^2} \approx \frac{A_{\beta}^2}{WL}$$

Best guess for  $A_{\beta}$  is 2 %  $\mu\text{m}$

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# Drain current mismatch

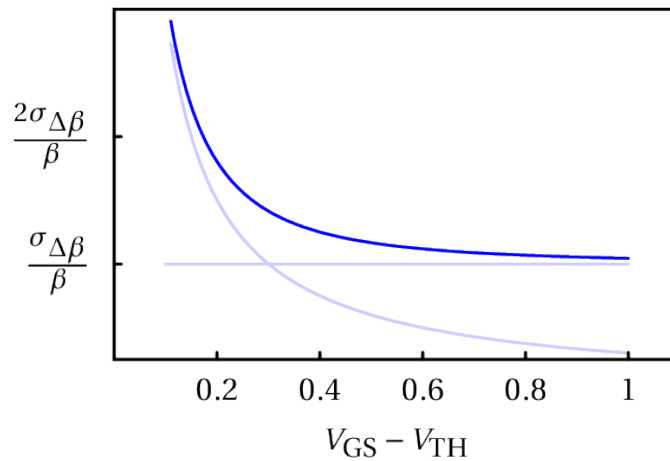
$$I_D = \frac{\beta}{2} (V_{\text{GS}} - V_{\text{TH}})^2$$

$$\sigma_y^2 \approx \left(\frac{\partial y}{\partial x_1}\right)^2 \sigma_{x_1}^2 + \left(\frac{\partial y}{\partial x_2}\right)^2 \sigma_{x_2}^2 + \dots + \left(\frac{\partial y}{\partial x_n}\right)^2 \sigma_{x_n}^2$$

$$\longrightarrow \frac{\sigma_{\Delta I_D}^2}{I_D^2} = \frac{4\sigma_{\Delta V_{\text{TH}}}^2}{(V_{\text{GS}} - V_{\text{TH}})^2} + \frac{\sigma_{\Delta\beta}^2}{\beta^2}$$

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# $\Delta I_D / I_D$ vs $V_{GS}$



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# Current mirror example

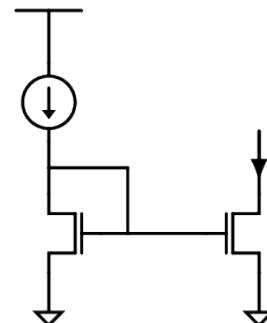
$$\frac{\sigma_{\Delta I_D}^2}{I_D^2} = \frac{4\sigma_{\Delta V_{TH}}^2}{(V_{GS} - V_{TH})^2} + \frac{\sigma_{\Delta\beta}^2}{\beta^2}$$

$$W = 2 \mu\text{m}, L = 0.5 \mu\text{m}$$

$$A_{\Delta V_{TH}} = 3 \text{ mV} \mu\text{m}$$

$$A_{\Delta\beta/\beta} = 2 \% \mu\text{m}$$

$$V_{GS} - V_{TH} = 200 \text{ mV}$$



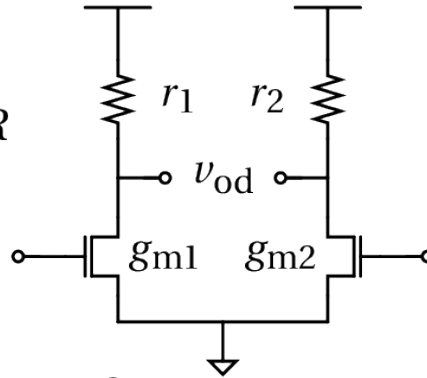
$$\frac{\sigma_{\Delta I_D}}{I_D} \approx 3.6 \% \quad \leftarrow \text{One standard deviation!}$$

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# Input referred offset

$$\sigma_{VOS,out} = \sigma_{\Delta I_D} \cdot R, A_0 = g_m R$$

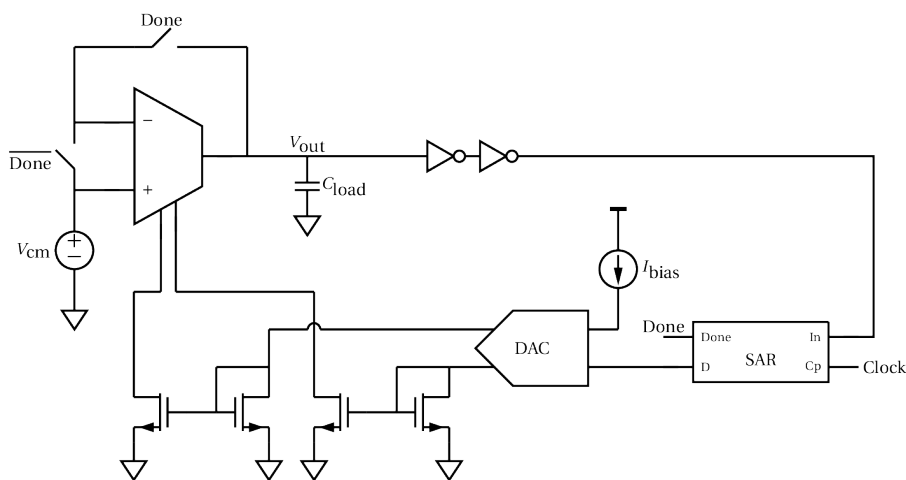
$$\sigma_{VOS,in} = \frac{\sigma_{VOS,out}}{A_0} = \frac{\sigma_{\Delta I_D}}{g_m}$$



$$\sigma_{VOS,in}^2 = \sigma_{\Delta V_{TH}}^2 + \frac{(V_{GS} - V_{TH})^2}{4} \frac{\sigma_{\Delta \beta}^2}{\beta^2}$$

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# Digital offset calibration



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# References

Orshansky, et al., *Design for Manufacturability and Statistical Design*, Springer, 2008

Pelgrom, *Component matching: best practices and fundamental limits*, [IDESIA](#).

Pastre and Kayal, [Methodology for the Digital Calibration of Analog Circuits and Systems](#), Springer, 2006