UiO : Department of Informatics
University of Oslo

INF4420

Switched capacitor circuits

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Outline

Switched capacitor introduction

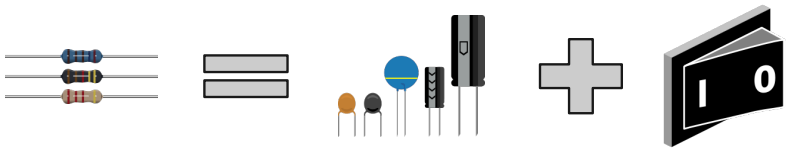
MOSFET as an analog switch

z-transform

Switched capacitor integrators

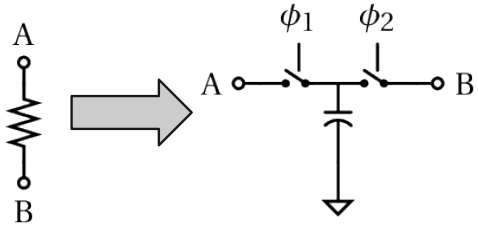
Introduction

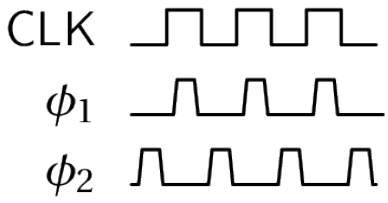
Discrete time analog signal processing



Why?

Introduction





The arrangement of switches and the capacitor approximates a resistor.

Analyze each clock phase separately

Introduction

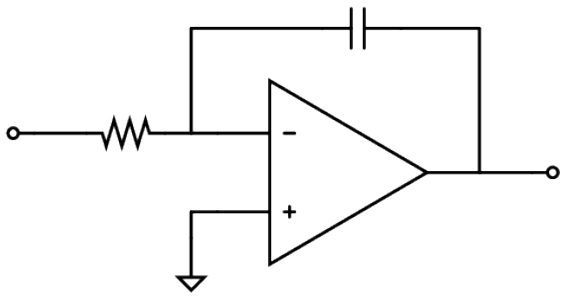
Assuming steady-state, and arbitrarily assume $V_A > V_B$. T is one clock cycle.

1. At the *beginning* of ϕ_1, node V_C is at V_B Volt
2. During ϕ_1, V_C is charged to V_A. Charge transfer from V_A to C: $\Delta Q = C(V_A - V_B)$
3. During ϕ_2: ΔQ transfered from C to V_B

Net charge transfer, ΔQ, from V_A to V_B in T sec.

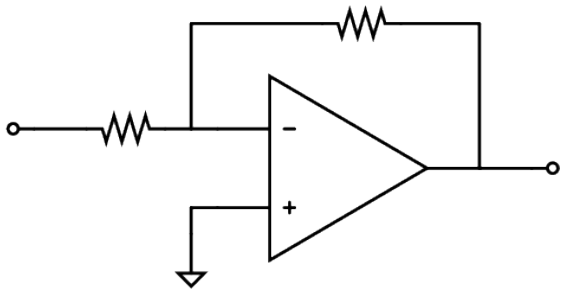
$I_{AVG} = C(V_A - V_B)/T$, $R_{AVG} = T/C$

Introduction



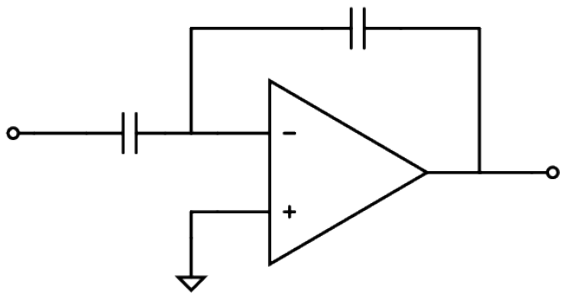
RC accuracy (matching). Large time constants .

Introduction



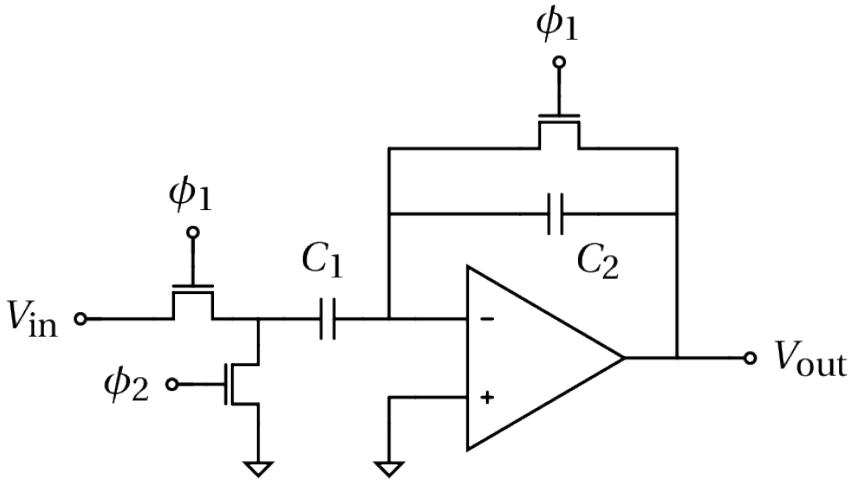
Resistive loading is not ideal for CMOS

Introduction



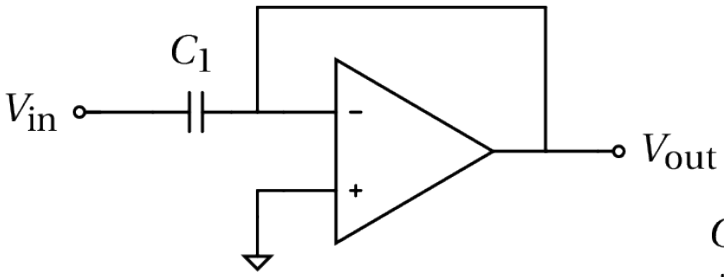
Capacitive feedback. DC issues.

Switch-cap amplifier

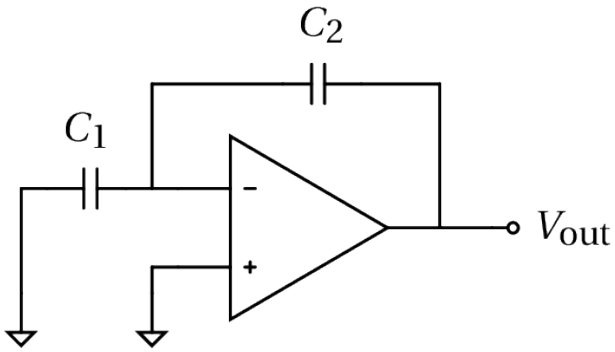


Analyze ϕ_1 and ϕ_2 separately!

Switch-cap amplifier



Phase ϕ_1:
C_1 tracks V_{in},
$Q = C_1 V_{in}$



Phase ϕ_2:
Charge transfer
from C_1 to C_2

Switch-cap amplifier

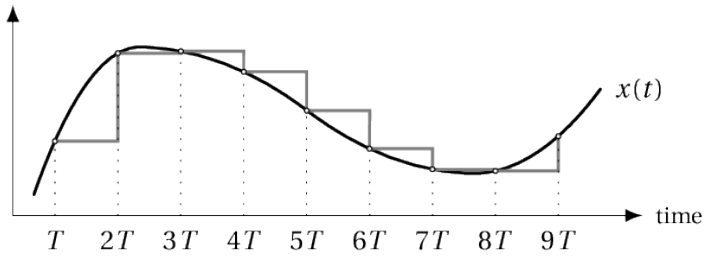
1. During ϕ_1, C_1 is charged to $Q = C_1 V_{in}$
2. During ϕ_2, the charge, Q, is transferred to C_2.

If C_1 and C_2 are of different value, the same charge will give a different voltage drop

$$C_1 V_{in} = C_2 V_{out} \Rightarrow V_{out} = V_{in} \frac{C_1}{C_2}$$

Sampling

Discrete time, continuous amplitude



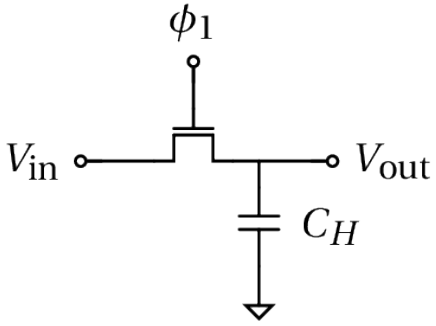
Signal, x(t), sampled at discrete time points, nT

MOSFET analog switch

During ϕ_1, V_{out} tracks V_{in}

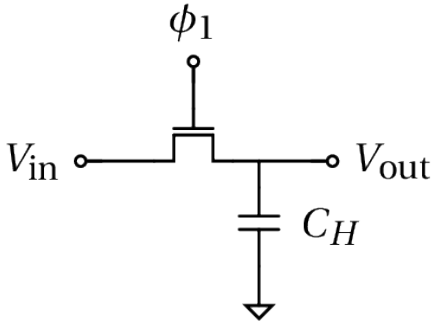
After ϕ_1 the switch is closed and V_{in} (from the end of ϕ_1) is held on C_H.

However, the MOSFET "switch" is not perfect ...



MOSFET analog switch

- Finite resistance (settling)
- Charge injection
- Clock feed-through



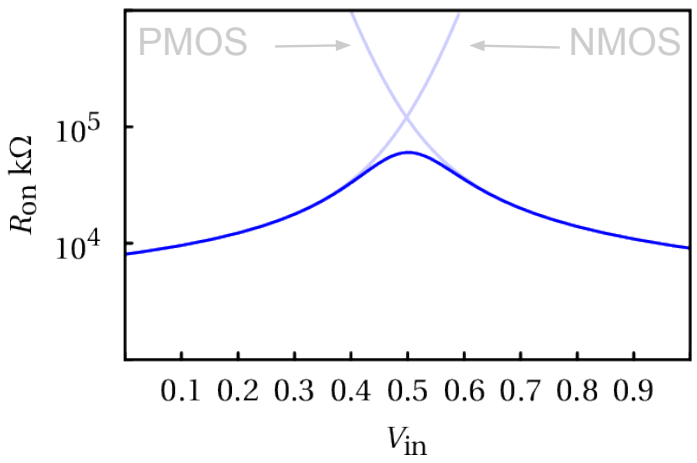
Large signal behaviour

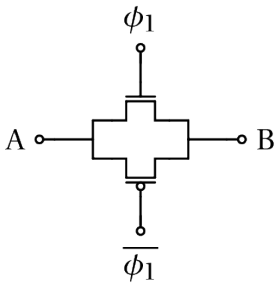
NMOS can discharge effectively from Vdd to 0 (compare to a digital inverter). Saturation, then triode.

However, the NMOS can not charge from 0 to Vdd. The MOSFET will enter subthreshold and current through the switch will be low. Output will settle to Vdd - Vth. If we wait for a long time, output will slowly approach Vdd.

Finite switch resistance

Complimentary switch resistance, still problems for low Vdd

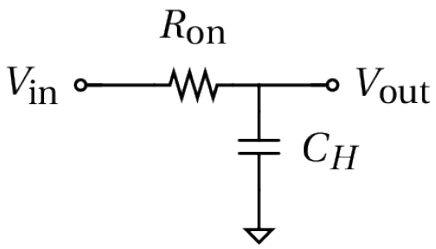




Finite switch resistance

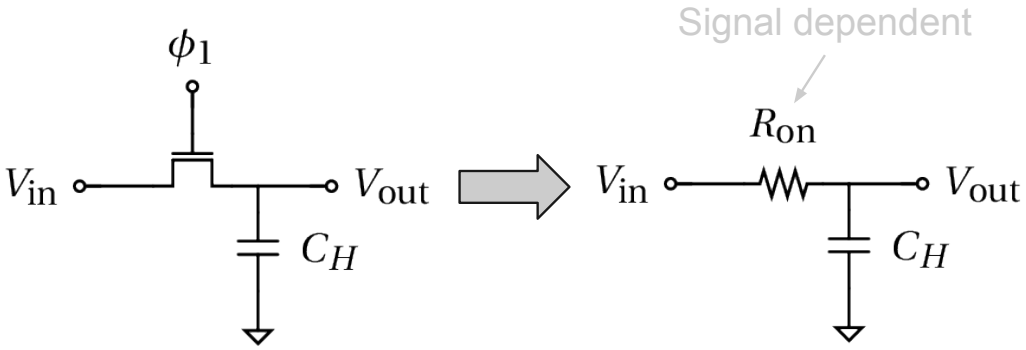
The RC time constant will define the sampling time, therefore the maximum frequency of operation.

$$R_{\text{on}} = \frac{1}{\beta(V_{\text{dd}} - V_{\text{in}} - V_{\text{TH}})}$$



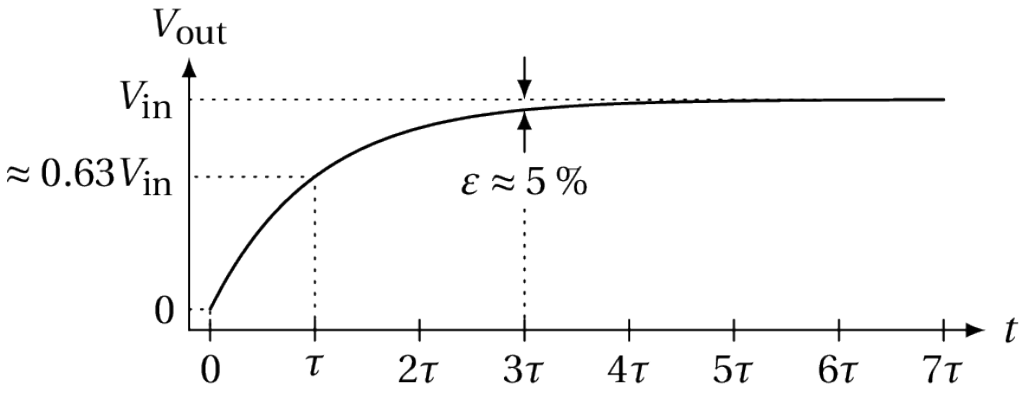
Finite switch resistance

Even if we restrict the input voltage range so that we avoid subthreshold. The settling speed will still be limited by the finite switch resistance.



Finite switch resistance

Settling behaviour introduces an error in the final value. Need to wait several time constants for accurate settling.



Finite switch resistance

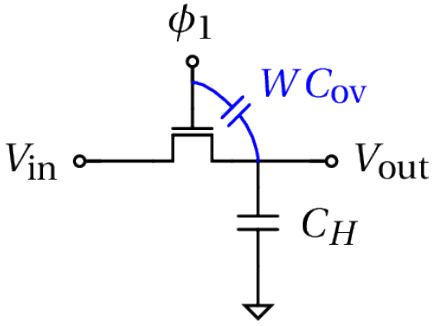
t_s	ε
3*RC*	5 %
7*RC*	0.1 %
9*RC*	0.01 %

$$t_s = \tau \ln \frac{1}{\varepsilon}$$

Faster settling: Smaller C (more noise and parasitics more prominent) or smaller R (wider transistor, more channel charge)

Clock feed-through

Capacitive voltage divider (hold capacitor and parasitic overlap capacitor)



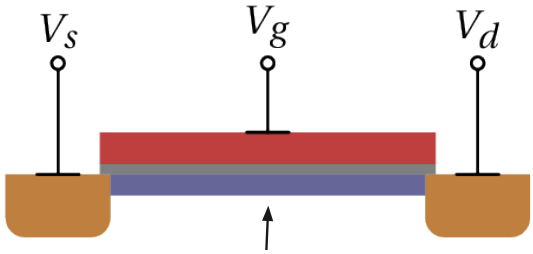
$$\Delta V = V_{dd}\frac{WC_{ov}}{WC_{ov}+C_H}$$

Signal independent!

Increasing C_H helps but degrades settling speed

Charge injection

Channel charge, Q_{ch}, when switch is "on". Released when switch turns off. Common assumption: Half the channel charge goes to source and other half to drain.

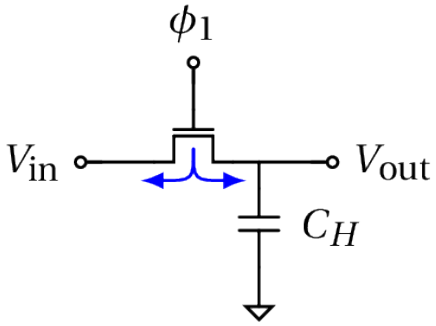


$$Q_{ch} = WLC_{ox}(V_{dd} - V_{in} - V_{TH})$$

$$\Delta V \approx \frac{Q_{ch}}{2C_H}$$

Charge injection

Q_{ch} is a function of V_{in} and (worse) V_{TH} is a function of V_{in} through body effect (non-linear).



Charge distribution is complex and poorly modelled

$$Q_{ch} = WLC_{ox}(V_{dd} - V_{in} - V_{TH})$$

Signal dependence

Charge injection

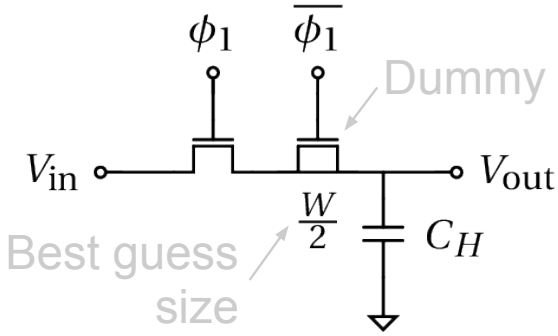
Figure of merit (FoM) to study speed vs. precision trade-off. Larger C_H makes charge injection less prominent but also increases the time constant and therefore ΔV from settling error.

$$\text{FoM} = \frac{1}{\tau \cdot \Delta V} = \frac{\mu_n}{L^2}$$

Charge injection

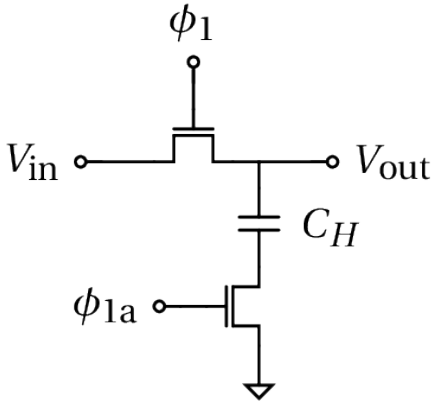
Dummy switch will ideally cancel the injected channel charge. Because the charge distribution is complex, finding the optimal size of the dummy switch is difficult.

The purpose of the dummy switch is to soak up channel charge from the main switch.



Charge injection

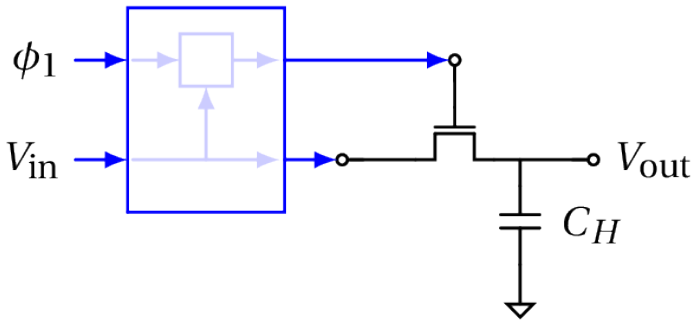
Bottom plate sampling: ϕ_{1a} turns off slightly before ϕ_1, injecting a constant channel charge. Signal dependent charge from ϕ_1 will ideally not enter C_H (no path to ground).



Bootstrapped switch

Include extra circuitry to generate a clock voltage that takes V_{in} into account to generate a *constant* V_{GS}. Reliability concerns. Complexity.

Better R_{ON} independent of V_{in}. High clock V_{in} + V_{dd}



Amplifier specification

- C_{in} (contributes to gain error)
- Slew rate
- DC gain (loop gain, determines static error)
- GBW (determines dynamic error)
- Phase margin (stability)
- Offset (can be compensated, CDS)
- Noise (offset compensation helps 1/f noise)

Sampling and z-transform

For continuous time circuits the Laplace transform is very convenient as it allows us to solve differential equations using algebraic manipulation.

Analyzing SC circuits in terms of charge transfer, and charge conservation, results in difference equations. Need a similar tool for this case.

Sampling and z-transform

Laplace transform:

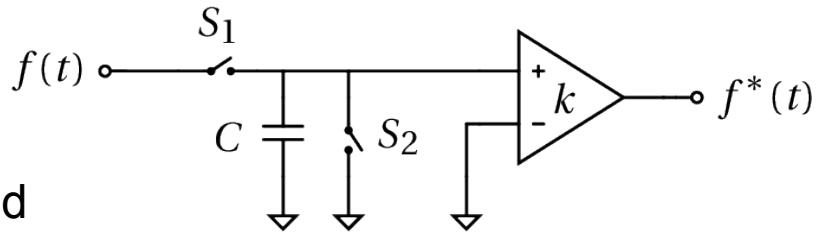
Input signal

$$F(s) = \int_0^\infty f(t)\, e^{-st}\, dt$$

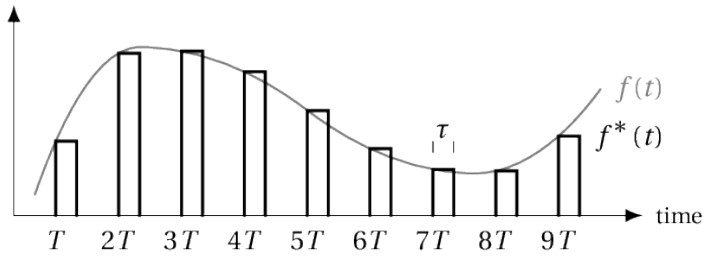
Fourier transform:

$$F(j\omega) = \int_{-\infty}^{\infty} f(t)\, e^{-j\omega t}\, dt$$

Sampling and z-transform



Circuit and waveforms for illustrating sampling theory



Sampling and z-transform

Modelling the sampled output, $f^*(t)$

Step function: $u(t) \equiv \begin{cases} 1, & t \geq 0 \\ 0, & t < 0 \end{cases}$

Laplace transforms:

$$f(t) \longleftrightarrow F(s)$$

$$u(t) \longleftrightarrow s^{-1}$$

$$f(t-a)\,u(t-a),\ a \geq 0 \longleftrightarrow e^{-as}F(s)$$

Sampling and z-transform

$$f^*(t) = \sum_{n=0}^{\infty} f(nT)[u(t-nT) - u(t-nT-\tau)]$$

assuming $f(t) = 0$ for $t < 0$

$$F^*(s) = k\sum_{n=0}^{\infty} f(nT)\left[\frac{e^{-snT}}{s} - \frac{e^{-s(nT+\tau)}}{s}\right]$$

$$= k\frac{1-e^{-s\tau}}{s}\sum_{n=0}^{\infty} f(nT)\,e^{-snT}$$

Sampling and z-transform

Impulse sampling: Choose τ "infinitely narrow" and the gain, $k = 1/\tau$ (area of the pulse equal to the instantaneous value of the input, $f(nT)$). In this case, we find:

$$F^*(s) \approx \sum_{n=0}^{\infty} f(nT)\,e^{-snT}$$

A very convenient notation: $z \equiv e^{sT}$

Sampling and *z*-transform

The *z*-transform is very convenient for sampled data systems:

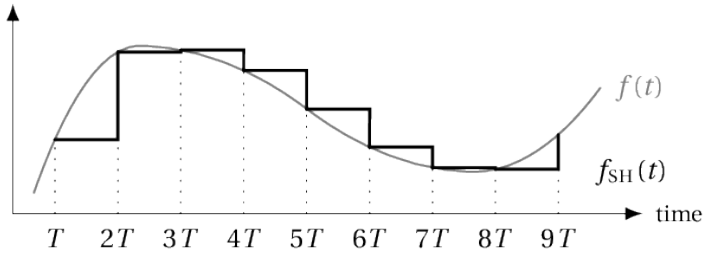
$$F(z) = \sum_{n=-\infty}^{\infty} f(nT)\, z^{-n}$$

Delay by *k* samples (*k* periods):

$$z^{-k} F(z)$$ Important!

Sampling and *z*-transform

We have assumed infinitely narrow pulses. Most switched capacitor systems will have sample and hold (S&H) behaviour.



Sampling and z-transform

Use the same equation as before, but instead of letting τ be infinitely narrow, we let τ = T.

$$F^*(s) = \underbrace{k\frac{1-e^{-s\tau}}{s}}_{\approx 1 \text{ for impulse sampling}} \sum_{n=0}^{\infty} f(nT)\, e^{-snT}$$

Sample & hold:

$$F_{\mathrm{SH}}(s) = k\frac{1-e^{-sT}}{s} \sum_{n=0}^{\infty} f(nT)\, e^{-snT}$$

Sampling and z-transform

Comparing $F^*(s)$ and $F_{\mathrm{SH}}(s)$, we define the transfer function of the sample and hold as:

$$H_{\mathrm{SH}}(s) \equiv \frac{1-e^{-sT}}{s}$$

Frequency response

Comparing the *z*-transform to the Fourier transform, we can find the frequency response from the *z*-domain expression,

$s = j\omega$ gives $z = e^{j\omega T}$.

$$F(z) = \sum_{n=-\infty}^{\infty} f(nT)\, z^{-n}$$

$$F\left(e^{j\omega T}\right) = \sum_{n=-\infty}^{\infty} f(nT)\, e^{-jn\omega T}$$

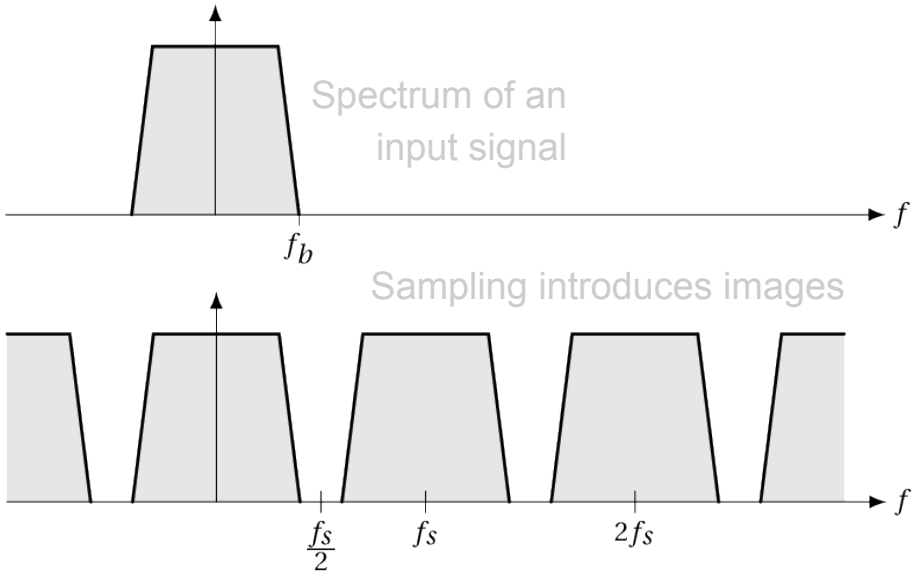
Frequency response

z-transform: $z \rightarrow e^{sT}$. Mapping between *s*-plane and *z*-plane.

Points on the imaginary axis of the *s*-plane map to the *unit circle* in the *z*-plane, periodic with 2π

For a sampled data system, frequency response is *z*-domain expression evaluated on the unit circle in the *z*-plane. Poles must be inside unit circle for stability.

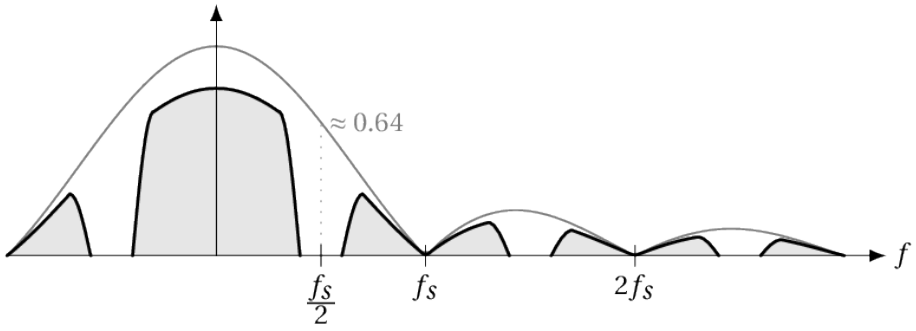
Frequency response



Frequency response

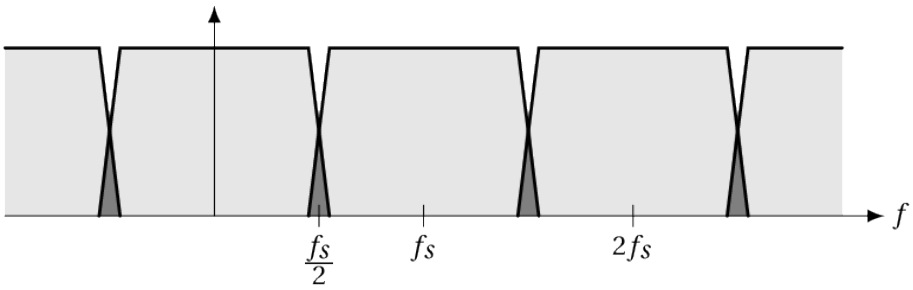
Multiplying by the transfer function of the sample and hold, we find the frequency spectrum of $F_{SH}(j\omega)$ (sin(x)/x, sinc-response).

Linear distortion from droop.



Frequency aliasing

If the signal contains frequencies beyond $f_s/2$ when sampled, aliasing will occur (non-linear distortion). Images of the original signal interfere.

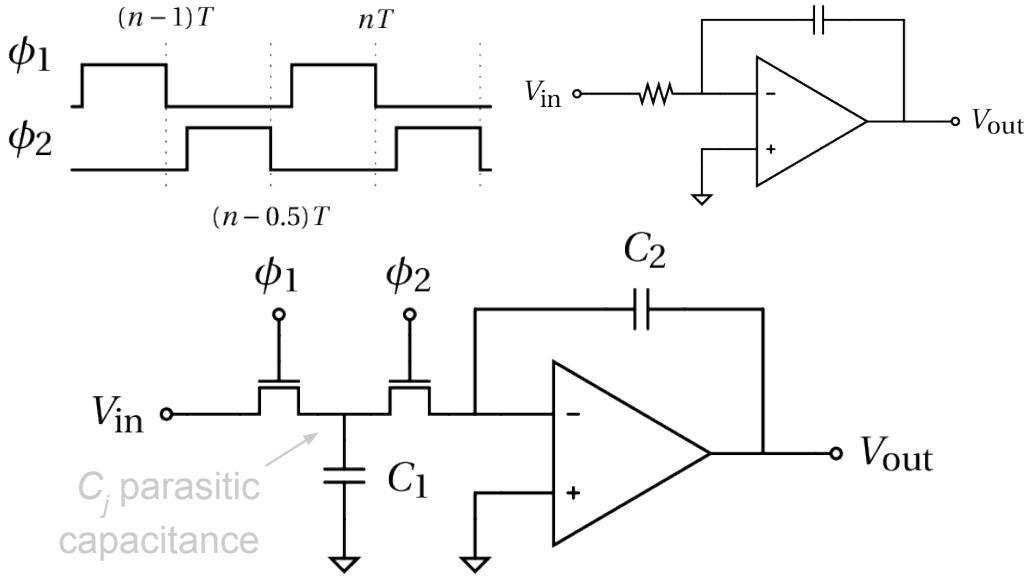


Frequency aliasing

A continuous time low-pass filter (anti-aliasing filter) on the input to the sampled data system will ensure that the input signal is band limited to a frequency below the Nyquist frequency.

Need to take some margin to account for the transition band of the filter (usually first or second order).

Switch-cap integrator



Switch-cap integrator

Charge on C_1 is proportional to V_{in}, $Q_1 = C_1 V_{in}$. Each clock cycle, Q_1, is transferred from C_1 to C_2. C_2 is never reset, so charge accumulates on C_2 (indefinitely). We are adding up a quantity proportional to the input signal, V_{in}. This is a discrete time integrator. In the following, we assume the output is read during ϕ_1.

Switch-cap integrator

$$Q_2(nT) = Q_2((n-0.5)T)$$ ← Output at ϕ_1

$$Q_2(nT) = Q_2((n-1)T) - Q_1((n-1)T)$$

$$C_2 V_{\text{out}}(nT) = C_2 V_{\text{out}}((n-1)T) - C_1 V_{\text{in}}((n-1)T)$$

$$C_2 V_{\text{out}}(z) = z^{-1} C_2 V_{\text{out}}(z) - z^{-1} C_1 V_{\text{in}}(z)$$

$$C_2 V_{\text{out}}(z)\left(1 - z^{-1}\right) = -z^{-1} C_1 V_{\text{in}}(z)$$

Delaying

$$H(z) = \frac{V_{\text{out}}(z)}{V_{\text{in}}(z)} = -\frac{C_1}{C_2}\frac{z^{-1}}{1-z^{-1}} = -\frac{C_1}{C_2}\frac{1}{z-1}$$

Switch-cap integrator

Approx frequency response: $z = e^{j\omega T} \approx 1 + j\omega T$

Valid when ωT is close to zero. I.e. when signal frequency is low compared to sampling freq.

$$H(z) = -\frac{C_1}{C_2}\frac{1}{z-1}$$

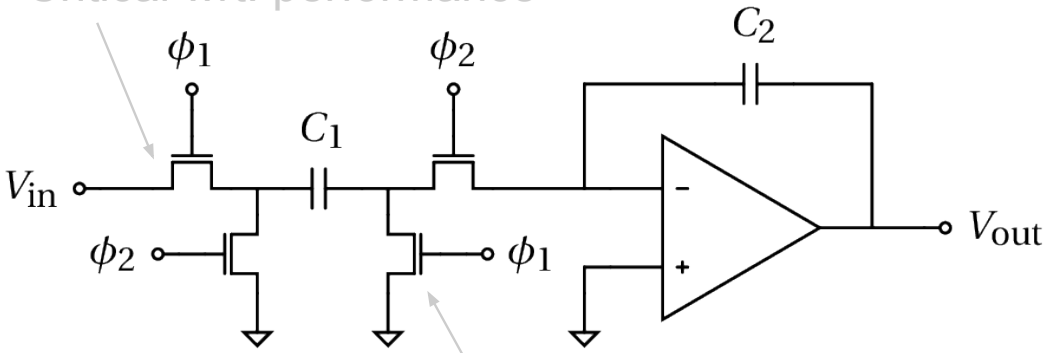
Compare to continuous time

$$H\left(e^{j\omega T}\right) \approx -\frac{C_1}{C_2}\frac{1}{j\omega T}, \quad \tau = T\frac{C_2}{C_1}$$

Switch-cap integrator

Insensitive to non-linear parasitic cap, C_j

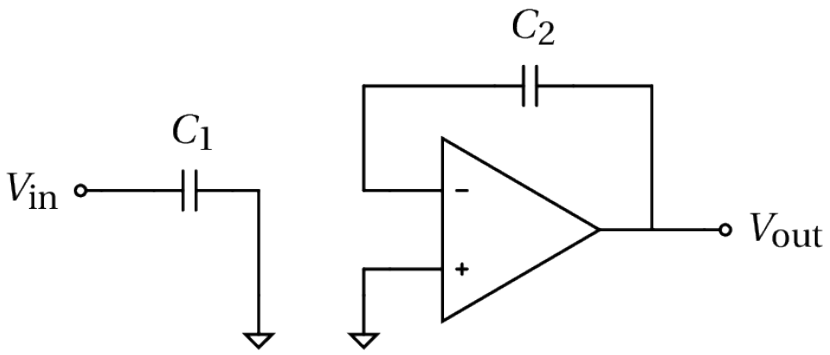
Critical wrt. performance



Turn off first (bottom plate sampling)

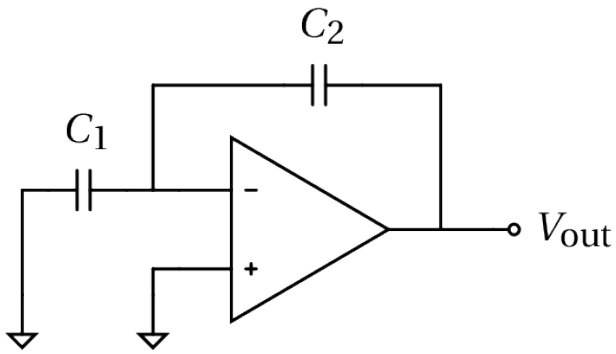
Switch-cap integrator

During ϕ_1 C_1 tracks V_{in} and V_{out} is constant.



Switch-cap integrator

During ϕ_2 charge is transferred from C_1 to C_2. V_{out} settles to the new value.



Switch-cap integrator

Analysis similar to the parasitic sensitive integrator, however, polarity of the capacitor changes because of the switching. So gain is not inverting.

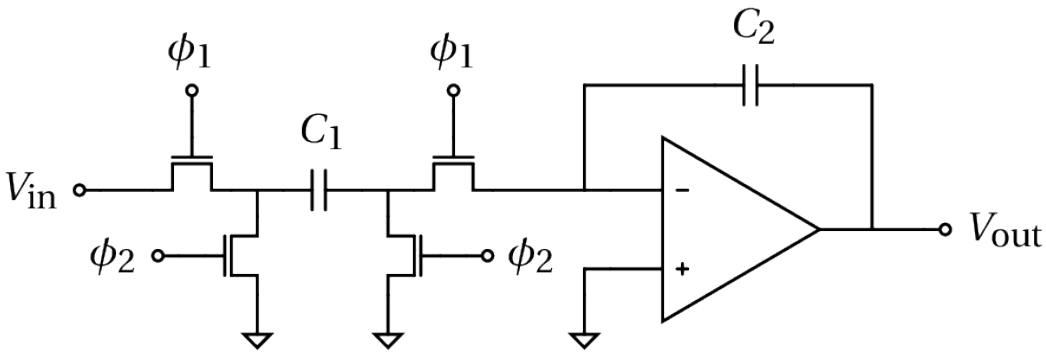
Looking at the output during ϕ_1 we have a delaying non-inverting integrator.

$$H(z) = \frac{C_1}{C_2}\frac{z^{-1}}{1-z^{-1}} = \frac{C_1}{C_2}\frac{1}{z-1}$$

Switch-cap integrator

By changing the switching we get a non-delaying inverting int.

$$H(z) = -\frac{C_1}{C_2}\frac{1}{1-z^{-1}} = -\frac{C_1}{C_2}\frac{z}{z-1}$$



References

Gregorian and Temes, *Analog MOS Integrated Circuits for Signal Processing*, Wiley, 1986

Baker, *Mixed Signal Circuit Design,* IEEE Wiley, 2009

Sansen, *Analog Design Essentials,* Springer, 2006, Ch. 17

Johns and Martin, *Analog Integrated Circuit Design,* Wiley, 1997