VHDL ARRAYS

- Signals of the same type.

- ”Std_logic_array” are array of type ”std_logic” defined in ieee.std_logic_1164 package.

- Note that:
  - signal z_bus : std_logic_vector(3 downto 0);
  - signal c_bus : std_logic_vector(0 to 3);

  - z_bus <= c_bus;

- This may be correct(?), but the result is:

  - z_bus(3) gets the c_bus(0) value,
  - z_bus(2) gets the c_bus(1) value,
  - z_bus(1) gets the c_bus(2) value,
  - z_bus(0) gets the c_bus(3) value.

MULIDIMENSIONAL ARRAY DECLARATION

- Example declarations:
  - type t_nibble is array(3 downto 0) of std_logic;
  - type t_a_of_a is array(7 downto 0) of t_nibble;
  - type t_2d_a is array(5 downto 0, 3 downto 0) of std_logic;
  - signal mem8x4 : t_a_of_a;
  - signal mem6x4 : t_2d_a;
  - signal nibble0, nibble1, nibble2, nibble3, nibble4,
    nibble5, nibble6, nibble7 : t_nibble;

MULIDIMENSIONAL ARRAY USE

- Example use:
  - **single values** :
```
mem8x4(0)(0) <= '1';
mem6x4(0,0) <= '1';
```
  - **aggregates** :
```
mem8x4 <= (nibble0, nibble1, … , nibble7);
mem6x4 <= (nibble0, nibble1, … , nibble5);

mem8x4 <= (others => nibble0);
mem6x4 <= (others => nibble5);

mem8x4 <= (others => (others => '0'));
mem6x4 <= (others => (others => '1'));
```