F13 Mot 10.
Amplifier Architectures

When a transistor is used in an amplifier, oscillator, filter, sensor, etc. it will also be a need for passive elements like resistors, capacitors and coils to provide biasing so that the transistor has the correct working point. These passive elements will influence on the noise. In the following we will look at some architectures and how they affect the equivalent input noise.

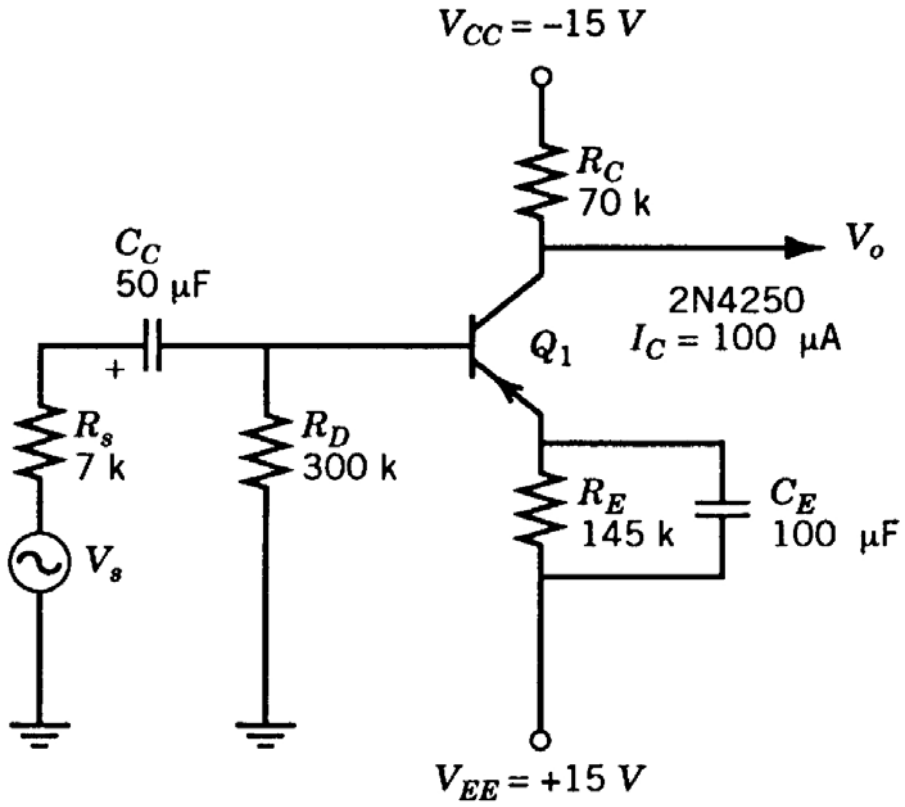
Transistor configurations:
There are three main ways to place a FET/BJT in an architecture:

BJT	FET
CE: Common Emitter	**CS**: Common Source
CB: Common Base	**CG**: Common Gate
CC: Common Collector	**CD**: Common Drain

CE/CS has the largest power amplification.
CC/CD is used to achieve high input impedance and low output impedance.
CG/CB is used by achieve low input impedance and high output impedance.

When the *Eni* is calculated for the gate/bias it is almost equal for all configurations. Hence the E_{ni}, E_n and I_n calculated for CE/CS can also be used in CC/CD and CB/CG configurations. This assumes that the frequency is so low that the internal collector-base feedback capacitance can be ignored.
NB! Although the input noise is the same this does not apply to the output noise.

10-2 Common-Emitter



The figure shows a transistor that is biased for low noise operation between 10Hz and 10kHz.
The noise values are as follows:

	10Hz	10kHz
E_n	2nV	2nV
I_n	2pA	0.3pA
R_0	1000Ω	6700Ω
$NF@R_0$	1.8dB	0.3dB

Small signal equivalent schematic for the circuit is shown on the next page.

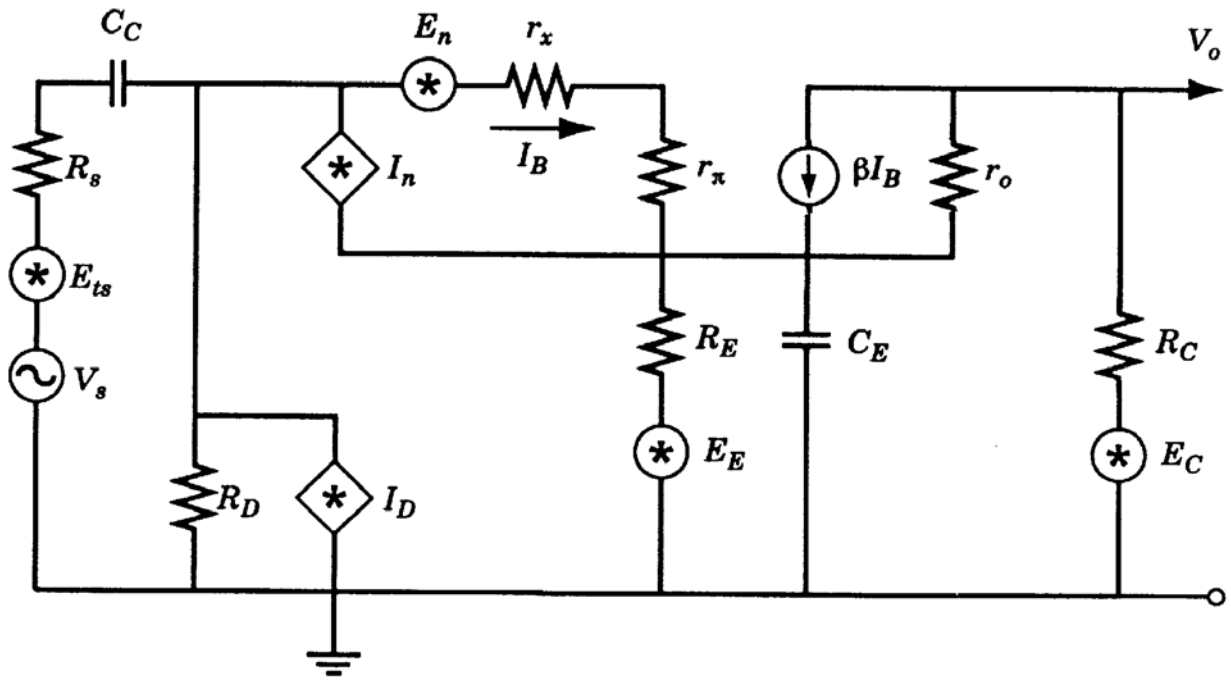


Figure 10-2 Noise and small-signal equivalent circuit for CE stage.

The schematic shows a hybrid-π model together with passive bias elements.

The voltage gain *Kt*:

$$K_t \cong \left(\frac{-\beta R_L}{Z_i}\right)\left(\frac{Z_i \parallel R_D}{Z_S + Z_i \parallel R_D}\right)$$

K_t is the voltage gain from V_s to V_o. The first parenthesis is the voltage gain within the transistor (β is I_C/I_B) while the second parenthesis is the network in front of the base.

$$Z_i = r_x + r_\pi + (\beta + 1)Z_E$$

The input resistance Z_i consists also of the resistance you can see through the base to emitter. ($\beta+1=I_E/I_B$).

$$R_L \cong R_C \parallel r_0 \parallel R_{i2}$$

The load resistance consists of both the collector bias resistance, the transistor internal resistance and the input resistance of the next stage: R_{i2}.

$$Z_E = R_E \parallel -jX_E .$$

The emitter impedance consists of a real part and an imaginary part (a resistance and a capacitance in parallel).

$$Z_S = R_S - jX_C$$

The source impedance is a resistance in series with a capacitor.

If we assume ignorable loss in biasing, coupling and feedback we can simplify the expression for K_t to:

$$K_t \cong -\frac{\beta R_L}{Z_S + r_x + r_\pi + \beta Z_E}$$

If $Z_S << r_\pi$ and $Z_E << r_e$ the expression is simplified to:

$$K_t \cong -\frac{R_L}{r_e} = -g_m R_L$$

We simplify and ignore the external load and simplifies R_L so that:

$$K'_t = K_t \quad for \quad R_L = R_C$$

We will then have the following expression for the equivalent input noise:

$$E_{ni}^2 \cong E_{ns}^2 + E_n^2\left(\frac{R_S + R_D}{R_D}\right)^2 + I_n^2\left(R_S - jX_C\right)^2 + I_D^2 R_S^2$$

$$+\frac{E_E^2}{1+\left(\omega R_E C_E\right)^2} + \left(\frac{E_C}{K'_t}\right)^2$$

In the expression, we recognise the first line (say from section. 7.3). Last term is also known. The second last term, however, need some comments. The voltage over R_E will not be E_E for higher frequencies, because C_E will "attempt to short-circuit" this. We choose to model the thermal noise in R_E as a current noise of size $I_E=E_E/R_E$. The noise current over R_E and C_E will be:

$$E'^2_E = I_E^2 \cdot \left(C_E \parallel R_E\right) = \frac{E_E^2}{R_E^2}\left|\frac{R_E}{j\omega R_E C_E + 1}\right|^2 = \frac{E_E^2}{1+\left(\omega R_E C_E\right)^2}$$

Back to the expression for E_{ni}:

$$E_{ni}^2 \cong E_{ns}^2 + E_n^2\left(\frac{R_S + R_D}{R_D}\right)^2 + I_n^2\left(R_S - jX_C\right)^2 + I_D^2 R_S^2$$

$$+\frac{E_E^2}{1+\left(\omega R_E C_E\right)^2} + \left(\frac{E_C}{K'_t}\right)^2$$

From the expression we find that to have low noise:

- ⇨ R_D should be large relative to R_S.
- ⇨ C_C should be great.
- ⇨ Rs should be small.
- ⇨ R_E should be small (less than R_S).
- ⇨ C_E should be high.
- ⇨ K_t should be large.
- ⇨ R_C should be large.

If the AC-coupling is not needed is remove R_D and C_C.

CE has the greatest power amplification and noise from stages following the amplifier can probably be ignored.

The input resistance varies with I_C.

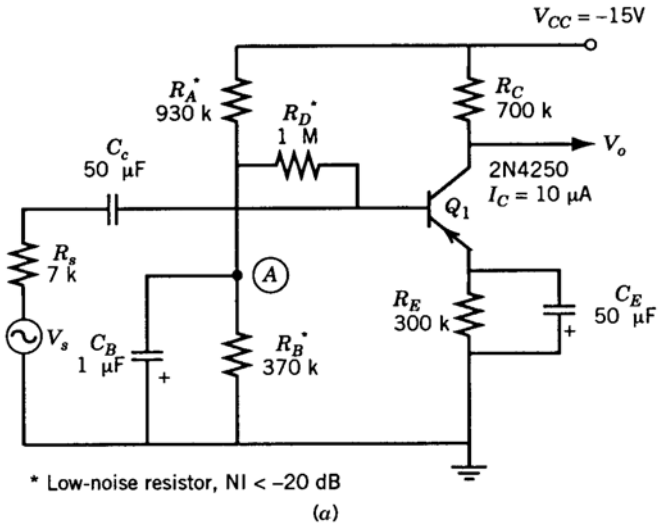
Choice of capacitance value.

C_C has a high pass effect with 3dB limit equal to the sum of the source resistance and resistance to the amplifier (including bias).
With regard to noise $1/(\omega C_C)$ should be much less than R_S at the lowest relevant frequency. This is because these are added and determines the contribution of I_n: $In\cdot(R_S+j/(\omega C_C))$. Obviously the last term should be tried made small (<1/100) relative to R_S. NB! Hence due to noise C_C must not be used intentionally for filter functions!

C_E should short-circuit emitter AC-wise to ground. The impedance of C_E should be small in relation to the internal resistance in the emitter: r_e.
Basically noise in R_E has the same weight as the noise in the source. However, C_E will reduce the contribution from R_E. In the expression below is the noise contribution from R_E in the numerator.

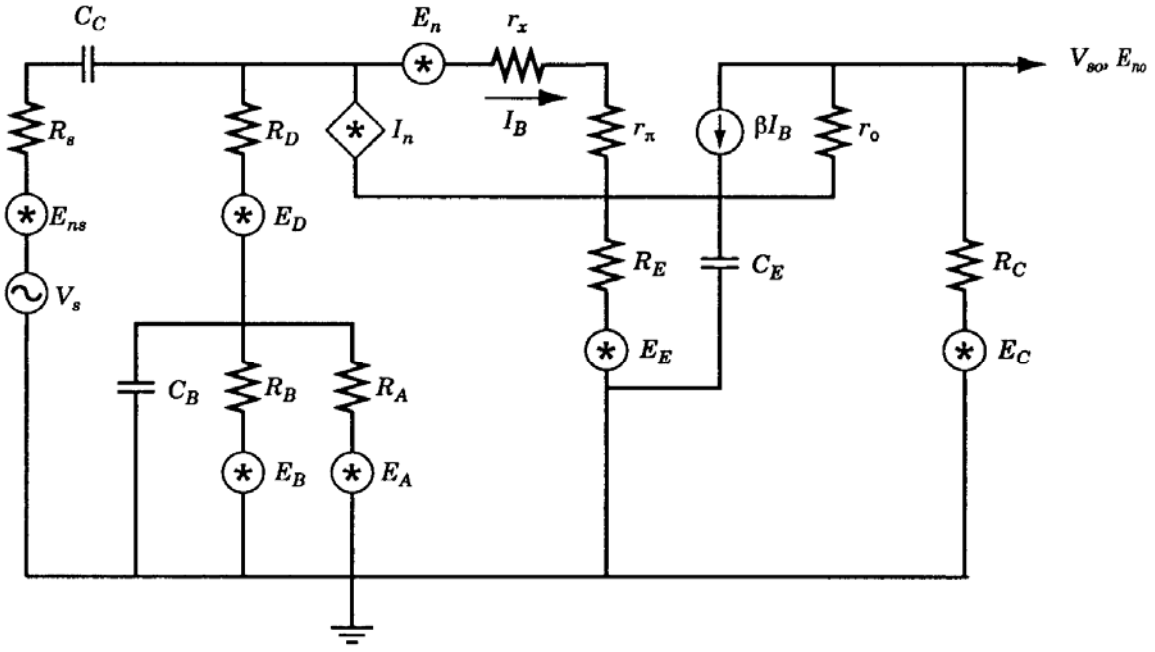
$$\frac{E_{tE}^2}{1+\omega^2 R_E^2 C_E^2} << E_S^2$$

Common-emitter with one voltage supply.



Here a point A is established supplying a stable DC potential for the base and that AC-wise is short circuited to ground through C_B.

The noise schematic is as follows:



(b)

Equivalent input noise can be expressed as:

$$E_{ni}^2 \cong E_{ns}^2 + E_n^2\left(\frac{R_S + R_D}{R_D}\right)^2 + I_n^2\left(R_S - jX_C\right)^2$$

$$+\left[\frac{E_A^2}{1+\left(\omega R_A C_B\right)^2} + \frac{E_B^2}{1+\left(\omega R_B C_B\right)^2} + E_D^2\right]\frac{R_S^2}{R_D^2} + \frac{E_E^2}{1+\left(\omega R_E C_E\right)^2} + \left(\frac{E_C}{K'_t}\right)^2$$

In addition to the known terms, we have now a new term in square parenthesis due to the base bias network. The parenthesis is weighted with the R_S/R_D ratio.

The DC-voltage at the base is determined by the relationship between R_A and R_B as follows:

$$V_A = \frac{R_B V_{CC}}{R_A + R_B}$$

The contributing noise from the resistors R_A and R_B should be relatively small. A good starting point is to chose C_B so large that the noise in the relevant frequency range satisfies the inequality:

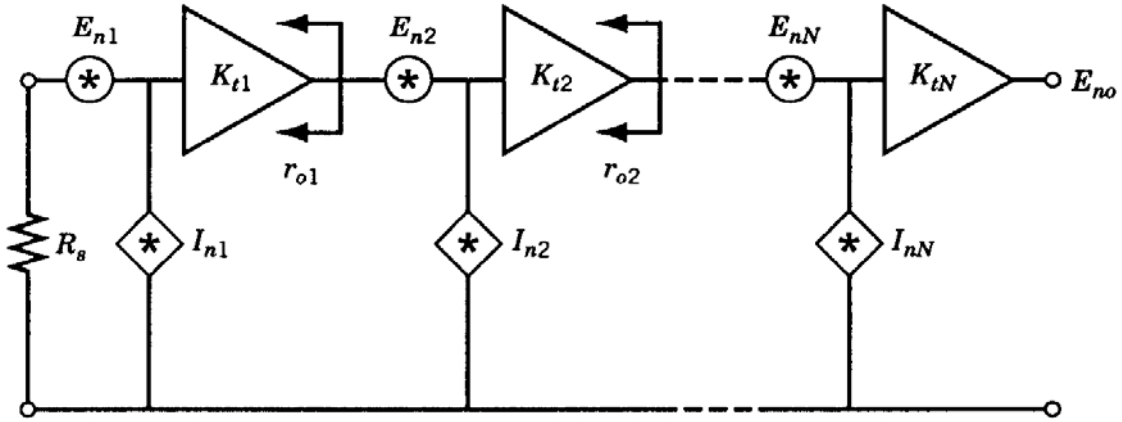
$$E_{tD}^2 >> \frac{E_{tA}^2 + E_{xA}^2}{1+\omega^2 R_A^2 C_B^2} + \frac{E_{tB}^2 + E_{xB}^2}{1+\omega^2 R_B^2 C_B^2}$$

Noise in the amplifier is given in the following table:

	10Hz	10kHz
E_n	4.5nV	4.5nV
I_n	0.3pA	0.1pA
R_0	10kΩ	45Ω
$NF@R_0$	0.68dB	0.35dB
Kt	280	
Ri	780	

Noise in cascaded stages

We have previously studied the noise figure for cascaded amplifiers. We will now look at the equivalent input noise:



The expression for equivalent input noise can be expressed as follows .....

$$E_{ni}^2 = E_{ns}^2 + E_{n1}^2 + I_{n1}^2 R_S^2 + \frac{E_{n2}^2 + I_{n2}^2 r_{o1}^2}{K_{t1}^2} + \frac{E_{n3}^2 + I_{n3}^2 r_{o2}^2}{K_{t1}^2 K_{t2}^2} + \cdots\cdots$$

Here r_{o1} is the output resistance of stage 1. Similarly for r_{o2}, r_{o3} etc. K_{ti} is as earlier the voltage gain.

As previously if the gain is large enough in the first stage noise from subsequent stages can be ignored.

There are three methods one can use for noise analysis of more complex systems such as cascaded network:

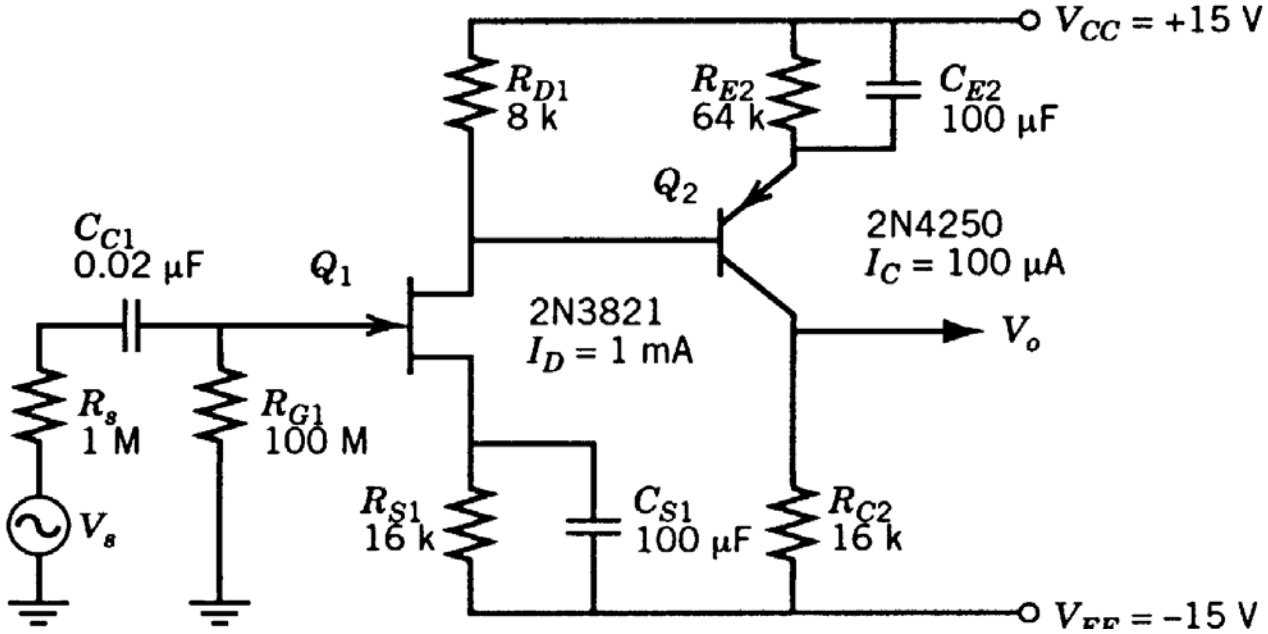
- Manual network analysis (hand calculations),
- use a simulator as say LTspice, or
- measure the system after realisation.

Tricks for simulation (and measurement):
If one is unsure of the impact of noise from a source: simulate only with this source and measure results on the end.

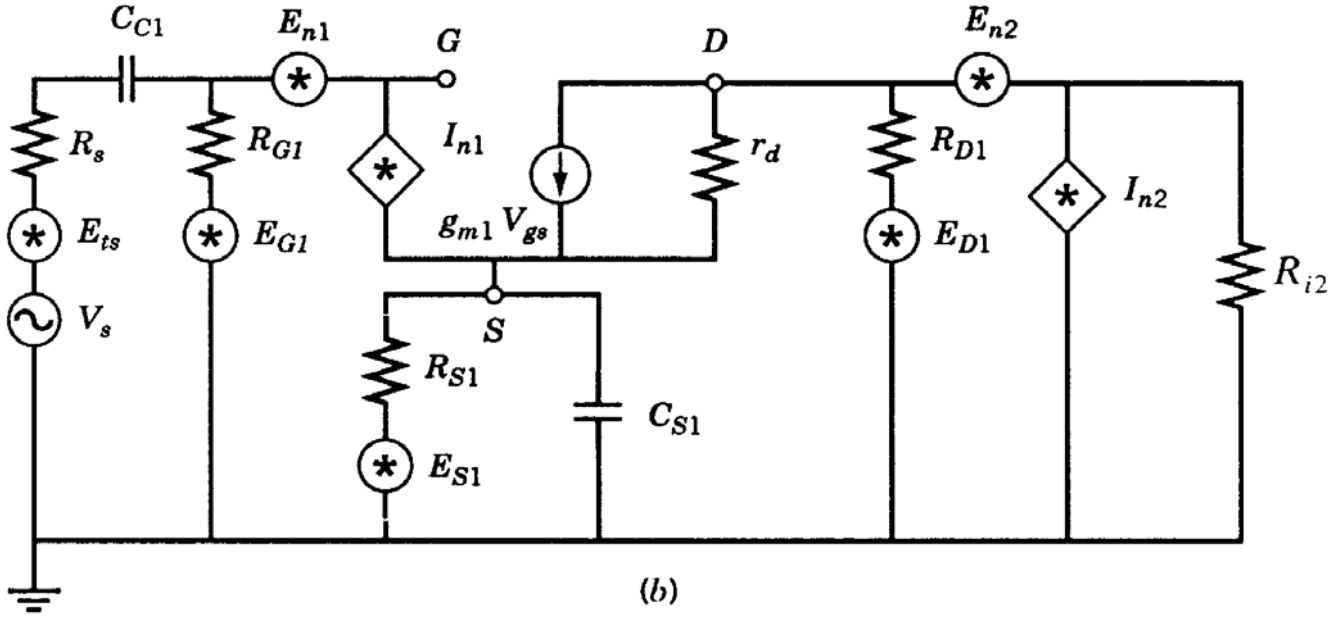
Combined architectures:

Common-Source --- Common-Emitter couple

CS provides high input impedance and high voltage gain.



In the example is an JFET but the considerations applies to MOSFETs also.



The noise figures for this circuit are as follows:

	10Hz	10kHz
E_n	8nV	4nV
I_n	7fA	7fA
R_0	1.1MΩ	570kΩ
$NF@R_0$	0.03dB	0.015dB

The voltage amplification for the CS-stage is:

$$K_{t1} \cong -\frac{g_{m1}R_{L1}}{1+g_{m1}Z_{S1}}$$

R_{L1} and Z_{S1} is given by:

$$R_{L1} = R_{D1} \parallel r_d \parallel R_{i2}$$

and

$$R_{L1} = R_{D1} \parallel r_d \parallel R_{i2}$$

The total voltage gain is:

$$K_{tc} \cong \frac{g_{m1}R_{L1}\beta R_{C2}}{(1+g_{m1}Z_{S1})(r_{x2}+r_{\pi 2})}$$

When $r_{\pi 2} >> R_{D1}$ and $R_{C2} >> r_{o2}$ we have that:

$$K_{tc} \cong \frac{g_{m1}R_{D1}R_{C2}}{r_{e2}}$$

To reduce the E_{n1}-noise contribution from the FET we increase I_{D1}. But this assumes a smaller R_{D1} which means less total gain.

The expression for the equivalent input noise for this circuit is:

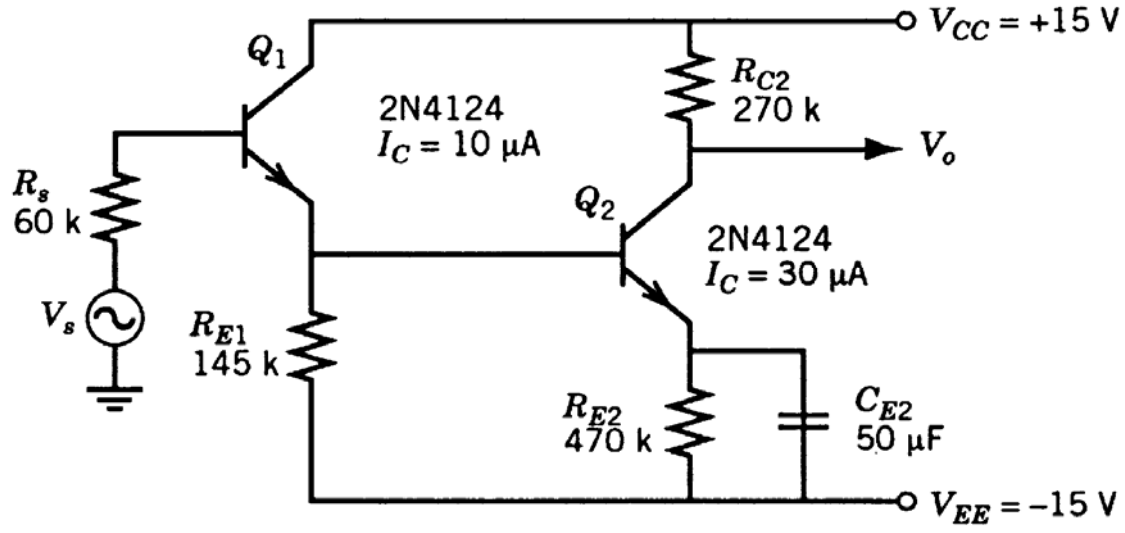
$$E_{ni}^2 = E_{ns}^2 + E_{n1}^2\left(\frac{R_{G1}+R_S}{R_{G1}}\right)^2 + I_{n1}^2\left(R_S - jX_{C1}\right)^2 + \frac{E_{G1}^2 R_S^2}{R_{G1}^2}$$

$$+\frac{E_{S1}^2}{1+\left(\omega R_{S1}C_{S1}\right)^2} + \frac{1}{K_{t1}^2}\left(E_{D1}^2 + E_{n2}^2 + I_{n2}^2 R_{D1}^2\right) + \frac{E_{C2}^2}{K_{tc}^2}$$

- R_{G1} must be large compared to RS
- R_{G1} must be large compared to RS
- C_{S1} must be sufficiently large
- K_{t1} should be large and
- K_{tc} should be great.

Common-collector --- Common-emitter couple

CC-CE has only a little larger E_n than a pure CE stage but can offer higher input resistance and lower input capacitance.



First stage has a gain of approx. 1. The total gain is:

$$K_{tc} = -\frac{\beta_1\beta_2 R_{L1} R_{C2}}{\left(R_S + r_{x1} + r_{\pi 1} + \beta_1 R_{L1}\right)\left(r_{x2} + r_{\pi 2} + \beta_2 Z_{E2}\right)}$$

where

$$R_{L1} = R_{E1} \parallel \left(r_{x2} + r_{\pi 2} + \beta_2 Z_{E2}\right)$$

The expression for K_{tc} can be simplified when $\beta_1 R_{L1} >> (R_S + r_{x1} + r_{\pi 1})$ and $r_{\pi 2} >> r_{x2} + \beta_2 Z_{E2}$:

$$K_{tc} \cong -\frac{R_{C2}}{r_{e2}}$$

Equivalent input noise is:

$$E_{ni}^2 = E_{ns}^2 + E_{n1}^2 + I_{n1}^2 R_S^2 + \frac{E_{n2}^2}{K_{t1}^2} + \left(\frac{I_{n2} R_{E1}}{K'_{t1}}\right)^2 + \left(\frac{E_{E1}}{K'_{t1}}\right)^2 + \frac{E_{C2}^2}{K_{tc}^2}$$

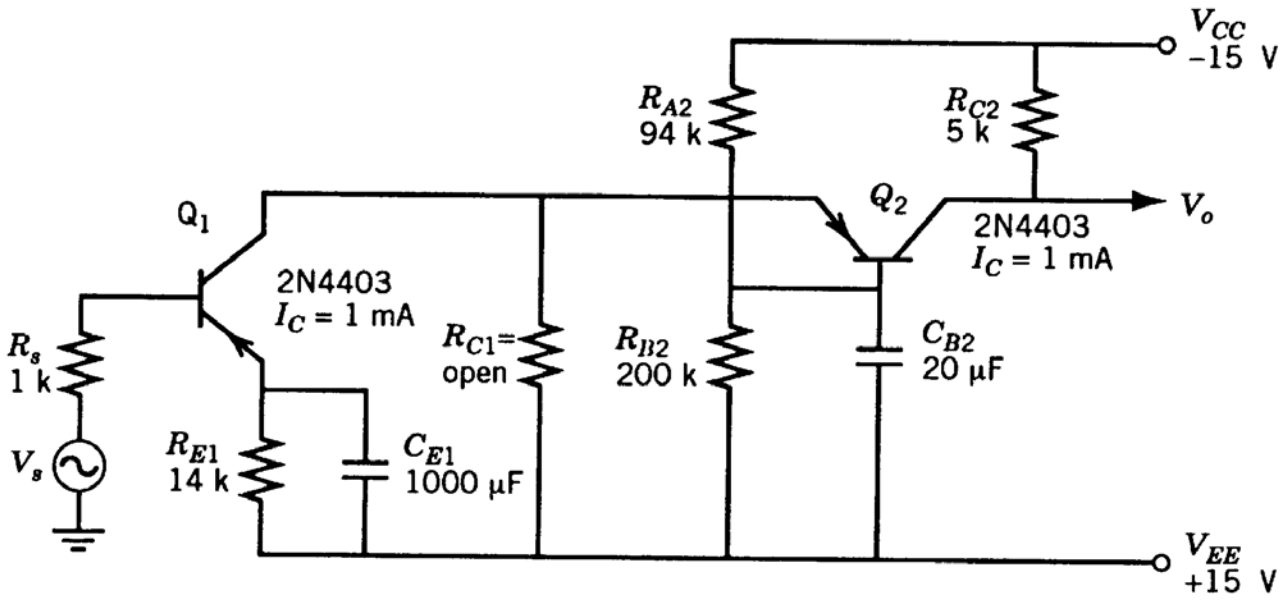
K'_{t1} is the gain in the first CC stage with R_{E1} as load.

$$K'_{t1} = \frac{\beta_1 R_{E1}}{R_S + r_{x1} + r_{\pi 1}} \cong \frac{R_{E1}}{r_{e1} + R_S / \beta_1}$$

- In CC and CD should the emitter resistance be large.

Common-Emitter --- Common base couple

CE-CB has low input capacitance and high output impedance. Due to the low input resistance of the second stage the voltage gain of the first stage will be low. This reduces the high frequency feedback (Miller effect) through $C\mu$ as discussed before. The input capacitance is thus much less than for a regular CE step.



Q1 provides power amplification but not voltage gain (ie Q1 provides a current gain.) Q2 provides a large voltage gain.

R_{C1} is used to provide extra collector current to Q2 when there is a need for large gain-bandwidth.

The total power gain can be expressed as:

$$K_{tc=} = -\frac{\beta_1 R_{L1}}{\left(r_{x1} + r_{\pi 1} + R_S + \beta_1 Z_{E1}\right)} \frac{\beta_2 R_{C2}}{\left(r_{\pi 2} + r_{x2} + Z_{B2}\right)} =$$

$$-\frac{\beta_1 \beta_2 R_{L1} R_{C2}}{\left(r_{x1} + r_{\pi 1} + R_S + \beta_1 Z_{E1}\right)\left(r_{\pi 2} + r_{x2} + Z_{B2}\right)}$$

where

$$R_{L1} = R_{C1} \| \frac{r_{x2} + r_{\pi 1} + Z_{B2}}{\beta_2} \cong r_{e2}$$

When $R_S = 0$ and $R_{C1} >> r_\pi/\beta_2$ we can simplify K_{tc} to:

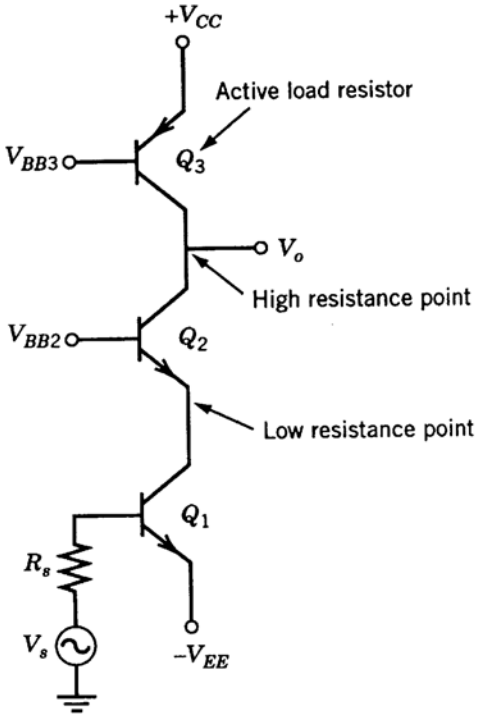
$$K_{tc} \cong -\frac{R_{C2}}{r_{e1}}$$

The equivalent input noise is:

$$E_{ni}^2 = E_{ns}^2 + E_{n1}^2 + I_{n1}^2 R_S^2 + \frac{1}{K_{t1}^2}\left[E_{C1}^2 + E_{n2}^2 + I_{n2}^2 \left(R_{L1} + Z_{B2}\right)^2\right]$$

$$+ \frac{E_{A2}^2}{K_{t1}^2\left[1 + \left(\omega C_{B2} R_{A2}\right)^2\right]} + \frac{E_{B2}^2}{K_{t1}^2\left[1 + \left(\omega C_{B2} R_{B2}\right)^2\right]} + \frac{E_{C2}^2}{K_{tc}^2}$$

Integrated BJT cascade amplifier



Here Q1 acts as a CE-stage and Q2 as a CB-stage. Q3 is load. The total voltage gain is:

$$K_{tc} \cong -\frac{r_{o3}}{r_{e1}}$$

The equivalent input noise is:

$$E_{ni}^2 = E_{ns}^2 + E_{n1}^2 + I_{n1}^2 R_S^2 + \frac{1}{K_{t1}^2}\left[E_{n2}^2 + I_{n2}^2 \left(r_{e2} + Z_{B2}\right)^2\right] + \frac{E_{o3}^2}{K_{tc}^2}$$

Here is $K_{t1}=r_{e2}/r_{e1}$. Since the collector currents are equal so will $K_{t1}=1$. Z_{B2} is the impedance to V_{BB2} (should be low). Since R_{e2} also is small the contribution from I_{n2} should also be ignorable.

The noise voltage from Q3 is:

$$E_{o3} = E_{n3} K_{t3}$$

The gain in Q3 is:

$$K_{t3} = \frac{r_{o2}}{r_{e3}} \cong K_{tc}$$

With these simplifications the expression for the equivalent input noise is reduced to:

$$E_{ni}^2 = E_{ns}^2 + E_{n1}^2 + I_{n1}^2 R_S^2 + E_{n2}^3 + E_{n3}^2$$

$$\cong E_{ns}^2 + 3E_n^2 + I_{n1}^2 R_S^2$$

Differential amplifier

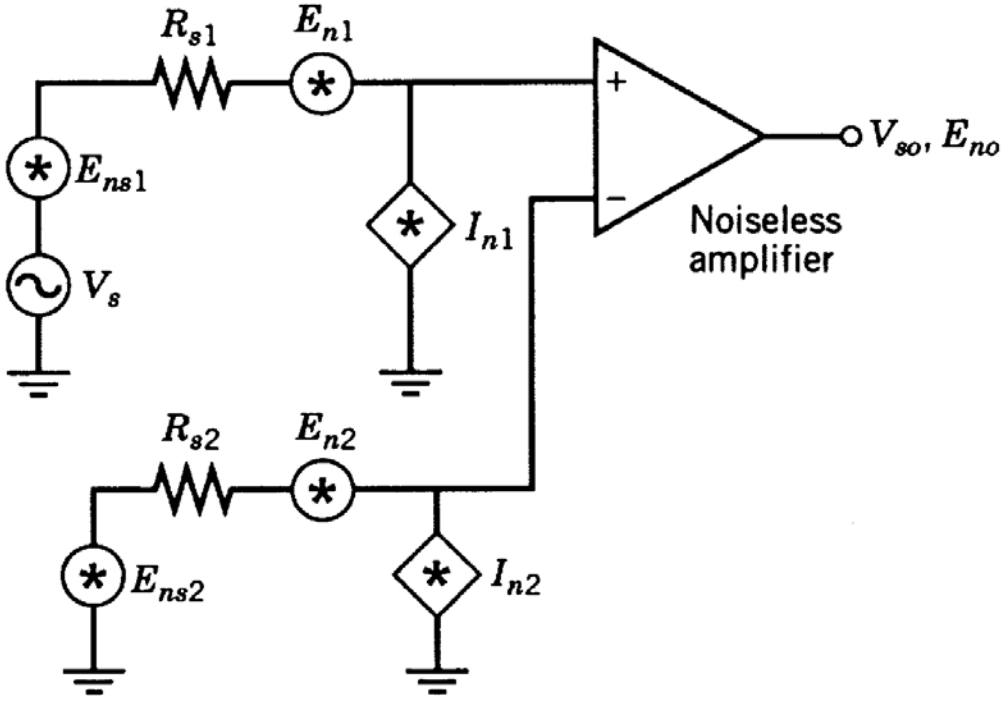
The two input signals V_1 and V_2 can be defined relative to a common value (common-mode) V_C, and a difference value V_D.

$$V_C = \frac{V_1 + V_2}{2}, \quad \text{and} \quad V_D = V_1 - V_2$$

We will then have:

$$V_1 = \frac{V_D}{2} + V_C, \quad \text{and} \quad V_2 = -\frac{V_D}{2} + V_C$$

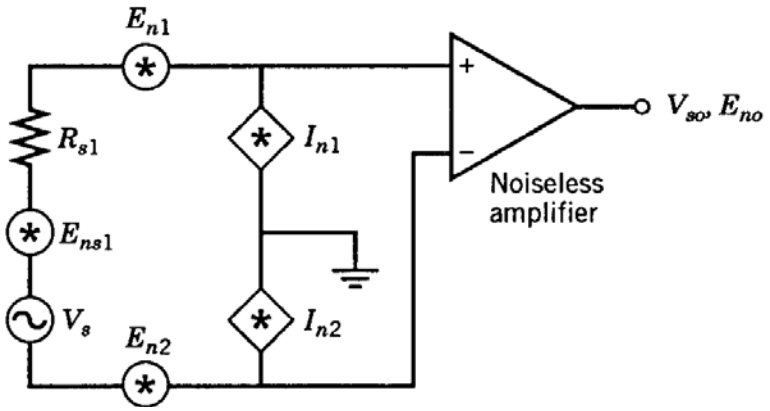
The noise schematic looks as follows:



The equivalent input noise is:

$$E_{ni}^2 = E_{ns1}^2 + E_{ns2}^2 + E_{n1}^2 + E_{n2}^2 + I_{n1}^2 R_{S1}^2 + I_{n2}^2 R_{S2}^2$$

Differential connection:



We assume that the positive and negative input has the same noise characteristics and adds together the En and In-values for the amplifier.

$$E_{nT}^2 = E_{n1}^2 + E_{n2}^2 = 2E_{n1}^2$$

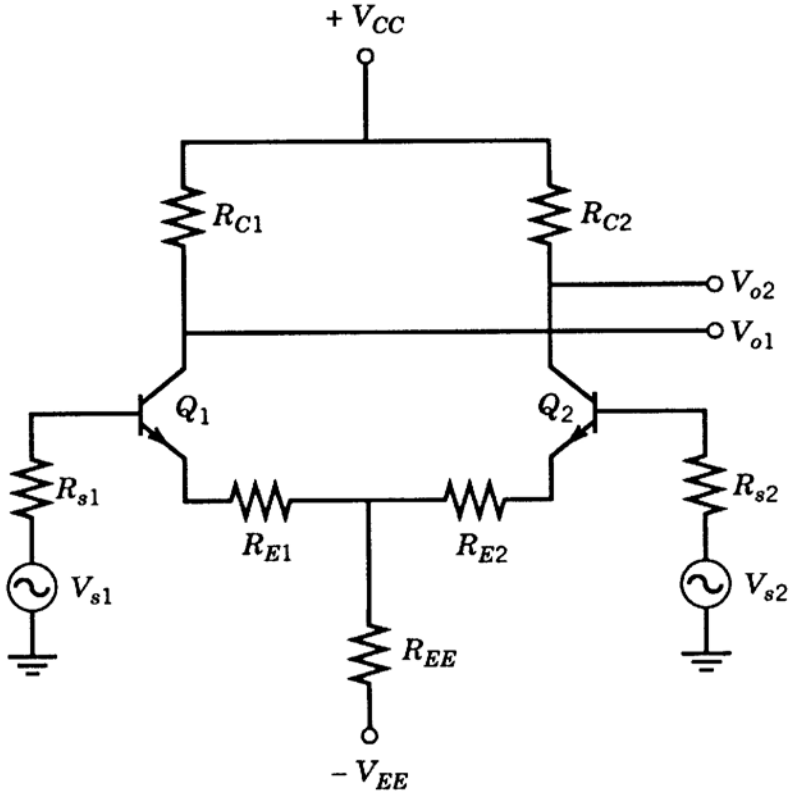
$$I_{nT}^2 R_S^2 = I_{n1}^2 \left(\frac{R_S}{2} \right)^2 + I_{n2}^2 \left(\frac{R_S}{2} \right)^2 = \frac{I_{n1}^2}{2} R_S^2$$

When we put together with the source resistance, we obtain the equivalent input noise:

$$E_{ni}^2 = E_{ns}^2 + 2E_{n1}^2 + \frac{I_{n1}^2 R_S^2}{2}$$

Noise model for the differential amplifier.

Example of differential stage:



a)

Voltage gain of differential signal:

$$K_{dm} = \frac{V_{o2} - V_{o1}}{V_{s2} - V_{s1}} = \frac{-2R_C}{\frac{1}{g_m} + R_E + \frac{R_S}{\beta}}$$

Here is $g_m = 1/r_e$ for each of the transistors.

Assuming identical transistors and $R_{C1} = R_{C2} = R_C$, $R_{E1} = R_{E2} = R_E$ and $R_{S1} = R_{S2} = R_S$.

For the typical cases where $R_E = 0$ and $R_S << r_\pi$ we can simplify K_{dm} to:

$$K_{dm} \cong \frac{-2R_C}{r_e}$$

b)

Gain for the common voltage signal:

$$K_{cm} = \frac{V_{o2} + V_{o1}}{V_{s2} + V_{s1}} = \frac{-R_C}{\frac{1}{g_m} + R_E + \frac{R_S}{\beta} + 2R_{EE}}$$

When R_{EE} is large we get:

$$K_{cm} \cong \frac{-R_C}{2R_{EE}}$$

c)

Differential voltage gain between outputs with common input signal:

$$K_{dc} = \frac{V_{o2} - V_{o1}}{2V_S} = \frac{R_{C1}\left(\frac{R_{S2}}{\beta_2} + \frac{1}{g_{m2}} + R_{E2}\right) - R_{C2}\left(\frac{R_{S1}}{\beta_1} + \frac{1}{g_{m1}} + R_{E1}\right)}{2R_{EE}\left(\frac{R_{S2}}{\beta_2} + \frac{1}{g_{m2}} + R_{E2} + \frac{R_{S1}}{\beta_1} + \frac{1}{g_{m1}} + R_{E1}\right)}$$

Ideally if the inputs were completely symmetrical K_{dc} should be 0. When this is not the case one can reduce K_{dc} say by increasing R_{EE}.

Eni:

$$E_{ni}^2 = E_{S1}^2 + E_{S2}^2 + E_{n1}^2 + E_{n2}^2 + I_{n1}^2 R_{S1}^2 + I_{n2}^2 R_{S2}^2$$
$$+ E_{E1}^2 + E_{E2}^2 + \frac{E_{C1}^2 + E_{C2}^2}{K_{dm}^2} + \frac{E_{EE}^2 + E_{VEE}^2 + E_{VCC}^2}{K_{dc}^2}$$

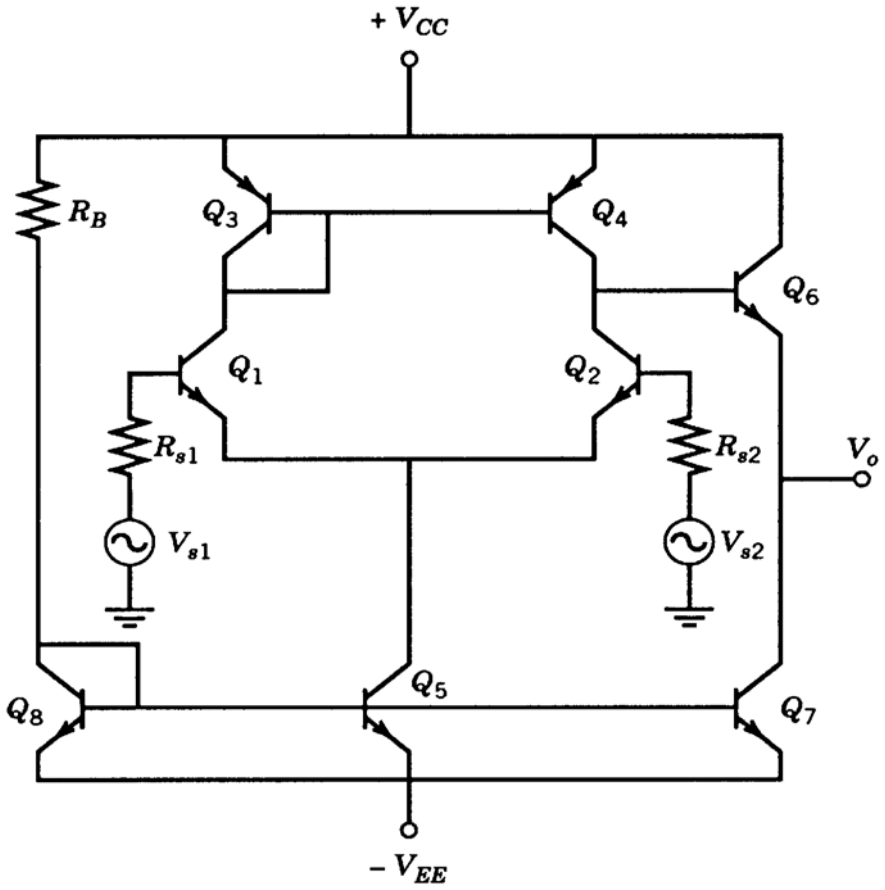
Here is E_{VEE} and E_{VCC} noise on the voltage supplies.

Integrated BJT differential amplifier

It can be relatively large variation in process parameters for integrated circuits from production to production. However between the elements on the same circuit the variation will be little. This is exploited by basing designs more on the symmetry between the elements than on their actual values. On integrated circuits the common-mode noise rejection is improved. On the other hand, on integrated circuits requires compromises that may give more noise than when optimizing a process for a single isolated component. Examples of these compromises are:

- long insulation diffuse sessions,
- active loads, and
- power sources.

The figure shows the integrated version of the differential amplifier we studied previously.



Equivalent input noise:

$$E_{ni}^2 = E_{s1}^2 + E_{s2}^2 + E_{n1}^2 + E_{n2}^2 + I_{n1}^2 R_{s1}^2 + I_{n2}^2 R_{s2}^2$$

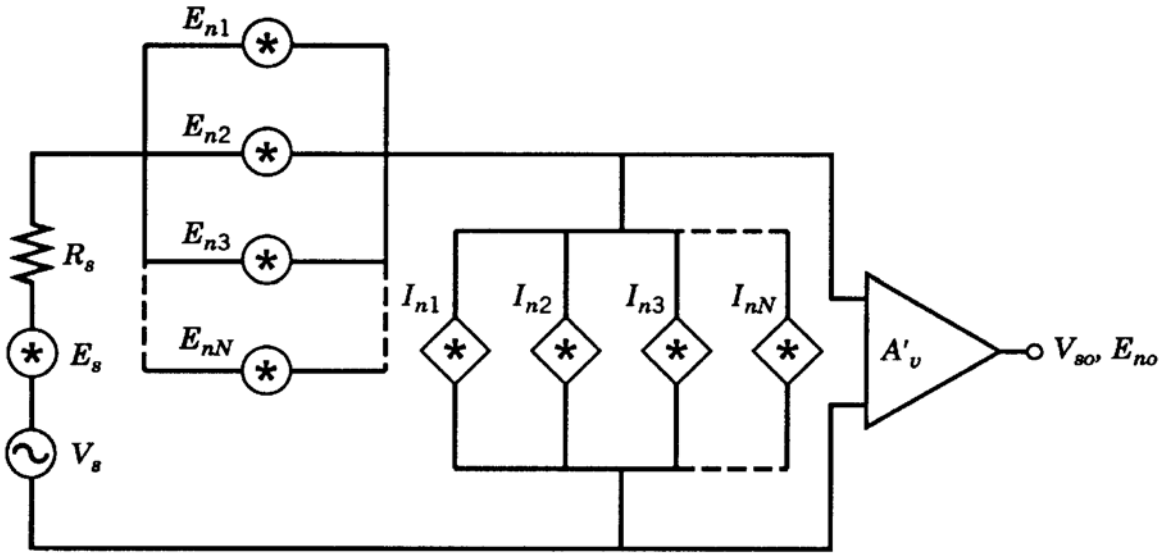
$$+ E_{n3}^2 + E_{n4}^2 + \frac{E_{n5}^2 + E_{VEE}^2 + E_{VCC}^2}{K_{dc}^e}$$

Since common-mode rejection is high and all active circuits have approximately the same geometry and noise mechanisms, E_{ni} will be reduced to:

$$E_{ni}^2 = 2E_S^2 + 4E_n^2 + 2I_n^2 R_S^2$$

Parallel amplifier stages

What when several amplifiers are placed in parallel? Schematically, we can draw noise sources as follows:



We have:

$$E'_n = \frac{E_n}{\sqrt{N}} \quad \text{and} \quad I'_n = I_n\sqrt{N}$$

A new optimal source resistance can be defined as:

$$R'_o = \frac{E'_n}{I'_n} = \frac{R_o}{N}$$

Gain is given by:

$$A'_v = NA_v$$

A significant contribution to the En -noise in a BJT is the base resistance r_x. The base resistance can be reduced by placing the base contacts all the way around the emitter and the closest possible on the emitter. In FETs it is determined by the channel

resistances, and by g_m. Low resistance and high g_m can be achieved by having a large W/L ratio. By parallelising both the $C'\mu$ and the Miller effect is increased.