F9 (Mot 6): Noise in field effect transistors

Two types of field effect transistors:
• MOSFET: capacitive control of the channel
• JFET: Variation of the width of a reverse biased diode where the depletion zone determines the width of the channel. GaAs FETs have a similar behaviour.

Noise Mechanisms

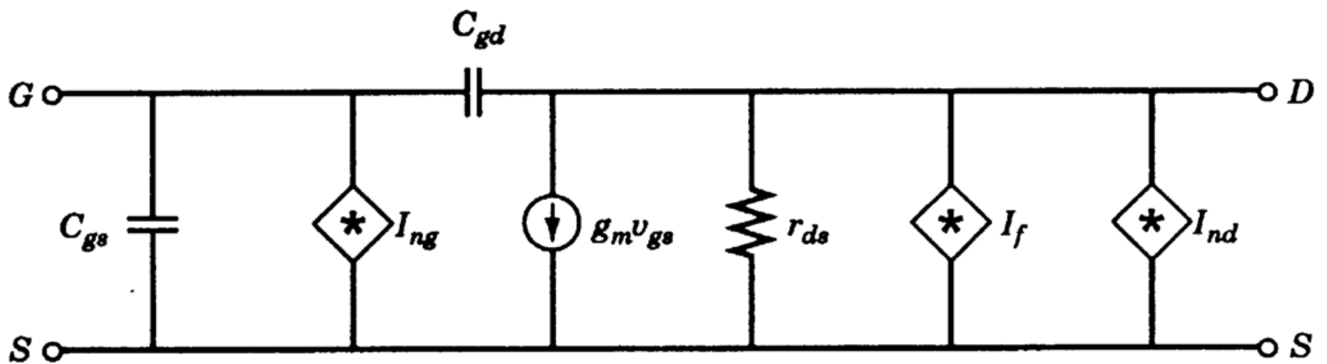


Figure 6-1 Small-signal noise equivalent circuit for a FET.

The figure shows a typical model extended with noise models.

Elements of a typical model:
C_{gs}, C_{gd}: Capacitance between gate and source and between gate and drain.
$g_m v_{gs}$: Current between source and drain.
r_{ds}: Resistance in the channel between drain and source.

Noise Models:
Gate:

- I_{ng}: Shot-noise in leakage current through the gate (especially JFET) and
- thermal fluctuations from the drain node, which affects the gate node

Drain:

- I_{nd}: Thermal excitations in the channel.
- I_f: Flicker noise in the channel

The thermal noise mentioned under the gate-section above and I_{nd} are both due to thermal noise in the channel and they are partially correlated at higher frequencies.

En-In representation of noise

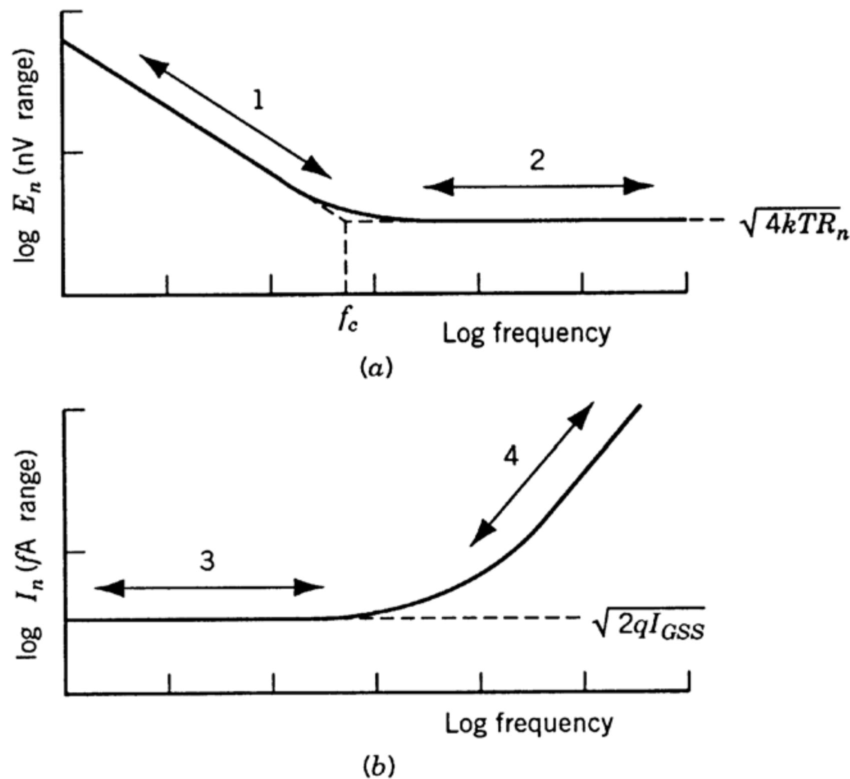


Figure 6-2 Typical noise behavior of a FET.

The curves above show the typical trends for respectively *En* and *In*. *En* is low and flat at high frequencies but grows at lower frequencies due flicker noise. *In* is low and flat at low frequencies but grows linearly with frequency above a corner frequency.

En:

The constant, frequency independent contribution of *En* at higher frequencies are due to thermal noise in the channel.

The thermal noise in the channel can be modelled by a serially connected resistance at the gate with size:

$$R_n \approx \frac{2}{3g_m}$$

The noise voltage is calculated in the usual way:

$$E_n = \sqrt{4kTR_n}$$

To minimize noise in region two g_m should be large.

In:

The *In*-noise at lower frequencies (region three) is due to shot-noise in the dc-reverse bias in JFETs and shot-noise leakage currents in the MOSFET. This noise is "white" and has usually no 1/f-component.

$$I_n = \sqrt{2qI_{GSS}}$$

The rise in region four is due to the real part of the input admittance.

Modified model for slightly higher rates:
We will now study the effect of the feedback caused by C_{gd} and will temporary forget the noise.

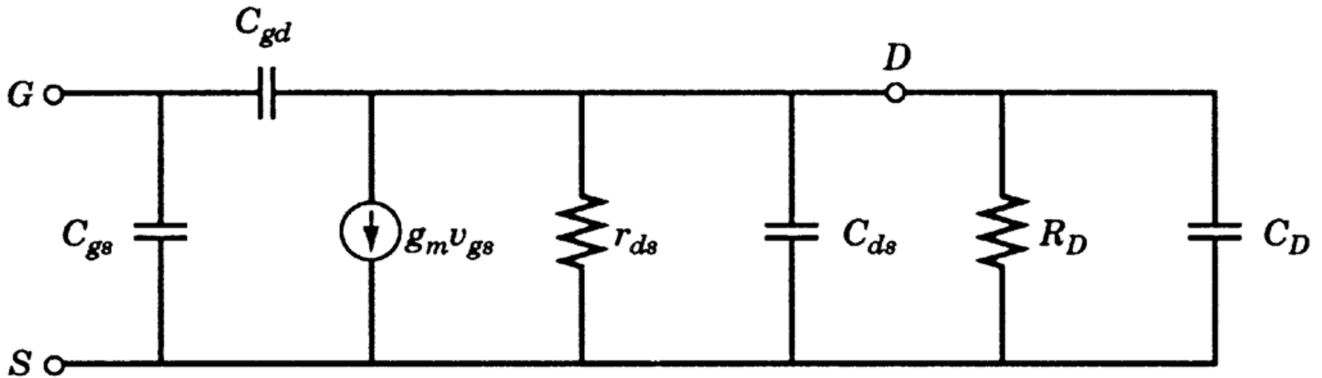
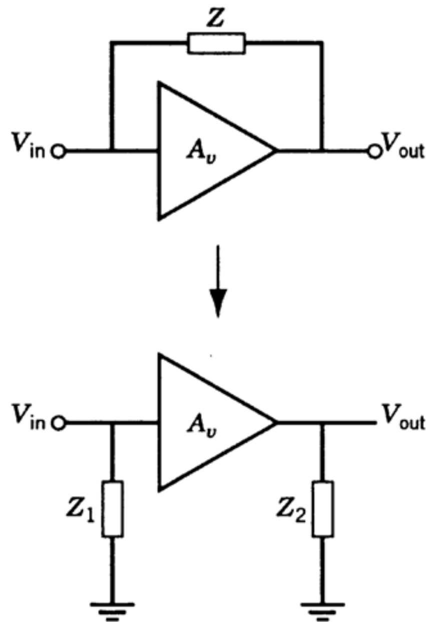


Figure 6-3 Circuit to determine high-frequency I_n noise of a FET.

We now also include C_{ds}. External loads are represented by a resistance and a capacitance. Total resistive load R_L is now the parallel value of the internal resistance r_{ds} and the external R_D. Total capacitive load C_L is the parallel value of the internal capacitance C_{ds} and the external C_D.

The effect of the feedback capacitor C_{gd} can be made visible by use of the Millers theorem.

Millers theorem:



With a voltage gain A_v the feedback element Z can be divided into two impedance Z_1 and Z_2 given by the following expression:

$$Z_1 = \frac{Z}{1 - A_v}$$

and

$$Z_2 = \frac{Z}{1 - 1/A_v}$$

With the elements of the MOSFET we get:

$$A_v = \frac{\partial v_{ds}}{\partial v_{gs}} = \frac{-g_m v_{gs} Z_L}{v_{gs}} = -g_m Z_L$$

Where Z_L is determined by

$$Z_L = R_L \parallel \left(1/ j\omega C_L\right)$$

The feedback element Z is given by

$$Z = 1/ j\omega C_{gd}$$

We want to analyze the input and insert in the expression of the Z1, so that we get:

$$Z_1 = \frac{1 + j\omega R_L C_L}{-\omega^2 R_L C_L C_{gd} + j\omega C_{gd}\left(1 + g_m R_L\right)}$$

The admittance is the inverse of Z_1 and we get:

$$Y_1 = \frac{-\omega^2 R_L C_L C_{gd} + \omega^2 C_{gd}\left(1 + g_m R_L\right) R_L C_L + j\omega C_{gd}\left[1 + g_m R_L + \omega^2 R_L^2 C_L^2\right]}{1 + \omega^2 R_L^2 C_L^2}$$

[We have also multiplied by $(1-j\omega R_L C_L)$ in the numerator and denomerator.]

Real part of Y1 is:

$$\operatorname{Re} Y_1 = \frac{\omega^2 g_m R_L^2 C_{gd} C_L}{1 + \omega^2 R_L^2 C_L^2}$$

The real part will be represented as a resistance. (In our case Z1 will be between the gate and source.)

$$R_{eq} = \frac{1}{\operatorname{Re} Y_1} = \frac{1 + \omega^2 R_L^2 C_L^2}{\omega^2 g_m R_L^2 C_{gd} C_L}$$

Normally, $\omega^2 R_L^2 C_L^2 << 1$ so that expression can be simplified to

$$R_{eq} \cong \frac{1}{\omega^2 g_m R_L^2 C_{gd} C_L}$$

Imaginary part of Y1 is:

$$\operatorname{Im} Y_1 = \frac{j\omega\left[C_{gd}\left(1 + g_m R_L\right) + R_L^2 C_L^2 C_{gd} \omega^2\right]}{1 + \omega^2 R_L^2 C_L^2}$$

This means that we have an equivalent capacitance between gate and source which is:

$$C_{eq} = \frac{C_{gd}\left(1 + g_m R_L\right) + R_L^2 C_L^2 C_{gd} \omega^2}{1 + \omega^2 R_L^2 C_L^2}$$

Also this expression can be simplified (because $\omega^2 R_L^2 C_L^2 << 1$) to

$$C_{eq} \cong C_{gd}\left(1 + g_m R_L\right) + R_L^2 C_L^2 C_{gd}\omega^2$$

Let us see a little more on the expression we found for the equivalent resistance:

$$R_{eq} \cong \frac{1}{\omega^2 g_m R_L^2 C_{gd} C_L}$$

We see that this resistance decreases with the square of the frequency. We will have an effective noise current on the basis of this: $\sqrt{(4kT/R_{eq})}$. This results in the rise in *In* at the higher frequencies as illustrated in the figure presented earlier.

The noise elements *En* and *In* are correlated at high frequencies since they both have a significant contribution from the same source: The thermal noise in the channel resistance. This means that the noise is somewhat greater and we must include an additional correlation term.

Example: Calculation of the input conductance
Target: Find the input inductance G_i and noise current I_n for a FET where:
$gm=500\mu S$, $C_{gd}=1pF$, $C_L=3pF$ og $R_L=200k\Omega$

We use the expression for "Re Y" that we have previously found and plot the curve:

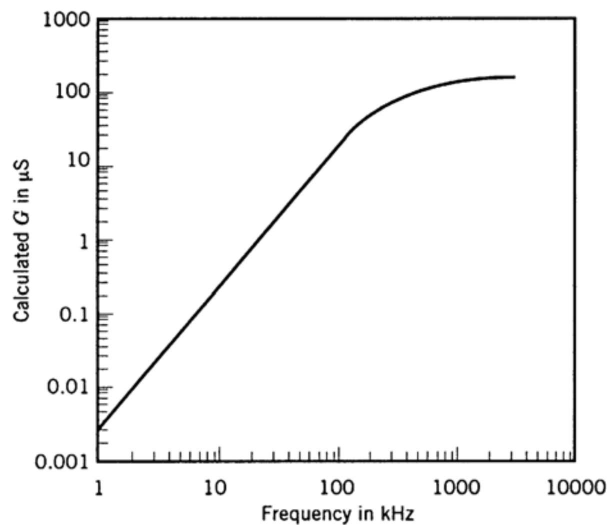


Figure 6-5 Calculated input conductance of a FET amplifier.

The noise current I_n can be calculated with $\sqrt{(4kTG_i)}$ and is shown in the plot below:

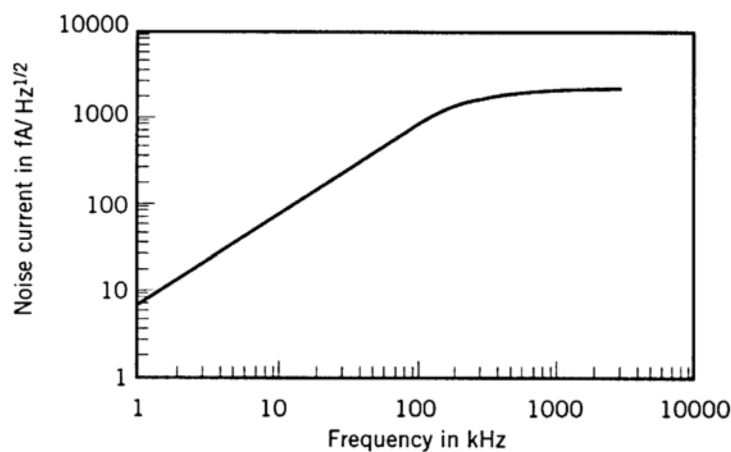


Figure 6-6 Calculated equivalent input noise current of a FET amplifier.

Regular expressions for FET

First, we ignore the noise and consider a standard N-MOSFET.

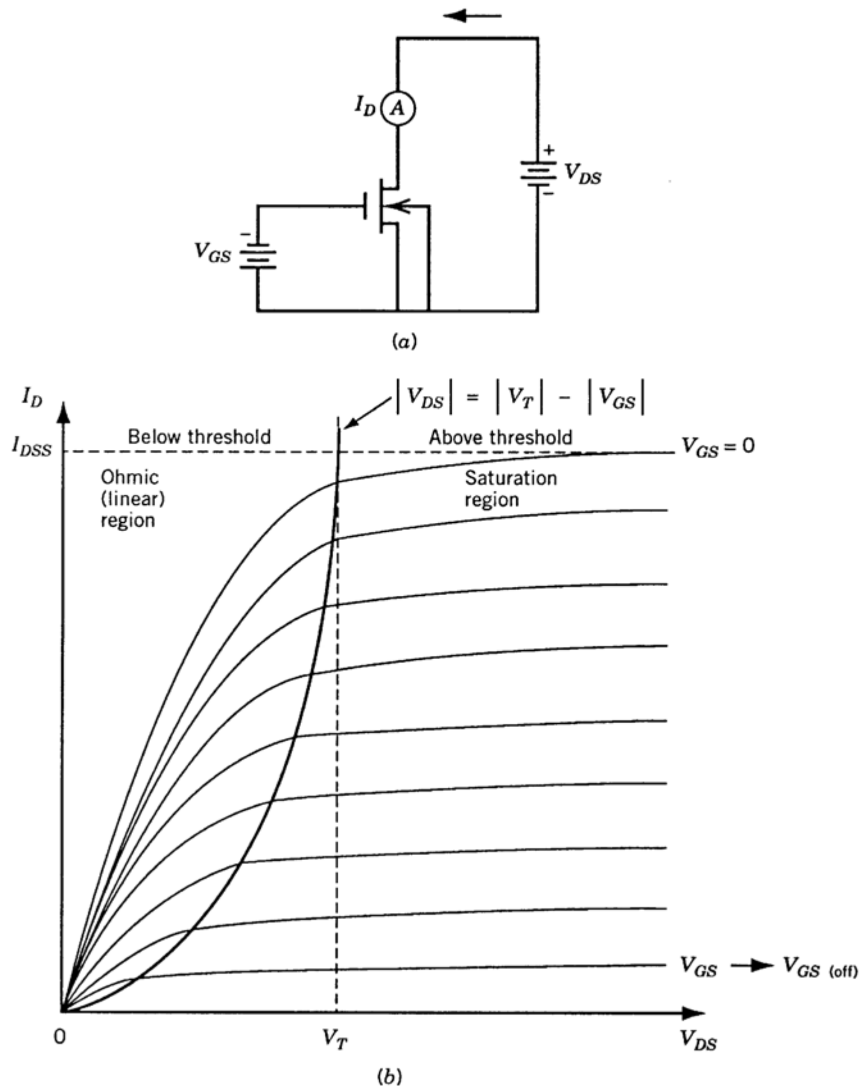


Figure 6-7 Determination of *n*-channel MOSFET *V–I* characteristics: (*a*) test circuit and (*b*) output characteristics.

The transistor can be in cut-off, linear region or in saturation. In the linear region the current I_{ds} has a strong dependence on V_{ds}, while in saturation is the dependence weaker. The linear range is often also called for the resistive region.

In saturation Ids can be expressed as follows:

$$I_D = K_p \left(\frac{W}{L} \right) (V_{GS} - V_T)^2 (1 + \lambda V_{DS})$$

Here λ modulates the dependency on the channel length, V_T is the threshold voltage, W is the channel width, while L is the channel length. The trans-conductance K_P can be expressed as:

$$K_p = \frac{\mu_0 C_{ox}}{2}$$

Here is μ_0 the mobility of an n-channel and Cox the gate oxide capacitance.

Some examples of sizes from the book:

	n-kanal	p-kanal	Benevning
K_P	41.8	15.5	µA/V²
V_T	0.79	-0.93	V
λ	0.01	0.01	1/V

$$g_m = \left.\frac{\partial I_D}{\partial V_{GS}}\right|_{Q-po\text{int}} = 2K_p\left(\frac{W}{L}\right)(V_{GS}-V_T)(1+\lambda V_{DS}) = \frac{2I_D}{V_{GS}-V_T}$$

$$g_{ds} = \frac{\partial I_D}{\partial V_{DS}} = \left.\frac{1}{r_{ds}}\right|_{Q-po\text{int}} = \lambda K_p\left(\frac{W}{L}\right)(V_{GS}-V_T)^2(1+\lambda V_{DS}) = \lambda I_D$$

Key sizes are the trans-conductance ...
.. and the output conductance ...
They can be calculated from the expression for I_{ds}.

The capacitances C_{gd} and C_{gs}.

These capacitances will vary depending on the transistor region:

	Region		
	Cut-off	*Linear*	*Saturation*
C_{gd}	$C_{OX}WL_D$	$C_{OX}WL_D+(1/2)WLC_{OX}$	$C_{OX}WL_D$
C_{gs}	$C_{OX}WL_D$	$C_{OX}WL_D+(1/2)WLC_{OX}$	$C_{OX}WL_D+(2/3)WLC_{OX}$

Cox may be defined as:

$$C_{ox} = \frac{\varepsilon_0 \varepsilon_{SiO_2}}{t_{ox}}$$

... and stated in fF/um²

Example: Find I_D, g_m and g_{ds}..
N-MOSFET with W/L = 50, VGS = VDS = 1V and 5V. Use additional values from the table.

First, we check whether it is in saturation?
VDS = 5V ≥VGS-VT=1-0.79=0.21V
Yes, it is in saturation!

Then we will calculate the current in accordance with the equation for I_{DS}.

$$I_D = \left(41.8\mu A/V^2\right)(50)(1-0.79)^2 V^2 (1.05) = 97.2\mu A$$

We find g_m and g_{ds}:

$$g_m = 2K_p(W/L)(V_{GS}-V_T)(1+0.01V_{DS}) =$$
$$2\left(41.8\mu A/V^2\right)(50)(0.21V)(1.05) = 926\mu\, A/V = \underline{\underline{926\mu S}}$$

$$g_{ds} = \lambda I_D = \left(0.01V^{-1}\right)(97.2\mu A) = \underline{\underline{0.972\mu S}}$$

$$r_{ds} = 1/g_{ds} = 1/0.972\mu S = 1.029M\Omega$$

Calculation of noise in a MOSFET.

As previously mentioned we have three sources in our noise model: I_{ng}, I_{nd} and I_f..

I_{ng}:

I_{ng} is mainly shot-noise and can be modelled with:

$$I_{ng}^2 = 2qI_{dc}$$

I_{ng} is dominant at low frequencies.

I_{nd}:

The increase in I_n at high frequencies is due to the Miller coupling through C_{gd} of noise in the channel. This noise is at the output:

$$I_{nd}^2 = \frac{8kTg_m}{3}$$

This is the same noise that we would have had if we had a parallel resistance in the channel with a size of:

$$R_{DRAIN} = \frac{3}{2g_m}$$

I_f:

The flicker noise is also between source and drain:

$$I_f^2 = \frac{K_F I_{DQ}^{A_F}}{fC_{ox}L_{eff}^2}$$

Total noise power at the output is:

$$I_{no}^2 = I_{nd}^2 + I_f^2$$

We will find the equivalent noise at the input and then have to first find the gain of the transistor. In this case we are considering current at the output and voltage at the input:

$$K_{tr} = \frac{i_{d(signal)}}{v_{gs(signal)}} = -g_m$$

We get the equivalent noise at the input by dividing the noise on the output by the gain:

$$E_{ni}^2 \approx \frac{I_{nd}^2}{g_m^2} + \frac{I_f^2}{g_m^2} \approx E_n^2$$

We insert for I_{nd} and I_f:

$$E_{ni}^2 \approx \frac{8kT}{3g_m} + \frac{K_F}{2K_p f C_{ox} W L_{eff}} \approx E_n^2$$

($AF \approx 1$, $L \approx L_{eff}$, $(1-\lambda V_{DS}) \approx 1$)

The first term corresponds to the noise voltage from a resistor with size:

$$R_n = \frac{2}{3g_m}$$

Example: Find E_{ni}

We use the same transistor as we considered previously. In addition:
Leakage current I_{DC}: 100fA,
C_{ox}=0.7fF/µm², Δf=1Hz, fc=1kHz,
K_F=3.6x10^-30C²/Vs, A_F=1 and

$$L_{eff} = L_{drawn} - L_{delta} = 3(1.2\mu m) - 0.365\mu m = 3.235\mu m$$

Solution:
First we find shot-noise at the input:

$$I_{ng}^2 = 2qI_{dc} = 2(1.602\times 10^{-19})(10^{-13}) = 3.2\times 10^{-32}\,A^2/Hz$$

$$I_{ng} = 0.18\,fA/Hz^{1/2}$$

Then we find the thermal noise in the channel:

$$I_{nd}^2 = \frac{8kTg_m}{3} = 2(1.6\times 10^{-20})(926\times 10^{-6})/3 = 9.88\times 10^{-24}\,A^2/Hz$$

$$I_{nd} = 3.14\,pA/Hz^{1/2}$$

$$R_{DRAIN} = \frac{3}{2g_m} = \frac{3}{2\times 926\times 10^{-6}} = 1.62k\Omega$$

Equivalent resistance for this noise is:

Flicker noise calculated:

$$I_f^2 = \frac{K_F I_{DQ}^{A_F}}{f C_{ox} L_{eff}^2}$$

$$I_f^2 = \frac{\left(3.6\times10^{-30}\right)\left(97.2\times10^{-6}\right)}{(1000)\left(0.7\times10^{-15}\right)(3.235)^2} = 4.77\times10^{-23} A^2 / Hz$$

$$I_f = 6.9\, pA / Hz^{1/2}$$

Total noise in the drain-source channel is:

$$I_{no}^2 = I_{nd}^2 + I_f^2$$

$$I_{no}^2 = \left(9.88\times10^{-24} + 4.77\times10^{-23}\right) A^2 / Hz$$

$$I_{no}^2 = 5.76\times10^{-23} A^2 / Hz$$

$$I_{no} = 7.59\, pA / Hz^{1/2}$$

So we find the equivalent input noise:

$$E_{ni}^2 = \frac{5.76\times10^{-23}}{\left(926\times10^{-6}\right)^2} = 6.71\times10^{-17} V^2 / Hz$$

$$E_{ni} = 8.19 nV / Hz^{1/2}$$

Some comments:

- Flicker noise is dominant at 1kHz

- The proportion of E_{ni}^2 due to I_{nd} is equivalent to placing a resistance at the gate (in series) with size:

$$R_n = \frac{2}{3g_m} = \frac{2}{3(926\times10^{-6})} = 720\Omega$$

How to achieve low noise?

Let us study the equation we found for the equivalent input noise:

$$E_{ni}^2 = \frac{8kT}{3g_m} + \frac{K_F}{2K_p f C_{ox} W L_{eff}} = E_n^2$$

We should have a large g_m which means that we should have a large W/L ratio and a high idle power. Creating a large transistor will also reduce the flicker noise and, thus, corner frequency (ie the frequency where the flicker noise is the same size as other sources.)

Example: Determine the corner frequency

At the corner frequency the contributions are equally large:

$$E_f^2 = E_{nd}^2$$

Inserted we get:

$$f_c = \frac{3K_F I_{DQ}^{A_F}}{8kTg_m C_{ox} L_{eff}^2}$$

After the values have been inserted and calculated we get:

$$f_c = 4.83kHz$$