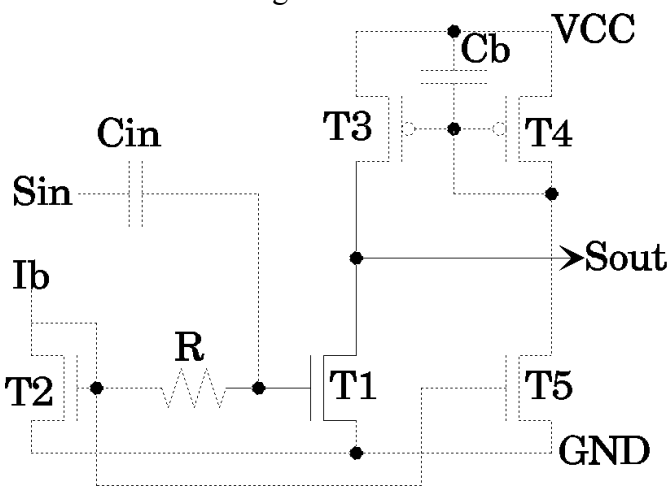
INF 5460 Electrical noise -- calculation and countermeasures

Mandatory task number 3.

The deadline for delivery: 30 April (at 23:59).
Evaluation: Approved / Not approved.
The tasks are delivered on an individual basis. The report has to contain schematics that have been used, simulation results and text that explain what has been done as well as an analysis of the results. The report is sent as email attachment.

1. Common Source

We will first look at a common source stage.



The central element is the transistor T1. The other components are used to provide correct bias. The T1 source is connected to ground (common), while the input signal on the gate will be amplified to the T1 drain.

We wish only to amplify a narrow frequency bandwidth and can ignore DC-value of the input signal. We leverage this to provide the T1 gate the DC value that provides optimal performance. We place a compensator (Cin) between Sin and the T1 gate to achieve DC isolation. Capacitors must be chosen so that the frequency we want to amplify is not muted too much of the capacitor.

The T1 working current is selected by an external current source at the input Ib. The circuit is based on multiple current mirrors. The current is reflected through T2 to T1 and T5, and the current through T4 is reflected to T3. In the current mirrors the gate length of T2, T1 and T5 should be equal and the gate length of T4 and T3 should be equal. To simplify a bit we choose to start with setting the width of the transistors T2, T1 and T5 as well as the transistor T3 and T4 equal. Then all the local currents will be equal to the reference current Ib. (In an actual realization, we will let currents through T2, T4 and T5 to be minimal in order to save power. Proper current in T1 and T3, will be achieved through the choice of the width ratio of the current mirrors.)

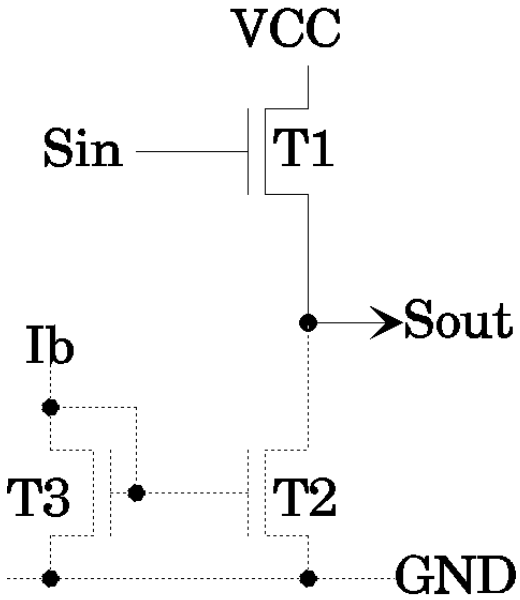
Parameters:
We will focus on the amplification of a signal at 1MHz. During noise analysis, we calculate the noise level between 0.8MHz and 1.2MHz. Let the input signal have amplitude on 1mV.

Initially we let the NMOS transistor lengths be 0.35µm and the PMOS transistor length to be 2µm. The NMOS transistors may have a width of 35µm and the PMOS transistors 20µm width. We use the models MODN and MODP as in mandatory number 2. VCC is 3.3V. Start by giving Cb a very low value . R can be set to 1kΩ. We start with a bias current Ib = 10µA.

a) How large must Cin be to not mute the signal more than about 10% in this case?
b) How large must R be to not contribute significantly (<10%) thermal noise?
c) What does the Cb do? How much noise reduction can we achieve with Cb and how large must Cb be to achieve this? What is the gain, noise on the output and equivalent input noise now?
We entitle in the following the amplifier with the Cin, R and Cb you have found for the reference setup.
d) Experiment by doubling the width of the NMOS transistor, the length of the NMOS transistor, the PMOS transistor width and length of the PMOS transistor. Find the output noise, equivalent input noise as well as the gain for these 5 setups (reference + 4 variations).
e) Increase the power Ib in steps of 10µA from 10µA to 100µA, and find the output noise, equivalent input noise and gain. Plot the equivalent input noise as a function of current.
f) Replace MODN and MODP (3.3V models) with MODNH and MODPH (5V models). Compare the noise with your results in the reference setup.
g) Replace the MOS transistor with NPN and PNP transistors and compare with the reference setup.

2. Common Drain (source follower)

We will in the following look at a common drain stage ie the drain is connected to a stable voltage potential while the signal propagates from the gate to the source of the transistor T1.

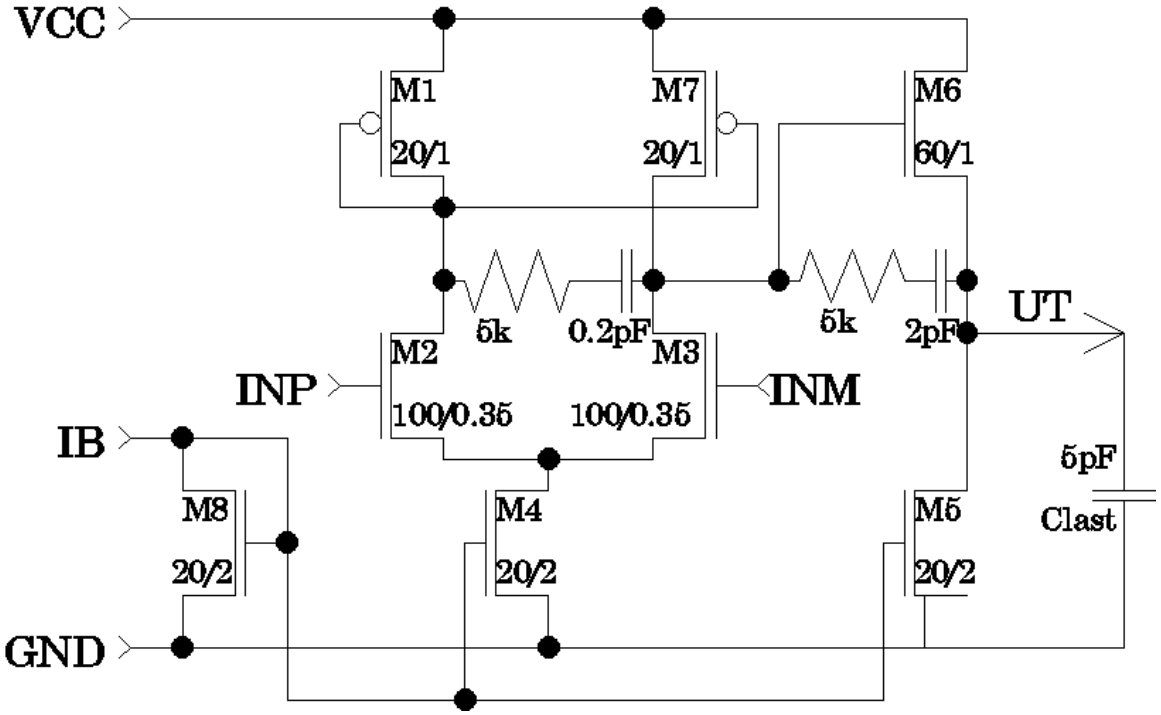


This stage is useful to be able to drive a large load. As the stage is drawn above it can be connected directly to the output of the common source stage described earlier. Use the transistor sizes 20µm/2µm in the current mirror and 35µm/0.35µm in the source follower.

a) Approximately how much current do we need to draw a 50pF load 20mV (peak-to-peak) with a flank which is equivalent to a 1MHz sine?
b) What is the gain, noise on the output and equivalent input noise of the source follower? (If you have not found a current in point a) use a current of 70µA).
c) Combine the common source stage developed earlier with the common drain stage. It has to be able to support a load of 50pF. The input signal is a (<1mV) small sinus with frequency 1MHz. The amplification should be a minimum of 20dB. Where occurs most of noise influencing on th eperformance? Report gain, output and equivalent input noise, power consumption and maximum input signal amplitude before the signal begins to be distorted.

3. CMOS amplifier with differential input

We shall in this subtask study a slightly modified version of the amplifier we had in the secondary mandatory task.



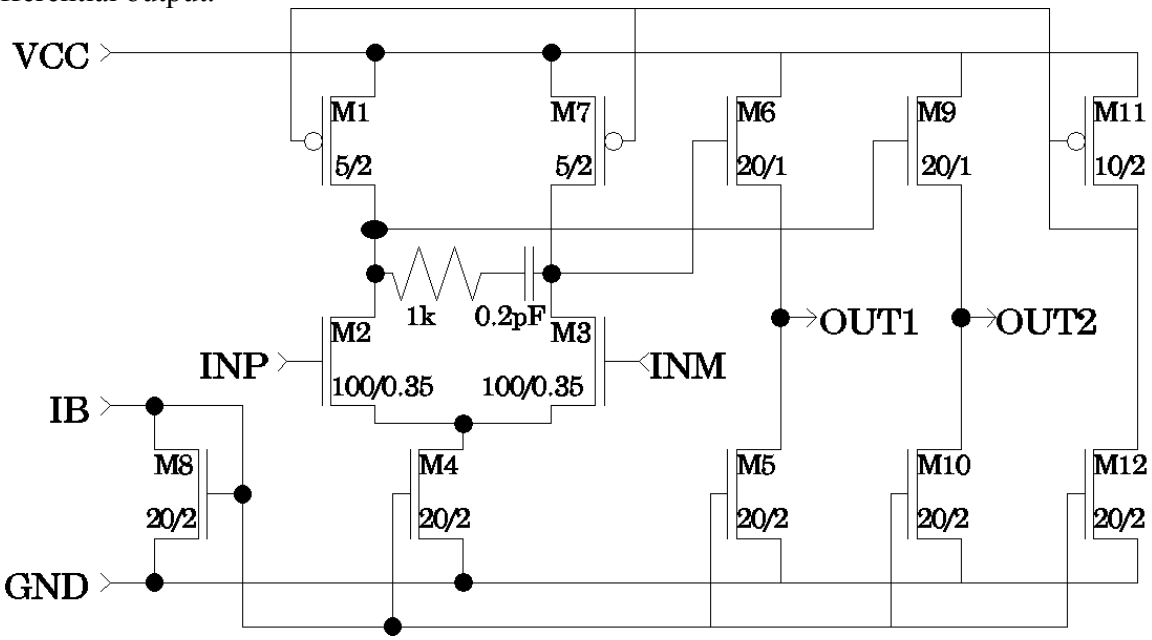
Set the VCC to 3.3V and the DC-offset (signal ground) of the INM and INP to 1.65V. Use INP as signal input. We look for the amplifier alone without feedback (open loop). The output has a capacitive load of 5pF.

In the following, you should vary some sizes and values and see how this will affect the gain, noise on the output and equivalent input noise. Give the values at 1MHz.

a) IB varies from 30µA to 110µA in 20µA steps.
b) Make the width of M1 and M7 half.
c) Double the length of the M1 and M7.
d) Make the width of M2 and M3 half.
e) Double both the length and width of M2 and M3.

4. CMOS amplifier with differential input and output

In the following we have developed the amplifier from the previous subtask into one with differential output.



Use the same forces and the same transistor models as in the previous task.

a) Find the gain, the differential gain, output noise and equivalent input noise with bias currents 30µA, 50µA and 70µA.

b) Use the current reference 50µA and double the width and length of the M2 and M3 so that the W/L-ratio is kept constant. Find the gain, output noise and equivalent input noise.

c) Set up a simulation to determine the impact of noise on the supply voltage VCC. Find the impact on each of the outputs and impact of the difference between the outputs. Do this both with identical M2 and M3 (as defined above) and with the width of M2 1% larger than the width of M3. Compare the results.

d) Try to indicate the variation in current draw on the VCC when the input signal is a 1MHz sine. Let the signal be the largest possible before the signal is distorted.