UNIVERSITY OF OSLO

Faculty of Mathematics and Natural Sciences

Exam in	**:** FYS 3240/4240
Day of exam:	**:** 12. June 2014
Exam hours:	**:** 09.00 – 12.00

This examination paper consists of 2 pages.

Permitted materials: : Calculator

Make sure that your copy of this examination paper is complete before answering.

Problem 1

a) Explain how the accuracy (constant frequency output) of quartz crystal oscillators is improved.
b) Explain the **IEEE 1588** and the **NTP** protocols.
c) Explain the limitations of software timing based on the computer clock when you try to measure the time between events in your software code.
d) How can you make more accurate relative time measurements in your software then what you can obtain using the computer clock?
e) You are provided two separate text files with measurements recorded from two different instruments. The first column in both files should contain a GPS timestamp for each data sample. However, comparing the measurement data in the two files you discover that it must be an offset in time between the timestamps in the two files. What could be the reason for this time offset?

Problem 2

a) Explain why UDP is used instead of TCP in applications such as video streaming.
b) What is a **jumbo frame**, and why is it used?
c) What is required in order to run data acquisition software on a modern computer running Windows with protected mode? Explain.
d) What are the advantages and disadvantages of selecting RAID-10 when doing data acquisition?
e) What is the "definition" of a real time system?
f) Many computer-based data acquisition systems are running on non-real-time hardware using operating systems such as Windows 7. Explain the main hardware and software solutions used to make this possible.

g) How can you to increase the signal-to-noise-ratio (SNR) in a data acquisition system?

h) The equivalent circuit for a sensor and the DAQ front-end electronics is shown in Figure 1. The sensor is modelled as an ideal voltage generator with output voltage V_{in} followed by a parallel connection of a resistor R_s and a capacitance C_s on the output. The DAQ front-end electronics is modelled as an ideal amplifier with gain 1, with a parallel connection of a resistor R_L and a capacitor C_L on the input. The signal cable between the sensor output and the front-end electronics input is assuemd ideal, with zero resistance and zero capacitance.

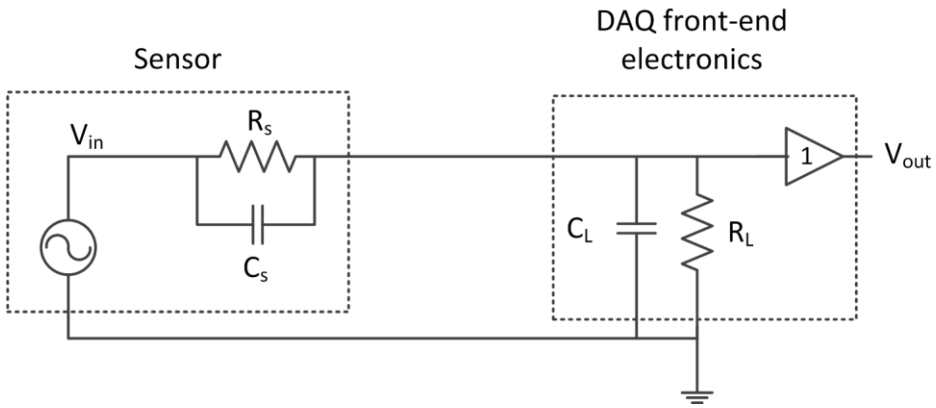

Figure 1: Equivalent circuit for a sensor and the DAQ front-end electronics. (The signal cable between the sensor output and the DAQ front-end electronics input is assuemd ideal, with zero resistance and zero capacitance).

Look at the following two cases:

1) very low frequency of the input signal from the sensor ($f \rightarrow 0$)

2) very high frequency of the input signal ($f \rightarrow \infty$)

Show that the conditons $R_L >> R_s$ and $C_L << C_s$ are required to get $V_{out} \approx V_{in}$.

Hints:
All calculations can be based on V = Z * I (Ohm's law with a complex impedance). Look at the circuit as a voltge divider between the sensor impedance and the load impedance.

The following relations are provided to assist in the calculations:

- Voltage divider: $V_{out} = \frac{Z_L}{Z_s + Z_L} \cdot V_{in}$
- Impedance of a resistor: $Z_R = R$
- Impedance of a capacitor : $Z_C = \frac{1}{j\omega C}$, where $\omega = 2\pi f$
- Impedance of a parallel connection of a resistor and a capacitor: $Z_p = Z_R \parallel Z_C = \frac{Z_C \cdot R}{Z_C + R}$