SECTION 4

HIGH SPEED SAMPLING ADCs

- ADC Dynamic Considerations
- Selecting the Drive Amplifier Based on ADC Dynamic Performance
- Driving Flash Converters
- Driving the AD9050 Single-Supply ADC
- Driving ADCs with Switched Capacitor Inputs
- Gain Setting and Level Shifting
- External Reference Voltage Generation
- ADC Input Protection and Clamping
- Applications for Clamping Amplifiers
- Noise Considerations in High Speed Sampling ADC Applications

SECTION 4

HIGH SPEED SAMPLING ADCS
Walt Kester

Modern high speed sampling ADCs are designed to give low distortion and wide dynamic range in signal processing systems. Realization of specified performance levels depends upon a number of factors external to the ADC itself, including proper design of any necessary support circuitry. The analog input drive circuitry is especially critical, because it can degrade the inherent ADC dynamic performance if not designed properly.

Because of various process and design-related constraints, it is generally not possible to make the input of a high speed sampling ADC totally well-behaved, i.e., high impedance, low capacitance, ground-referenced, free from glitches, impervious to overdrive, etc. Therefore, the ADC drive amplifier must provide excellent ac performance while driving what may be a somewhat hostile load (depending upon the particular ADC selected).

The trend toward single-supply high speed designs adds additional constraints. The input voltage range of high speed single-supply ADCs may not be ground referenced (for valid design reasons), therefore level shifting with single-supply op amps (which may have limited common-mode input and output ranges) is usually required, unless the application allows the signal to be ac coupled.

Although there is no *standard* high speed ADC input structure, this section addresses the most common ones and provides guidelines for properly designing the appropriate input drive circuitry.

Some sampling ADCs also require external reference voltages. In other cases, performance improvements can be realized by using an external reference in lieu of an internal one. It is equally important that these reference circuits be designed with utmost care, since they too affect the overall ADC performance.

HIGH SPEED, LOW VOLTAGE SAMPLING ADCs

- **Key Specifications for sampling ADCs:**
  - **Distortion**
  - **Noise**
  - **Distortion Plus Noise**
  - **Effective Number of Bits**
  - **Bandwidth (Full Power and Small Signal)**
  - **Sampling Rate**
- **Modern Trends**
  - **Low Power:** **CMOS, BiMOS, or XFCB Processes**
  - **Low Voltage:** **±5V, +5V, +5V (Analog) / +3V (Digital)**
  - **Input Voltage Ranges not always Ground-Referenced**
  - **Analog Input Can Generate Transient Currents**

Figure 4.1

ADC DYNAMIC CONSIDERATIONS

In order to make intelligent decisions regarding the input drive circuitry, it is necessary to understand first exactly how the dynamic performance of the ADC is characterized. Modern signal processing applications require ADCs with wide dynamic range, high bandwidth, low distortion, and low noise. As well as having traditional dc specifications (offset error, gain error, differential linearity error, and integral linearity error), *sampling* ADCs (ADCs with an internal sample-and-hold function) are generally specified in terms of Signal-to-Noise Ratio (SNR, or S/N), Signal-to-Noise-Plus Distortion Ratio [S/(N+D), or SINAD], Effective Number of Bits (ENOB), Harmonic Distortion, Total Harmonic Distortion (THD), Total Harmonic Distortion Plus Noise (THD+N), Intermodulation Distortion (IMD), and Spurious Free Dynamic Range (SFDR). Sampling ADC data sheets may provide some, but not all of these ac specifications. The ac specifications are usually tested by applying spectrally pure sinewaves to the ADC and analyzing its output in the frequency domain with a Fast Fourier Transform (FFT). The process is similar to using an analog spectrum analyzer to measure the ac performance of an amplifier. Because of the quantization process, however, an ADC produces some errors not found in amplifiers.

ADC DYNAMIC PERFORMANCE SPECIFICATIONS

- **Distortion Specifications: (Narrowband)**
  - **Harmonic Distortion**
  - **Total Harmonic Distortion (THD)**
  - **Spurious Free Dynamic Range (SFDR)**
  - **Intermodulation Distortion (IMD), Two-Tone Input**
- **Noise Specifications: dc to f_s / 2**
  - **Signal-to-Noise Ratio without Harmonics (often called SNR, or S/N)**
- **Noise Plus Distortion Specifications: dc to f_s / 2**
  - **Signal-to-Noise and Distortion (S/N+D, SINAD), but often referred to as SNR (check definition carefully when evaluating ADCs), often converted to Effective Bits (ENOB)**
  - **Total Harmonic Distortion Plus Noise (THD + N)**
- **Broadband Noise can be reduced by filtering or averaging**

Figure 4.2

An ideal N-bit ADC, sampling at a rate f_S, produces quantization noise having an rms value of q/(sqrt 12) measured in the Nyquist bandwidth dc to $f_S/2$, where q is the weight of the Least Significant Bit (LSB). The value of q is obtained by dividing the full scale input range of the ADC by the number of quantization levels, 2^N. For example, an ideal 10-bit ADC with a 2.048V peak-to-peak input range has 2^10 = 1024 quantization levels, an LSB of 2mV, and an rms quantization noise of 2mV/(sqrt 12) = 577μV rms. The derivation of the theoretical value of quantization noise, q/(sqrt 12), makes the assumption that the quantization noise is not correlated in any fashion to the input signal, and may therefore be treated as Gaussian noise. This is normally true, but in certain cases where the input sinewave frequency happens to be an exact submultiple of the sampling rate, the quantization noise may tend to be concentrated at the harmonics of the input signal, even though the rms value is still approximately q/(sqrt 12).

Another way to express quantization noise is to convert it into a Signal-to-Noise ratio by dividing the rms value of the input sinewave by the rms value of the quantization noise. Normally, this is measured with a full scale input sinewave, and the expression relating the two is given by the well-known equation,

$$SNR = 6.02N + 1.76 dB.$$

An actual ADC will produce noise in excess of the theoretical quantization noise, as well as distortion products caused by a non-linear transfer function. An FFT is used to calculate the rms value of all the distortion and noise products, and the actual

signal-to-noise-plus-distortion, S/(N+D), is computed. The above equation is solved for N, yielding the well-known expression for Effective Number of Bits, ENOB:

$$ENOB = \frac{S/(N+D)_{ACTUAL} - 1.76dB}{6.02}.$$

For example, if a 10-bit ADC has an actual measured S/(N+D) of 56dB (theoretical would be 61.96dB), then it will have 9 effective bits, i.e., the non-ideal 10-bit ADC yields the same performance as an ideal 9-bit one.

EFFECTIVE NUMBER OF BITS (ENOB)
INDICATES OVERALL DYNAMIC PERFORMANCE OF ADCs

- **S/(N+D) = 6.02N + 1.76dB (Theoretical)**
- **ADC ACHIEVES S/(N+D) = XdB (Actual)**
- **ENOB = (XdB - 1.76dB) / (6.02dB)**
- **ENOB Includes Effects of All Noise and Distortion in the bandwidth DC to $f_s/2$**

Figure 4.3

Even well-designed sampling ADCs have non-linearities which contribute to non-ideal low frequency performance, and additionally, performance degrades as the input frequency is increased. A useful way to evaluate the ac performance of ADCs is to plot Signal-to-Noise Plus Distortion, S/(N+D), (or convert it to ENOB) as a function of input frequency. This measurement is somewhat all-inclusive and includes the effects of both noise and distortion products.

In some instances, SNR may be specified both with and without the distortion products, and in other cases, distortion may be specified separately, either as individual harmonic components, or as total harmonic distortion (THD). Spurious Free Dynamic Range (SFDR) is simply another way of describing distortion products and is the ratio of the signal level to the worst frequency spur, under a given set of conditions. Intermodulation Distortion (IMD) is measured by applying two tones (F1 and F2) to the ADC and determining the ratio of the power in one of the tones to the various IMD as shown in Figure 4.4. Unless otherwise specified, the third-order products which occur at the frequencies 2F1 – F2 and 2F2 – F1 are the ones used in the measurement because they lie close to the original tones and are difficult to filter.

INTERMODULATION DISTORTION (IMD)

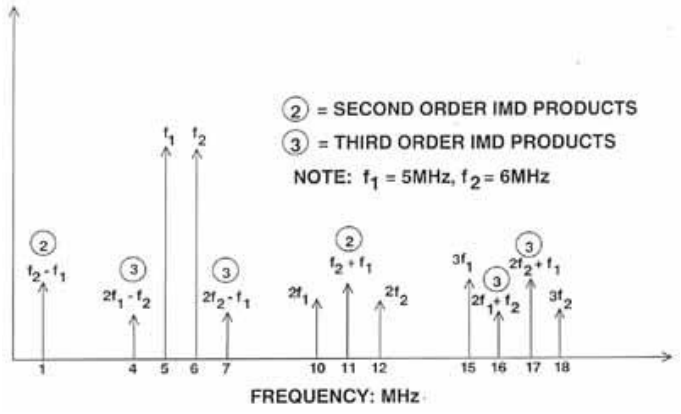


Figure 4.4

If we plot the gain of an amplifier with a small signal of a few millivolts or tens of millivolts, we find that as we increase the input frequency, there is a frequency at which the gain has dropped by 3 dB. This frequency is the upper limit of the *small signal bandwidth* of the amplifier and is set by the internal pole(s) in the amplifier response. If we drive the same amplifier with a large signal so that the output stage swings with its full rated peak-to-peak output voltage, we may find that the upper 3dB point is at a lower frequency, being limited by the slew rate of the amplifier output stage. This high-level 3dB point defines the *large signal bandwidth* of an amplifier. When defining the large signal bandwidth of an amplifier, a number of variables must be considered, including the power supply, the output amplitude (if slew rate is the only limiting factor, it is obvious that if the large signal amplitude is halved, the large signal bandwidth is doubled), and the load. Thus large signal bandwidth is a rather uncertain parameter in an amplifier, since it depends on so many uncontrolled variables - in cases where the large signal bandwidth is less than the small signal bandwidth, it is better to define the output slew rate and calculate the maximum output swing at any particular frequency.

In an ADC, however, the maximum signal swing is always full scale, and the load seen by the signal is defined. It is therefore quite reasonable to define the large signal bandwidth (or full-power bandwidth) of an ADC and report it on the data sheet. In some cases, the small signal bandwidth may also be given.

ADC LARGE SIGNAL (OR FULL POWER) BANDWIDTH

- **With Small Signal, the Bandwidth of a Circuit is limited by its Overall Frequency Response.**
- **At High Levels of Signal the Slew Rate of Some Stage May Control the Upper Frequency Limit.**
- **In Amplifiers There are so many Variables that *Large Signal Bandwidth* needs to be Redefined in every Individual Case, and *Slew Rate* is a more Useful Parameter for a Data Sheet.**
- **In ADCs the Maximum Signal Swing is the ADC's Full Scale Span, and is therefore Defined, so *Full Power Bandwidth* (FPBW) may Appear on the Data Sheet.**
- **HOWEVER the FPBW Specification Says Nothing About Distortion Levels. Effective Number of Bits (ENOB) is Much More Useful in Practical Applications.**

Figure 4.5

However, the large signal bandwidth tells us the frequency at which the amplitude response of the ADC drops by 3dB - it tells us nothing at all about the relationship between distortion and frequency. If we study the behavior of an ADC as its input frequency is increased, we discover that, in general, noise and distortion increase with increasing frequency. This reduces the resolution that we can obtain from the ADC.

If we draw a graph of the ratio of signal-to-noise plus distortion (S/N+D) against its input frequency, we find a much more discouraging graph than that of its frequency response. The ratio of S/N+D can be expressed in dB or as effective number of bits (ENOB) as discussed above. As we have seen, the SNR of a perfect N-bit ADC (with a full scale sinewave input) is (6.02N + 1.76)dB. A graph of ENOB against the variations of input amplitude can be depressing when we see just how little of the dc resolution of the ADC can actually be used, but can sometimes show interesting features: the ADC in Figure 4.6, for instance, has a larger ENOB for signals at 10% of FS at 1MHz than for FS signals of the same frequency. A simple frequency response curve cannot have plots crossing in this way.

ADC GAIN AND ENOB VERSUS FREQUENCY
SHOWS INPORTANCE OF ENOB SPECIFICATION

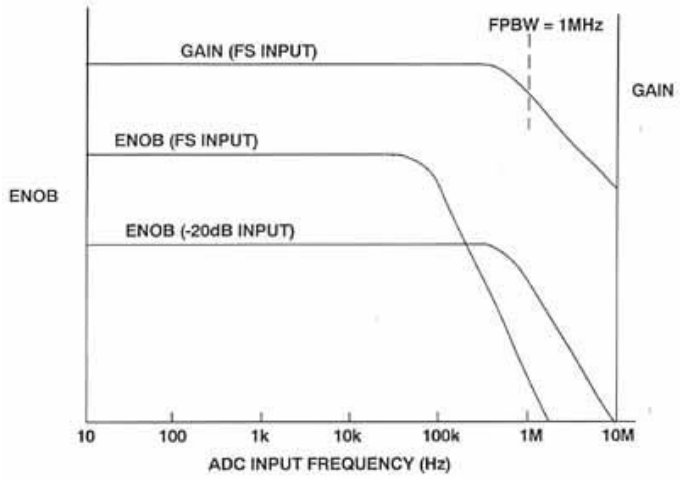


Figure 4.6

The causes of the loss of ENOB at higher input frequencies are varied. The linearity of the ADC transfer function degrades as the input frequency increases, thereby causing higher levels of distortion. Another reason that the SNR of an ADC decreases with input frequency may be deduced from Figure 4.7, which shows the effects of phase jitter on the sampling clock of an ADC. The phase jitter causes a voltage error which is a function of slew rate and results in an overall degradation in SNR as shown in Figure 4.8. This is quite serious, especially at higher input/output frequencies. Therefore, extreme care must be taken to minimize phase noise in the sampling/reconstruction clock of any sampled data system. This care must extend to all aspects of the clock signal: the oscillator itself (for example, a 555 timer is absolutely inadequate, but even a quartz crystal oscillator can give problems if it uses an active device which shares a chip with noisy logic); the transmission path (these clocks are very vulnerable to interference of all sorts), and phase noise introduced in the ADC or DAC. A very common source of phase noise in converter circuitry is aperture jitter in the integral sample-and-hold (SHA) circuitry.

EFFECTS OF APERATURE AND SAMPLING CLOCK JITTER

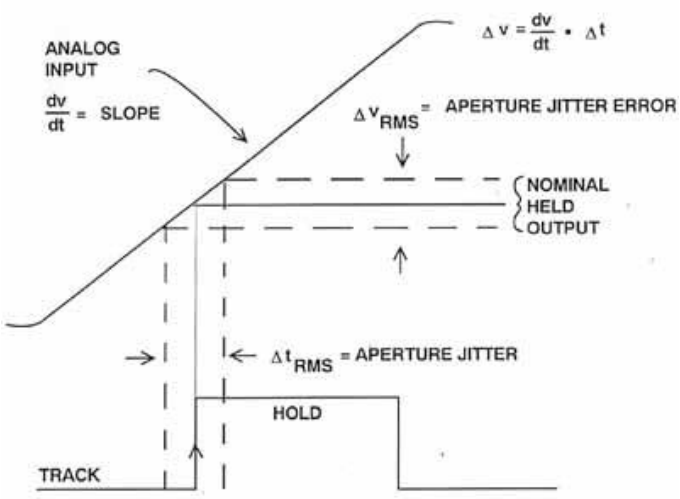


Figure 4.7

SNR DUE TO SAMPLING CLOCK JITTER (t_j)

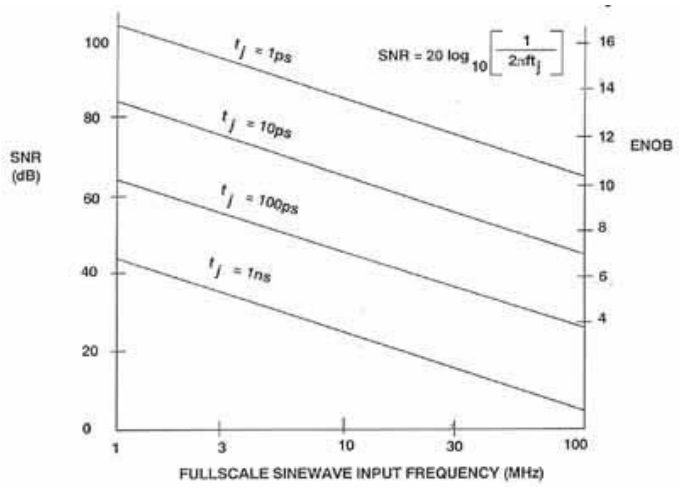


Figure 4.8

A decade or so ago, sampling ADCs were built up from a separate SHA and ADC. Interface design was difficult, and a key parameter was aperture jitter in the SHA. Today, most sampled data systems use *sampling* ADCs which contain an integral SHA. The aperture jitter of the SHA may not be specified as such, but this is not a cause of concern if the SNR or ENOB is clearly specified, since a guarantee of a specific SNR is an implicit guarantee of an adequate aperture jitter specification. However, the use of an additional high-performance SHA will sometimes improve

the high-frequency ENOB of a sampling ADC, and may be more cost-effective than replacing the ADC with a more expensive one.

It should be noted that there is also a fixed component which makes up the ADC aperture time. This component, usually called *effective aperture delay time*, does not produce an error. It simply results in a time offset between the time the ADC is asked to sample and when the actual sample takes place (see Figure 4.9). The variation or tolerance placed on this parameter from part to part is important in simultaneous sampling applications or other applications such as I and Q demodulation where several ADCs are required to track each other.

EFFECTIVE APERATURE DELAY TIME

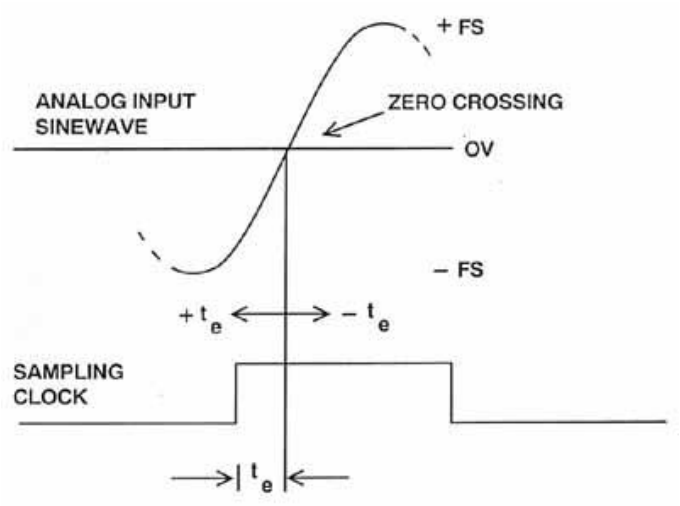


Figure 4.9

The distortion produced by an ADC or DAC cannot be analyzed in terms of second and third-order intercepts, as in the case of an amplifier. This is because there are two components of distortion in a high performance data converter. One component is due to the non-linearity associated with the analog circuits within the converter. This non-linearity has the familiar "bow" or "s"-shaped curve shown in Figure 4.10. (It may be polynomial or logarithmic in form). The distortion associated with this type of non-linearity is sometimes referred to as *soft* distortion and produces low-order distortion products. This component of distortion behaves in the traditional manner, and is a function of signal level. In a practical data converter, however, the soft distortion is usually much less than the other component of distortion, which is due to the differential nonlinearity of the transfer function. The converter transfer function is more likely to have discrete points of discontinuity across the signal range as shown in Figure 4.10.

TRANSFER CHARACTERISTICS FOR "SOFT" AND "HARD" DISTORTION IN ADCs

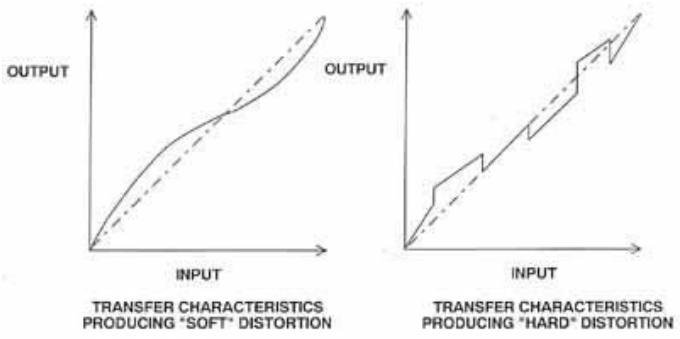


Figure 4.10

The actual location of the points of discontinuity depends on the particular data converter architecture, but nevertheless, such discontinuities occur in practically all converters. Non-linearity of this type produces high-order distortion products which are relatively unpredictable with respect to input signal level, and therefore such specifications as *third order intercept point* may be less relevant to converters than to amplifiers and mixers. For lower-amplitude signals, this constant level *hard* distortion causes the SFDR of the converter to *decrease* as input amplitude decreases. The soft distortion in a well-designed converter is only significant for high frequency large-amplitude signals where it may rise above the hard distortion floor.

In a practical system design, the ADC is usually selected based primarily on the required dynamic performance at the required sampling rate and input signal frequency, using one or more of the above specifications. DC performance may be important also, but is generally of less concern in signal processing applications. Once the ADC is selected, the appropriate interface circuitry must be designed to preserve these levels of ac and dc performance.

SELECTING THE DRIVE AMPLIFIER BASED ON ADC DYNAMIC PERFORMANCE

The ADC drive amplifier performs several important functions in a system. First, it isolates the signal source and provides a low-impedance drive to the ADC input. A low-impedance dc and ac drive source is important because the input impedance of the ADC may be signal-dependent, and the input may also generate transient load currents during the actual conversion process. A low source impedance at high frequencies minimizes the errors produced by these effects. Second, the drive amplifier provides the necessary gain and level shifting to match the signal to the ADC input voltage range.

FUNCTIONS OF THE ADC DRIVE AMPLIFIER

- **Buffer the analog signal from the ADC input:**
  - **ADC input may not be a constant high impedance**
  - **ADC input may generate transient loads**
- **Provide other functions:**
  - **Gain**
  - **Level Shifting**
- **If the ADC input is constant high impedance with no transient loading, do not use a buffer amplifier unless required for gain or level shifting!!**

Figure 4.11

The S/(N+D) plot of the ADC should generally be used as the first selection criterion for the drive amplifier. If the Total Harmonic Distortion Plus Noise (THD+N) of the drive amplifier is always 6 to 10dB better than the S/(N+D) of the ADC over the frequency range of interest, then the overall degradation in S/(N+D) caused by the amplifier will be limited to between approximately 0.5dB and 1db, respectively. This will be illustrated using two state of the art components: the AD9022 12 bit, 20MSPS ADC and the AD9631 op amp. A block diagram of the AD9022 is shown in Figure 4.12, and key specifications in Figure 4.13. AD9631/AD9632 key specifications are given in Figure 4.14.

The AD9022 employs a three-pass subranging architecture and digital error correction. The analog input is applied to a 300Ω attenuator and passed to the sampling bridge of the first internal track-and-hold amplifier (T/H). The held value of the first T/H is applied to a 5-bit flash converter and a second T/H. The 5-bit flash converter resolves the most significant bits (MSBs) of the held analog voltage. These 5 bits are reconstructed via a 5-bit DAC and subtracted from the original T/H output signal to form a residue signal. A second T/H holds the amplified residue signal while it is encoded with a second 5-bit flash ADC. Again, the 5-bits are reconstructed and subtracted from the second T/H output to form a residue signal. This residue is amplified and encoded with a 4-bit flash ADC to provide the 3 least significant bits (LSBs) of the digital output and one bit of error correction. The digital error correction logic combines the data from the three flash converters and presents the result as a 12-bit parallel digital word. The output stage is TTL (AD9022), or ECL (AD9023). Output data can be strobed on the rising edge of the ENCODE command.

AD9022 12-BIT, 20MSPS SAMPLING ADC

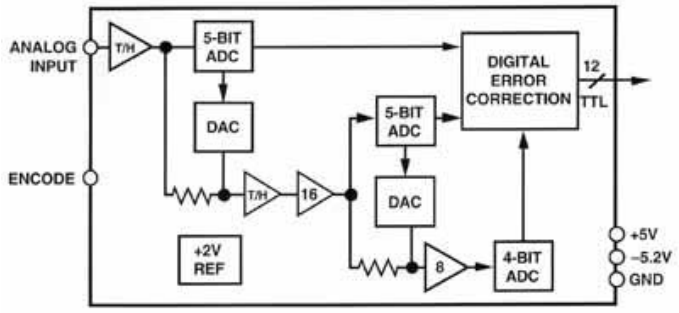


Figure 4.12

AD9022 ADC KEY SPECIFICATIONS

- **12-bit, 20MSPS Sampling ADC**
- **TTL Outputs (AD9023 has ECL outputs)**
- **On-Chip reference and SHA**
- **High Spurious Free Dynamic Range (SFDR):**
  - **76dB @ 1MHz Input f_s = 20MSPS**
  - **74dB @ 9.6MHz Input f_s = 20MSPS**
- **Analog Input Bandwidth: 110MHz**
- **Well-Behaved analog input with no transients**
- **Input Range: ±1.024V, Input Impedance: 300Ω, 5pF**
- **Dual Supplies (+5, -5.2V), 1.4W Power Dissipation**

Figure 4.13

AD9632 OP AMP KEY SPECIFICATIONS

- **Current-Feedback performance with voltage-feedback amps**
- **Small Signal Bandwidth:** **320MHz (AD9631, G = +1)**
  250MHz (AD9632, G = +2)
- **Low Distortion:** **-113dBc @ 1MHz**
  - 95dBc @ 5Mhz
  - 72dBc @ 20MHz
- **Slew Rate:** **1300V / μs**
- **Settling Time:** **16ns to 0.01%, 2V step**
- **Low Noise: Voltage: 7nV/√Hz, Current: 2pA/√Hz**
- **±3V to ±5V Supply Operation, 17mA Supply Current**

Figure 4.14

Figure 4.15 shows the THD+N of the AD9631 drive amplifier superimposed on the S/(N+D) plot for the AD9022 ADC (12-bits, 20MSPS). Notice that the amplifier THD+ N is at least 10dB better than the ADC S/(N+D) for input frequencies up to about 10MHz (the Nyquist frequency). In performing this comparison, it is important that the data for the op amp be obtained under the final operating conditions encountered in the actual circuit, i.e., gain, signal level, power supply voltage, etc.

AD9022 ADC S/(N+D) AND AD9631 OP AMP THD+N PLOTTED AS A FUNCTION OF INPUT FREQUENCY

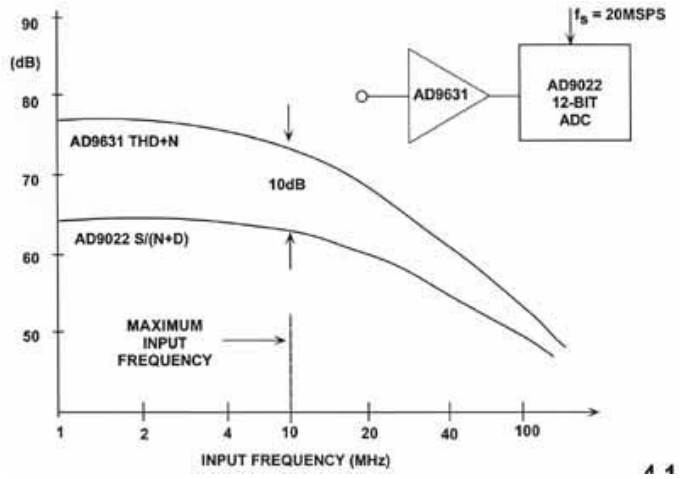


Figure 4.15

While S/(N+D) and THD+N are useful ac performance indicators, there are a number of applications where low distortion is more important than low noise. In spectral analysis using FFTs, or other applications where averaging techniques can be used to reduce the effects of noise, the amplifier THD and the ADC distortion (generally SFDR) should be used as the selection criteria. These characteristics should be plotted on the same scale, and the drive amplifier THD should be at least 6 to 10dB better than the ADC SFDR over the frequency range of interest. Such a plot for the AD9631 op amp and the AD9022 ADC is shown in Figure 4.16.

AD9022 ADC SFDR AND AD9631 OP AMP THD PLOTTED AS A FUNCTION OF INPUT FREQUENCY

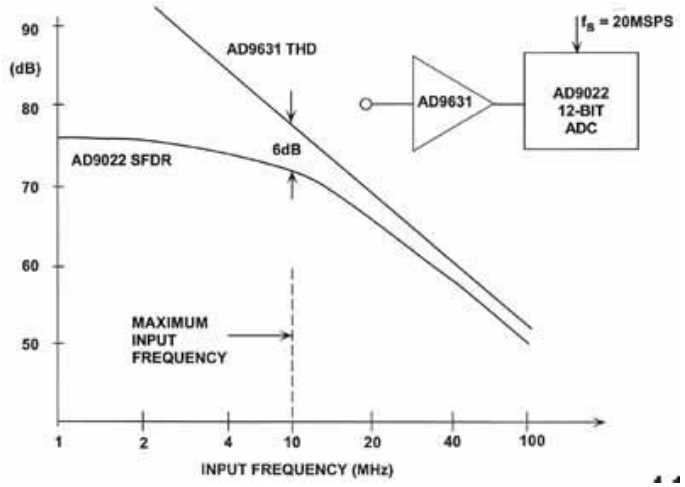


Figure 4.16

The above ac selection criterion works well if the ADC input is relatively benign, but may give overly optimistic results if the input impedance is signal dependent, or the input produces transient currents. The existence of either of these two conditions requires further investigation. The implications of signal-dependent input impedance will be demonstrated using a flash converter. Dealing with ADC input transient currents will be illustrated by examining a fast single-supply sampling ADC with a CMOS switched capacitor input stage.

DRIVING FLASH CONVERTERS

A typical flash converter (Figure 4.17) generally exhibits a signal-dependent input impedance (often referred to as *non-linear* input impedance), where the effective input capacitance is a function of signal level. The signal-dependent capacitance can be modeled as the junction capacitance of a diode, C_j. At the negative end of the input range, all the parallel comparators in the flash converter are "off", and the capacitance is low (modeled by a reverse-biased diode). At the positive end of the input range, all comparators are "on", thereby increasing the effective input capacitance (modeled by a zero-biased diode). For the example in the diagram, the Spice model (Figure 4.18) for the flash converter input under consideration is a

7.5nH inductor (simulating package pin and wirebond inductance), a 10pF fixed capacitor, and a diode having a 6pF zero-bias junction capacitance (C_{JO}). The total input capacitance changes from 16pF (0V input) to 12.5pF (–2V input) as shown in Figure 4.18. The 50ohm series resistor, R_S, is required to isolate the wideband op amp output from the flash converter input capacitance. Selecting the correct value for the series resistance is critical. If it is too low, the wideband, low-distortion op amp may be unstable because of the flash converter capacitive load. If it is too large, the distortion due to the non-linear input impedance may become significant, and bandwidth will be reduced because of the lowpass filter formed by the series resistor and the input capacitance. Data sheets for wideband low distortion amplifiers generally have curves showing the optimum value of series resistance as a function of the load capacitance. Typical recommended resistor values range from about 10ohms to 100ohms, depending on the amplifier and the load capacitance. In the model, a value of 50ohm was chosen. Figure 4.19 shows the simulated THD produced by the equivalent circuit (assuming an ideal op amp, of course).

TYPICAL FLASH ADC BLOCK DIAGRAM

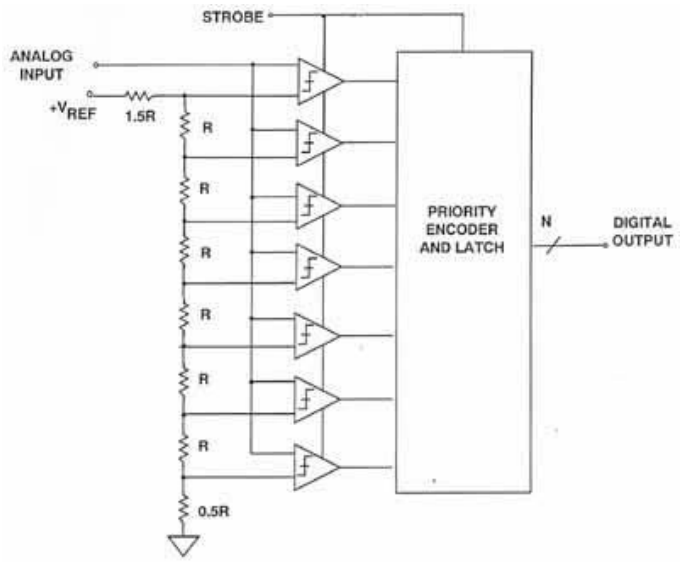


Figure 4.17

FLASH ADC INPUT MODEL SHOWS CAPACITANCE IS A FUNCTION OF INPUT SIGNAL

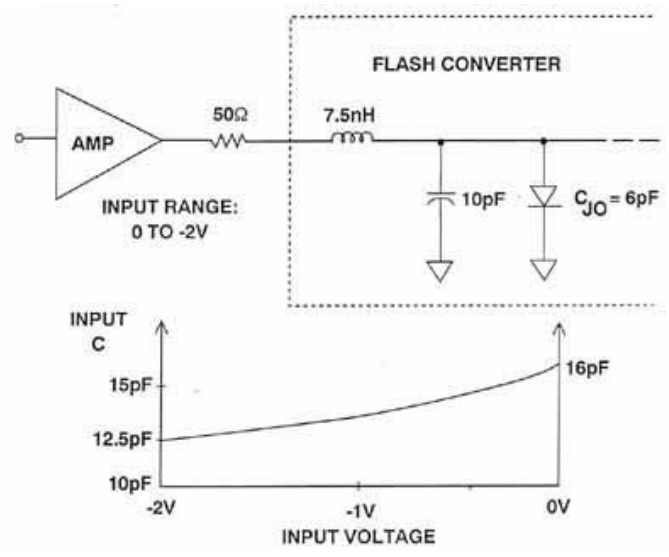


Figure 4.18

ADC TOTAL HARMONIC DISTORTION VERSUS INPUT FREQUENCY AS PREDICTED BY MODEL

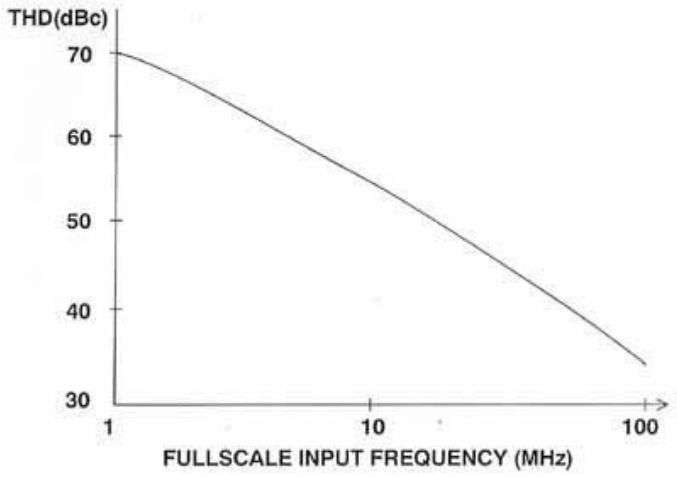


Figure 4.19

DRIVING THE AD9050 SINGLE-SUPPLY 10-BIT, 40MSPS ADC

The AD9050 is a 10-bit, 40MSPS single supply ADC designed for wide dynamic range applications such as ultrasound, instrumentation, digital communications, and professional video. A block diagram of the AD9050 (Figure 4.20) illustrates the two-step subranging architecture, and key specifications are summarized in Figure 4.21.

AD9050 10-BIT, 40MSPS SINGLE SUPPLY ADC

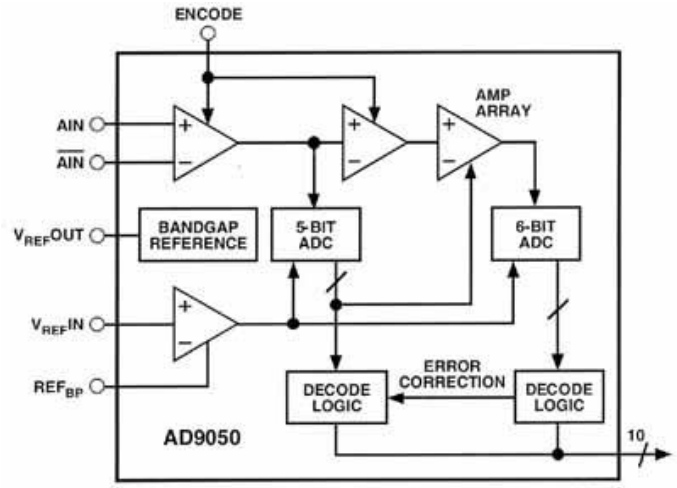


Figure 4.20

AD9050 10-BIT, 40MSPS ADC KEY SPECIFICATIONS

- **10-Bits, 40MSPS, Single +5V Supply**
- **Selectable Digital Supply: +5V, or +3V**
- **Low Power: 300mW on BiCMOS Process**
- **On-Chip SHA and +2.5V reference**
- **56dB S/(N+D), 9 Effective Bits, with 10.3MHz Input Signal**
- **No input transients, Input Impedance 5kΩ, 5pF**
- **Input Range +3.3V ±0.5V Single-Ended or Differential**
- **28-pin SOIC / SSOP Packages**
- **Ideal for Digital Beamforming Ultrasound Systems**

Figure 4.21

The analog input circuit of the AD9050 (see Figure 4.22) is differential, but can be driven either single-endedly or differentially with equal performance. The input signal range of the AD9050 is ±0.5V centered around a common-mode voltage of +3.3V.

AD9050 SIMPLIFIED INPUT CIRCUIT

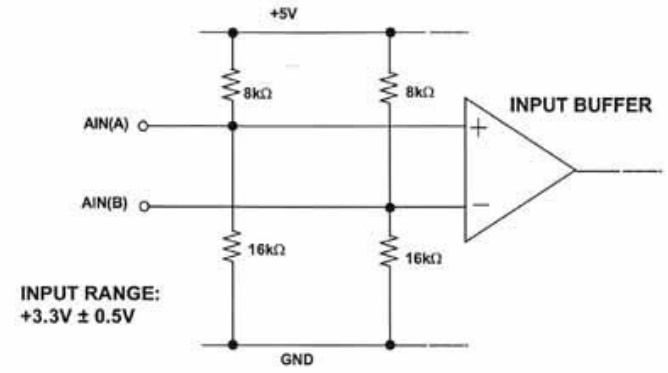


Figure 4.22

The input circuit of the AD9050 is a relatively benign and constant 5kΩ in parallel with approximately 5pF. Because of its well-behaved input, the AD9050 can be driven directly from 50, 75, or 100ohm sources without the need for a low-distortion buffer amplifier. In ultrasound applications, it is normal to ac couple the signal (generally between 1MHz and 15MHz) into the AD9050 differential inputs using a wideband transformer as shown in Figure 4.23 (A). Signal-to-noise plus distortion (S/N+D) values of 57dB (9.2 ENOB) are typical for a 10MHz input signal. If the

input signal comes directly from a 50, 75, or 100ohm single-ended source, capacitive coupling as shown in Figure 4.23 (B) can be used.

AC COUPLING INTO THE INPUT OF THE AD9050 ADC

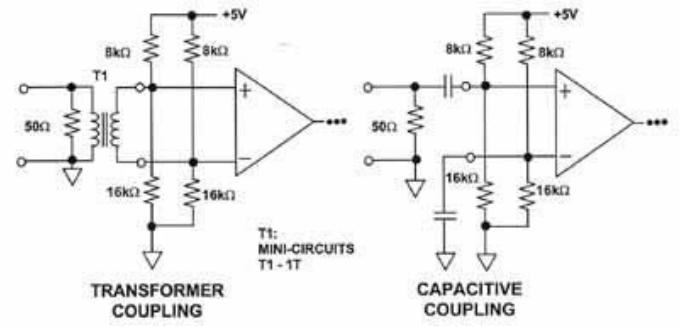


Figure 4.23

DRIVING ADCS WITH SWITCHED CAPACITOR INPUTS

Many ADCs, including fast sampling ones, have switched capacitor input circuits. Not only can the effective input impedance be a function of the sampling rate, but the switches (usually CMOS) may inject charge on the ADC's analog input. For instance, the internal track-and-hold amplifier (THA) may generate a current spike on the analog input when it switches from the *track* mode to the *hold* mode, and vice versa. Other spikes may be generated during the actual conversion. These fast current spikes appear on the output of the external ADC drive amplifier, producing corresponding voltage spikes (because of the closed-loop high frequency op amp output impedance), and conversion errors will result if the amplifier settling time to them is not adequate.

The AD876 is a 10-bit, 20MSPS, low power (150mW), CMOS ADC with a switched capacitor track-and-hold input circuit. The overall block diagram of the ADC is shown in Figure 4.24, and key specifications are given in Figure 4.25.

AD876 10-BIT, 20MSPS LOW POWER SINGLE SUPPLY ADC SIMPLIFIED BLOCK DIAGRAM

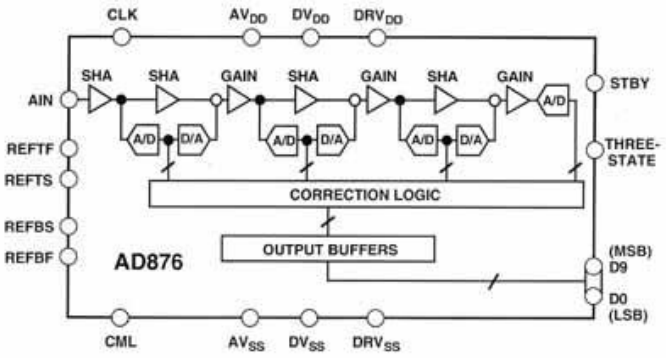


Figure 4.24

AD876 LOW POWER SINGLE SUPPLY ADC KEY SPECIFICATIONS

- **10-Bits, 20MSPS, Single-Supply**
- **Low Power CMOS Design: 140mW**
- **Standby Mode Power: <50mW**
- **S/(N+D): 56dB @ 1MHz**
  55dB @ 3.58MHz
  51dB @ 10MHz
- **Input Bandwidth: 250MHz**
- **Input Range: 2V peak-to-peak**
- **Differential Gain: 1%, Differential Phase: 0.5°**

Figure 4.25

Operation of the AD876 switched capacitor input circuit is illustrated in Figure 4.26, and the associated switching waveforms in Figure 4.27. The CMOS switches S1, S2, and S3 control the action of the internal sample and hold. They are shown in the track mode. Notice that in the track mode, the CMOS switch, S2, connects the input, V_{IN}, to the 3pF hold capacitor which must be charged by the drive amplifier.

When the circuit goes into the hold mode the following sequential switching occurs: S1 opens, S2 opens, and S3 closes (the entire sequence occurs in a few nanoseconds). The held voltage across C_H is thus transferred to the output of the internal op amp, A1. Opening CMOS switch S2 injects a small amount of charge into the ADC input (equivalent to approximately 1mA of current, having a duration of a few nanoseconds). This current produces a transient voltage across the op amp closed loop output impedance (approximately 10ohms at 10MHz, and 100ohms at 100MHz)

in series with the 30ohm isolation resistor, R_S. The resulting voltage spike is approximately 100mV, corresponding to the product of the 1mA transient and the total ac source impedance of 100ohms (the op amp Z_O of about 70ohms plus the 30ohm isolation resistor). During the hold mode, the AD876 performs the conversion, while the input signal may continue to change. The ADC input signal in Figure 4.27 goes from negative full scale (+1.7V) to positive full scale (+3.7V) during the first hold interval shown in the timing diagram. This represents a worst case condition, and input slew rates (and the corresponding charging transient) are quite likely to be less in a practical application.

At the end of the conversion, the switches return to their track mode state in the following sequence: S3 opens, S1 closes, and S2 closes (the entire sequence occurs in a few nanoseconds). When S2 closes, a small amount of charge is injected into the op amp output, but the dominant current spike (5mA) is the instantaneous current required to charge the hold capacitor, C_H, to the new signal value. The external drive amplifier must therefore charge C_H to the new signal value and settle to the required accuracy (1/2 LSB, or 1mV) before the initiation of the next conversion (the settling time must be less than 25ns if the ADC is sampling at its maximum rate of 20MSPS as shown). The charging current dominates and is shown on the ADC input waveform as a negative-going 500mV spike. The addition of an external capacitor, C_P = 15pF, in parallel with the ADC input helps absorb some of the transient charge and is small enough so that bandwidth is not compromised. The optimum value of 15pF was determined empirically.

AD876 ADC SWITCHED CAPACITOR INPUT CIRCUIT

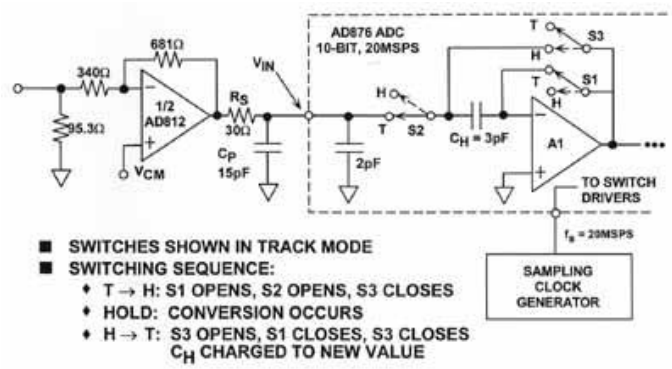


Figure 4.26

AD876 ANALOG INPUT TRANSIENTS
SHOWN FOR SAMPLING FREQUENCY OF 20MSPS

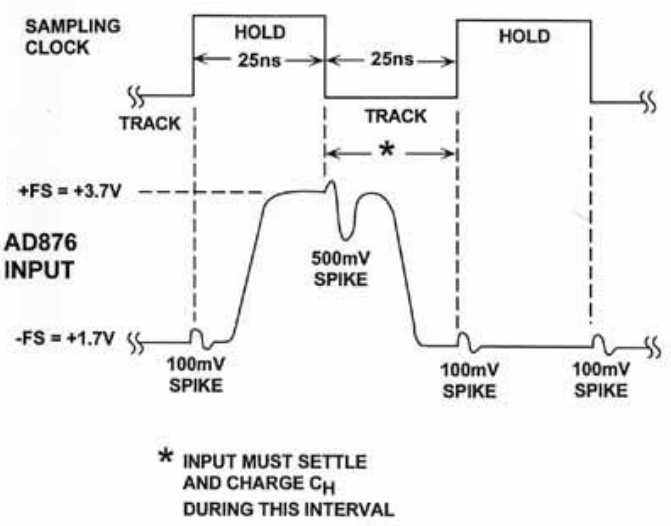


Figure 4.27

An empirical way to determine if the op amp transient load current settling time is adequate is to connect it to the ADC and observe the ADC input directly with a fast digital oscilloscope which is not sensitive to overdrive. If this is not possible, a good rule of thumb is to estimate the closed loop bandwidth, f_{cl}, required of the op amp to meet the required settling time. This is done as follows. The amplitude of the voltage spike, $V_{error}(t)$, at the ADC input is estimated by multiplying the input step current, Delta I, by the total driving impedance, Z_{out}, (composed of the closed loop output impedance plus the series isolation resistor, R_S). The output impedance of a typical high speed op amp (bandwidth of 50MHz or greater) is generally between 50ohms and 100ohms at the frequencies contained in the transient. If we assume a single-pole system with a bandwidth of f_{cl}, the transient exhibits an exponential decay described by the following equation:

$$V_{error}(t) = \Delta I \cdot Z_{out}\ e^{-t/\tau}.$$

Solving the equation for t:

$$t = -\tau \ln\left(\frac{V_{error}(t)}{\Delta I \cdot Z_{out}}\right).$$

Substituting $\tau = \frac{1}{2\pi f_{cl}}$,and solving for f_{cl}:

$$f_{cl} = -\frac{1}{2\pi t}\ln\left(\frac{V_{error}(t)}{\Delta I \cdot Z_{out}}\right)$$

Now, let $t = T_S/2 = 1/2f_S$ (where T_S = Sampling Period = $1/f_S$), and $V_{error}(t) = q/2$, q = weight of LSB:

$$f_{cl} = -\frac{f_S}{\pi} \ln\left(\frac{q/2}{\Delta I \cdot Z_{out}}\right),$$

the minimum required op amp closed loop bandwidth.

This equation determines the minimum closed-loop op amp bandwidth required based on the sampling rate, LSB weight, and the input voltage step (Delta I) Z_{out}.

In the example previously shown for the AD876 ADC, we can use the above equation to estimate the required op amp closed loop bandwidth by letting f_S = 20MSPS, q = 2mV, and (Delta I) Z_{out} = 500mV. Solving yields f_{cl} = 39.6MHz. The AD812 closed-loop bandwidth is approximately 60MHz in the configuration shown in Figure 4.28, which is more than sufficient to provide adequate settling time to the transient. Key specifications for the AD812 single-supply op amp are given in Figure 4.29.

SIMPLIFIED MODEL PREDICTS INPUT TRANSIENT SETTLING TIME OF ADC DRIVE AMP

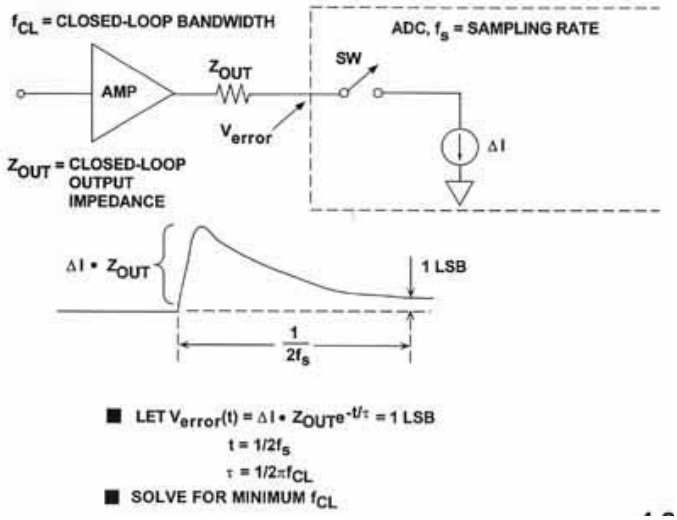


Figure 4.28

KEY SPECIFICATIONS OF AD812 DUAL OP AMP

- **Dual, Current Feedback, Low Current (11mA)**
- **Specified for ±15, ±5, +5, and +3V**
- **Input and Output CM Voltage Range (+1V to +4V), V_s = +5V**
- **Optimized for Video Applications:**
  - **Gain Flatness: 0.1dB to 40MHz**
  - **Differential Gain: 0.2%, Differential Phase: 0.02°**
- **145MHz Bandwidth (3dB)**
- **1600V / μs Slew Rate**
- **50mA Output Current**

Figure 4.29

It is generally true that if you select the op amp first based on the required distortion performance at the maximum input frequency of interest, then its bandwidth will be much greater than the ADC sampling rate, and the op amp will have adequate transient load current settling time.

The drive amplifier selection process can be summarized as follows. First, choose an op amp which provides the necessary bandwidth, distortion, and output voltage compatible with the ADC. A good ADC data sheet will recommend one or two op amps, generally selected to optimize ac performance at the higher frequencies. However, other choices may be better because of system considerations. For example, many tradeoffs are possible between ac and dc performance. If extremely low distortion at low frequencies is required (at the expense of high frequency performance), other low distortion amplifiers may provide optimum system performance. Other factors such a single-supply versus dual-supply may influence the decision.

The next step is to examine the ADC data sheet carefully to determine if the input structure presents any transient loads to the op amp. If transient loads are present, the op amp settling time is important, and the ADC data sheet should be consulted for specific requirements. If the data sheet does not specify the op amp settling time, a conservative approach is to choose an op amp with a settling time (to the required accuracy) of less than one-half the minimum sampling period. The required closed-loop bandwidth, f_{cl}, corresponding to the settling time can be estimated using the procedure and equations previously described. Finally, it is most important to construct a prototype of the system and perform an actual evaluation of the combined op amp and ADC performance. Manufacturer's evaluation boards are useful for this purpose.

DRIVE OP AMP SELECTION CRITERIA BASED ON ADC DYNAMIC PERFORMANCE: SUMMARY

- **Select Op Amp with distortion and noise better than ADC**
- **Consider other factors also:**
  - **Output Voltage Swing must match ADC input**
  - **Single or Dual-Supply System?**
  - **DC Accuracy / Drift if DC coupled**
- **Examine ADC for transient load currents, if any**
  - **Op amp must have sufficient closed-loop bandwidth to settle to transient currents**
  - **Use exponential decay model to estimate required f_{cl}**

Figure 4.30

GAIN SETTING AND LEVEL SHIFTING

In dc coupled applications, the drive amplifier must provide the required gain and offset to match the signal to the input voltage range of the ADC. Figure 4.31 summarizes various gain and level shifting options. The circuit of Figure 4.31A operates in the non-inverting mode and uses a reference voltage, V_{ref}, to offset the output. Gain and offset interact according to the equation:

$$V_{out} = \left(1 + \frac{R2}{R1}\right) V_{in} - \frac{R2}{R1} V_{ref}$$

The circuit in Figure 4.31B operates in the inverting mode, and the signal gain is independent of the offset. The disadvantage of this circuit is that the addition of R3 increases the noise gain, and hence the sensitivity to the op amp input offset voltage and noise. The input/output equation is given by:

$$V_{out} = -\frac{R2}{R1} V_{in} - \frac{R2}{R3} V_{ref}$$

The circuit in Figure 4.31C operates in the inverting mode, and the offset is applied to the non-inverting input, with no noise gain penalty. This circuit is also attractive for single-supply applications where $V_{ref} > 0$. The input/output equation is given by:

$$V_{out} = -\frac{R2}{R1} V_{in} + \left(\frac{R4}{R3 + R4}\right)\left(1 + \frac{R2}{R1}\right) V_{ref}$$

OP AMP LEVEL SHIFTING CIRCUITS

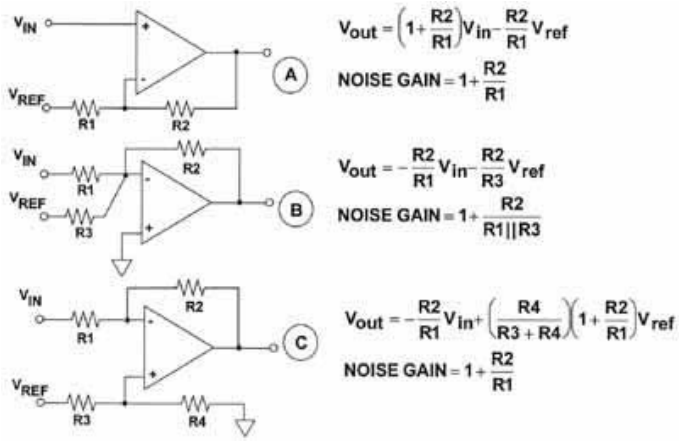


Figure 4.31

A practical example of a single-supply video signal-processing digitizing circuit is shown in Figure 4.32. The AD876 (10-bit, 20MSPS) ADC operates on a single +5V supply, and its nominal input voltage range is 2V peak-to-peak centered around an allowable common-mode voltage between +2.7V and +3.1V. The input voltage range of the AD876 is set by external references. The AD812 drive amplifier is a fast video op amp with a common-mode input voltage range of +1V to +4V, and a +1V to +4V output voltage range. With this amplifier/ADC combination, optimum performance is obtained by setting the AD876 input common-mode voltage at +2.7V (corresponding to an upper and lower input range of +3.7 and +1.7V, respectively).

SINGLE-SUPPLY DC-COUPLED DRIVE CIRCUIT FOR AD876 10-BIT, 20MSPS ADC USING AD812 OP AMP

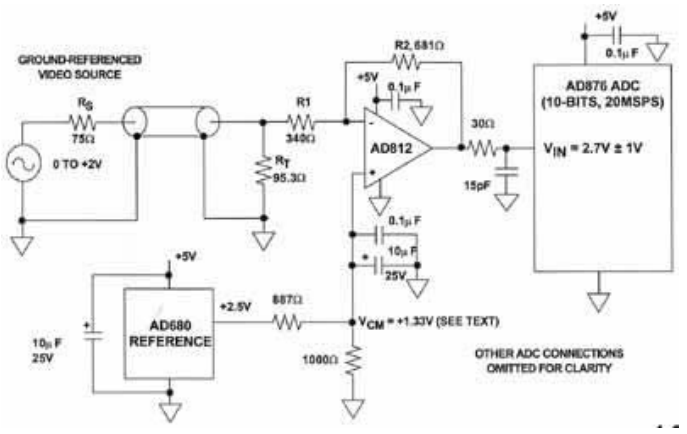


Figure 4.32

The Thevenin equivalent circuit of the video signal is a ground-referenced, 0 to +2V source with a 75ohm source impedance designed to drive a 75ohm terminated coaxial cable, producing a standard 0 to +1V video signal level at the load termination, R_T. (The video source can also be modeled as a Norton equivalent circuit with a 0 to +26.7mA current source in parallel with the 75ohm source resistance.)

The AD812 op amp is operated as an inverting level shifter, similar to the circuit previously shown in Figure 4.31C. The feedback resistor, R2, is chosen to be 681ohms for optimum flatness over the video bandwidth per the AD812 data sheet. The feedforward resistor, R1, is selected to give a signal gain of –2. The termination resistor, R_T, is chosen so that the parallel combination of R_T and R1 is 75ohms. The common-mode voltage, V_{cm}, required on the non-inverting op amp input must now be determined. Assume that the video source is zero volts. The corresponding op amp output voltage should be +3.7V. The common-mode voltage is determined by the voltage divider formed by R2, R1, R_T, and the 75ohm source resistance:

$$V_{cm} = 3.7\left(\frac{R_S \| R_T + R1}{R_S \| R_T + R1 + R2}\right) = 3.7\left(\frac{42 + 340}{42 + 340 + 681}\right) = 1.33\,V\ .$$

The +1.33V common-mode voltage is derived from the AD680 +2.5V reference using a resistor divider and is decoupled with a 10μF/25V tantalum capacitor in parallel with a 0.1μF low-inductance ceramic one.

The AD9050 10-bit, 40MSPS single-supply ADC input range of ±0.5V is centered around a common-mode voltage of +3.3V (corresponding to an upper and lower limit of +3.8V and +2.8V, respectively). An appropriate single-supply dc-coupled drive circuit based upon the AD8011 low power, low distortion op amp is shown in Figure 4.33. The source is a ground-referenced 0 to +2V signal which is series-terminated in 75ohms. The termination resistor, R_T, is chosen such that the parallel combination of R_T and R1 is 75ohms. The AD8011 current-feedback op amp is configured for a gain of –1. The feedback resistor, R2, is the value recommended for optimum bandwidth. Assume that the video source is at zero volts. The corresponding ADC input voltage should be +3.8V. The common-mode voltage, V_{cm}, is determined from the following equation:

$$V_{cm} = 3.8\left(\frac{R_S \| R_T + R1}{R_S \| R_T + R1 + R2}\right) = 3.8\left(\frac{38.8 + 1000}{38.8 + 1000 + 1000}\right) = 1.94V$$

The common-mode voltage, V_{cm}, is derived from the common-mode voltage at the inverting input of the AD9050. The +3.3V is buffered by the AD820 single-supply FET-input op amp. A divider network generates the required +1.94V for the AD8011, and a potentiometer provides offset adjustment capability.

The AD8011 current feedback op amp was chosen because of its low power (5mW), wide bandwidth (200MHz), and low distortion (–70dBc at 5MHz). It is fully specified for both ±5V and +5V operation. When operating on a single +5V supply, the input common-mode range is +1.5V to +3.5V, and the output swing is +1.2V to +3.5V. The high speed level-shifting PNP transistor at the output of the AD8011 allows the op

amp to operate within in its recommended output range and ensures best distortion performance. Distortion performance of the entire circuit including the ADC is better than –60dBc for an input frequency of 10MHz and a sampling rate of 40MSPS.

DC-COUPLED SINGLE-SUPPLY DRIVE CIRCUIT FOR AD9050 10-BIT, 40MSPS ADC USING AD8011 OP AMP

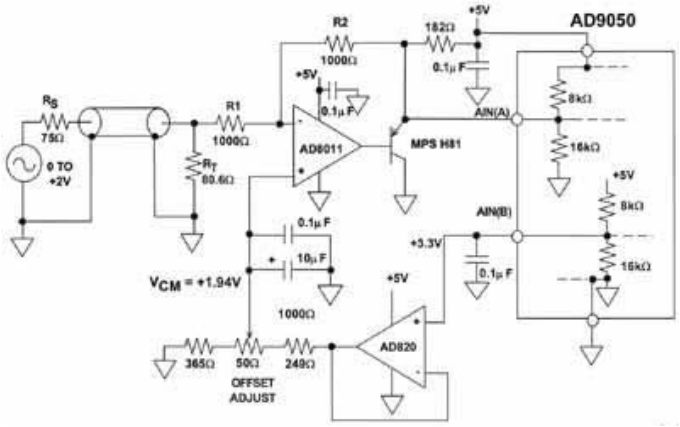


Figure 4.33

AD8011 OP AMP KEY SPECIFICATIONS

- **Low Power: 1mA Current (5mW on +5V Supply)**
- **Bandwidth: 320MHz (G=+1), 180MHz (G=+2)**
- **Settling Time: 25ns to 0.1%**
- **Low Distortion: -76dBc at 5MHz**
- **Input Common Mode Voltage (+5V Supply): +1.5V to +3.5V**
- **Output Voltage Swing (+5V Supply): +1.2V to +3.8V**
- **Fully Specified for Single or Dual-Supply Operation**

Figure 4.34

HIGH SPEED SAMPLING ADC EXTERNAL REFERENCE VOLTAGE GENERATION

Due to process and design-related constraints, it is not always possible to integrate the reference and the ADC on the same chip. In some ADCs which do have an internal reference, performance improvements (less noise and drift) may be obtained by using an external reference rather than the internal one. We saw in the case of the AD77XX series that this was the case.

There are a number of low-cost, low-noise, low-voltage references suitable for use with high performance sampling ADCs. Reference voltages of +1.25V, +2.048V, +2.5V, +3.0V, +3.3V, +4.096V, and +4.5V are ideal for single-supply (+3V or +5V) ADCs. (See Figure 4.35).

LOW VOLTAGE REFERENCE SUMMARY

REFERENCE PART #	OUTPUT (V)	TOLERANCE (mV) (max)	DRIFT ppm/°C (max)	NOISE (µV p-p, typ) 0.1 to 10Hz	SUPPLY CURRENT (mA) typ
AD780	+2.5 / +3.0	1 - 5	3 - 20	4	0.75
AD680	+2.5	5 - 10	20 - 30	8	0.195
REF43	+2.5	15 - 50	10 - 25	5	0.45
REF191	+2.048	2 - 10	5 - 25	20	0.045
REF192	+2.5	2 - 10	5 - 25	25	0.045
REF193	+3.00	10	10 - 25	30	0.045
REF196	+3.3	10	20 - 25	33	0.045
REF198	+4.096	2 - 10	5 - 25	40	0.045
REF194	+4.5	2 - 10	5 - 25	45	0.045
AD589*	+1.235	35	25 - 100	4	0.050 - 5

* Two Terminal

Figure 4.35

The AD876 requires two references: one for each end of its input range which is nominally set for +1.7V and +3.7V. The output impedance of the drive sources must be low at high frequencies to absorb the transient currents generated at the ADC reference input terminals by the internal switched capacitor circuits.

The circuit shown in Figure 4.36 makes use of the REF198 (+4.096V) reference (see previous discussion regarding the analog input drive circuit for the AD876) and a dual FET-input single-supply op amp (AD822) to generate the two voltages. The AD876 reference inputs each have a FORCE (F) and SENSE (S) pin. The Kelvin connection compensates for the voltage drop in the internal parasitic resistances (approximately 5ohms). The internal ADC reference ladder impedance is approximately 300ohms, requiring the AD822s to source and sink approximately 6.7mA. There is an additional resistance of approximately 300ohms in series with each SENSE line. The two reference FORCE pins are decoupled at low and high frequencies using both a tantalum and a ceramic capacitor. The additional 20µF across the two SENSE pins adds additional decoupling for differential transients.

Note that the AD822 must be properly compensated to drive the large capacitive load. Key specifications for the AD822 are summarized in Figure 4.37.

REFERENCE VOLTAGE GENERATOR FOR AD876 10-BIT, 20MSPS SINGLE-SUPPLY ADC

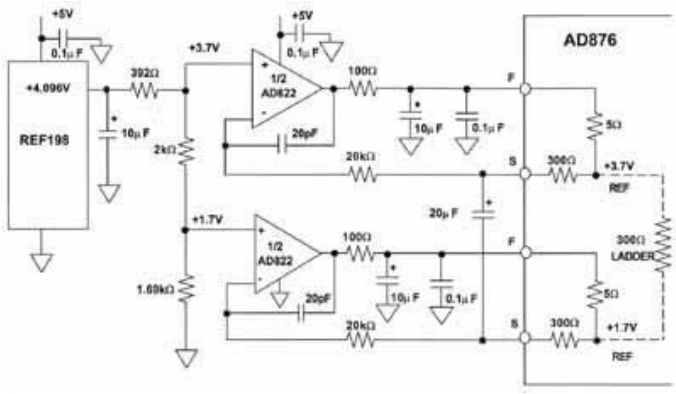


Figure 4.36

AD822 OP AMP KEY SPECIFICATIONS

- **True Single-Supply FET-Input Dual Op Amp**
- **Complete Specifications for ±15V, ±5V, +5V, +3V**
- **Input Voltage Range Extends 200mV Below Ground and to within 1V of $+V_s$**
- **Output Goes to Within 5mV of Supplies (Open-Collector Complementary Output Stage Limited by V_{cesat})**
- **1.8MHz Unity-Gain Bandwidth**
- **800μV Offset Voltage, 2μV/°C Offset Drift**
- **Low Noise: 13nV/√Hz**
- **Low Power: 800μA / Amplifier**
- **Single Version Available (AD820)**

Figure 4.37

ADC INPUT PROTECTION AND CLAMPING

The input to high speed ADCs should be protected from overdrive to prevent catastrophic damage or performance degradation. A good rule of thumb is never let the analog input exceed the supply voltage by more than 0.3V (this not only applies when the supply is on, but also when it is off, i.e., if the supply is off, the analog input should not exceed ±0.3V). In a dual supply system, this rule applies to both supplies. The rule of thumb protects most devices, but the data sheet Absolute Maximum specifications should always be consulted to determine possible exceptions. In some ADCs, the analog input is protected internally by diodes connected to the supplies. In these cases, an external resistor is required to limit the input current to 5mA or less under the overvoltage condition.
Several overdrive protection schemes which use external diodes are shown in Figure 4.38.

In Figure 4.38A, the op amp is powered from ±15V, and the ADC from ±5V. The addition of the Schottky diodes on the input will prevent the analog input from exceeding the ADC supplies. Some ADCs have internal diodes, but the addition of the external ones ensures protection for higher currents. An alternative solution is to generate the ±5V for the ADC from the op amp ±15V supplies using three terminal regulators (such as the 78L05 and 79L05). This eliminates possible sequencing and overdrive problems, and power dissipation in the regulator is not excessive if low power CMOS ADCs are used (see Figure 4.38B).

With the proliferation of high speed op amps and ADCs, both of which operate on dual 5V supplies, the situation shown in Figure 4.38C is quite common, and there is no sequencing problem provided both the amplifier and the ADC are operated from the same supplies.

Figure 4.38D shows the case where a flash converter (powered from a single –5V supply) is driven from an amplifier powered from ±5 V. The series resistor and the Schottky diode provide protection from forward-biasing the flash substrate diode more than a few tenths of a volt, thereby preventing possible damage.

ADC INPUT OVERVOLTAGE PROTECTION CIRCUITS

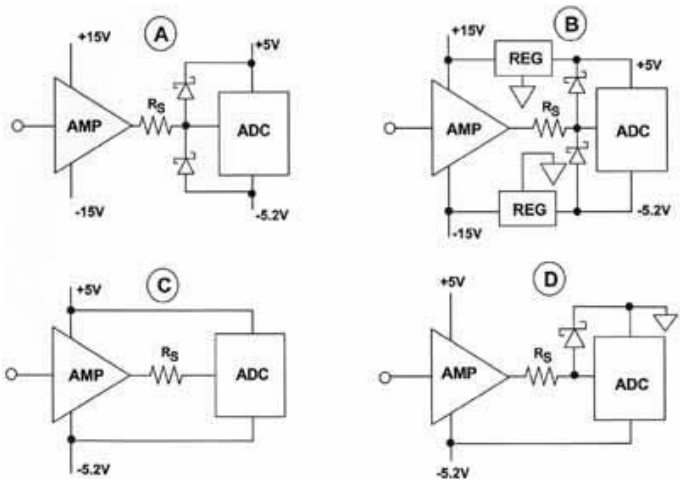


Figure 4.38

Specially designed high speed, fast recovery clamping amplifiers offer an attractive alternative to designing external clamping/protection circuits. The AD8036/AD8037 low distortion, wide bandwidth clamp amplifiers represent a significant breakthrough in this technology. These devices allow the designer to specify a high (V_H) and low (V_L) clamp voltage. The output of the device clamps when the input exceeds either of these two levels. The AD8036/AD8037 offer superior clamping performance compared to traditional output-clamping devices. Recovery time from overdrive is less than 5ns.

The key to the AD8036 and AD8037's fast, accurate clamp and amplifier performance is their proprietary input clamp architecture. this new design reduces clamp errors by more than 10x over previous output clamp based circuits, as well as substantially increasing the bandwidth, precision, and versatility of the clamp inputs.

Figure 4.39 is an idealized block diagram of the AD8036 connected as a unity gain voltage follower. The primary signal path comprises A1 (a 1200V/µs, 240MHz high voltage gain, differential to single-ended amplifier) and A2 (a G=+1 high current gain output buffer). The AD8037 differs from the AD8036 only in that A1 is optimized for closed-loop gains of two or greater.

AD8036/AD8037 CLAMP AMPLIFIER EQUIVALENT CIRCUIT

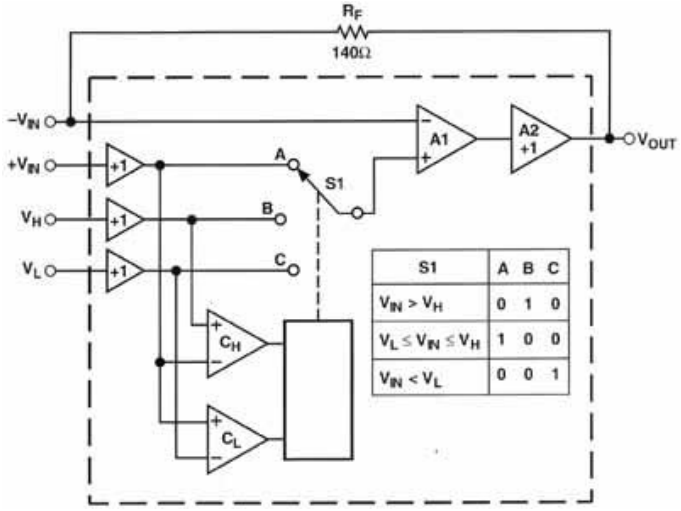


Figure 4.39

The input clamp section is comprised of comparators C_H and C_L, which drive switch S1 through a decoder. The unity-gain buffers in series with the $+V_{IN}$, V_H, and V_L inputs isolate the input pins from the comparators and S1 without reducing bandwidth or precision.

The two comparators have about the same bandwidth as A1 (240MHz), so they can keep up with signals within the useful bandwidth of the AD8036. To illustrate the operation of the input clamp circuit, consider the case where V_H is referenced to +1V, V_L is open, and the AD8036 is set for a gain of +1 by connecting its output back to its inverting input through the recommended 140ohm feedback resistor. Note that the main signal path always operates closed loop, since the clamping circuit only affects A1's noninverting input.

If a 0V to +2V voltage ramp is applied to the AD8036's $+V_{IN}$ for the connection just described, V_{OUT} should track $+V_{IN}$ perfectly up to +1V, then should limit at exactly +1V as $+V_{IN}$ continues to +2V.

In practice, the AD8036 comes close to this ideal behavior. As the $+V_{IN}$ input voltage ramps from zero to 1V, the output of the high limit comparator C_H starts in the off state, as does the output of C_L. When $+V_{IN}$ just exceed V_H (practically, by about 18mV), C_H changes state, switching S1 from "A" to "B" reference level. Since the + input of A1 is now connected to V_H, further increases in $+V_{IN}$ have no effect on the AD8036's output voltage. The AD8036 is now operating as a unity-gain buffer for the V_H input, as any variation in V_H, for V_H > 1V, will be faithfully produced at V_{OUT}.

Operation of the AD8036 for negative input voltages and negative clamp levels on V_L is similar, with comparator C_L controlling S1. Since the comparators see the

voltage on the $+V_{IN}$ pin as their common reference level, the voltage V_H and V_L are defined as "High" or "Low" with respect to $+V_{IN}$. For example, if V_{IN} is set to zero volts, V_H is open, and V_L is +1V, comparator C_L will switch S1 to "C", so the AD8036 will buffer the voltage on V_L and ignore $+V_{IN}$.

The performance of the AD8036/AD8037 closely matches the ideal just described. The comparator's threshold extends from 60mV inside the clamp window defined by the voltages on V_L and V_H to 60mV beyond the window's edge. Switch S1 is implemented with current steering, so that A1's + input makes a continuous transition from say, V_{IN} to V_H as the input voltage traverses the comparator's input threshold from 0.9V to 1.0V for V_H = 1.0V.

The practical effect of the non-ideal operation is to soften the transition from amplification to clamping modes, without compromising the absolute clamp limit set by the input clamping circuit. Figure 4.40 is a graph of V_{OUT} versus V_{IN} for the AD8036 and a typical *output* clamp amplifier. Both amplifiers are set for G=+1 and V_H = +1V.

COMPARISON BETWEEN INPUT AND OUTPUT CLAMPING

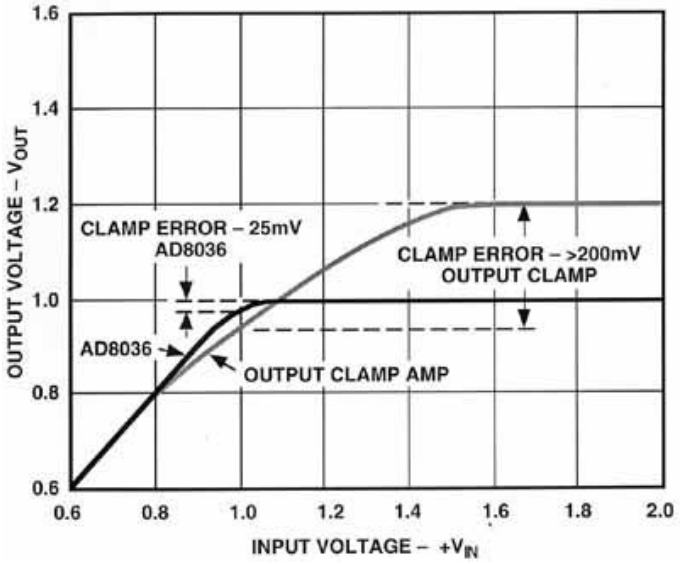


Figure 4.40

The worst case error between V_{OUT} (ideally clamped) and V_{OUT} (actual) is typically 18mV times the amplifier closed-loop gain. This occurs when V_{IN} equals V_H (or V_L). As V_{IN} goes above and/or below this limit, V_{OUT} will stay within 5mV of the ideal value.

In contrast, the output clamp amplifier's transfer curve typically will show some compression starting at an input of 0.8V, and can have an output voltage as far as 200mV over the clamp limit. In addition, since the output clamp causes the amplifier

to operate open-loop in the clamp mode, the amplifier's output impedance will increase, potentially causing additional errors, and the recovery time is significantly longer.

It is important that a clamped amplifier such as the AD8036/AD8037 maintain low levels of distortion when the input signals are close the clamping voltages. Figure 4.41 shows the second and third harmonic distortion for the amplifiers as the output approaches the clamp voltages. The input signal is 20MHz, the output signal is 2V peak-to-peak, and the output load is 100ohms.

Recovery from step voltage which is two times over the clamping voltage is shown in Figure 4.42. The input step voltage starts at +2V and goes to 0V (left-hand traces on scope photo). The input clamp voltage (V_H) is set at +1V. The right-hand trace shows the output waveform. The key specifications for the AD8036/AD8037 clamped amplifiers are summarized in Figure 4.43.

AD8036/AD8037 DISTORTION NEAR CLAMPING REGION, OUTPUT = 2V p-p, LOAD = 100Ω, f = 20MHz

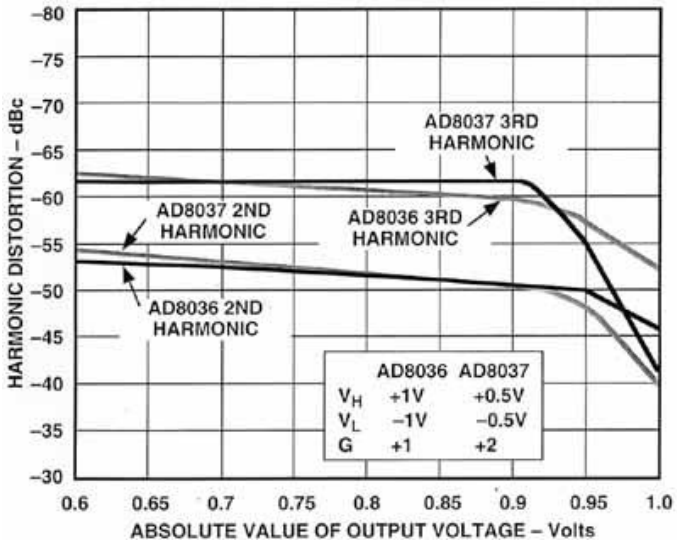


Figure 4.41

AD8036 / AD8037 OVERDRIVE (2x) RECOVERY

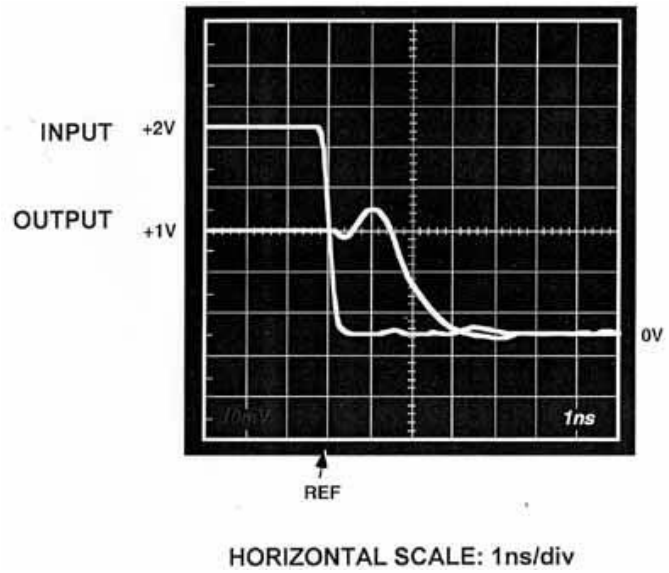


Figure 4.42

AD8036 / AD8037 SUMMARY SPECIFICATIONS

- **Proprietary Input Clamping Circuit with Minimized Nonlinear Clamping Region**
- **Small Signal Bandwidth: 240MHz (AD8036), 270MHz (AD8037)**
- **Slew Rate: 1500V/μs**
- **1.5ns Overdrive Recovery**
- **Low Distortion: -72dBc @ 20MHz (500Ω load)**
- **Low Noise: 4.5nv/√Hz, 2pA/√Hz**
- **20mA Supply Current on ±5V**

Figure 4.43

Figure 4.44 shows the AD9002 8-bit, 125MSPS flash converter driven by the AD8037 (240MHz bandwidth) clamping amplifier. In the circuit, the bandwidth of the AD8037 is 240MHz. The clamp voltages on the AD8037 are set to +0.55 and –0.55V, referenced to the ±0.5V input signal, with the external resistive dividers. The AD8037 also supplies a gain of two, and an offset of –1V (using the AD780 voltage reference), to match the 0 to –2V input range of the AD9002 flash converter. The output signal is clamped at +0.1V and –2.1V. This multi-function clamping circuit therefore performs several important functions as well as preventing damage to the

flash converter which occurs if its input exceeds +0.5V, thereby forward biasing the substrate diode. The 1N5712 Schottky diode adds further protection during power-up.

AD9002 8-BIT, 125MSPS FLASH CONVERTER DRIVEN BY AD8037 CLAMP AMPLIFIER

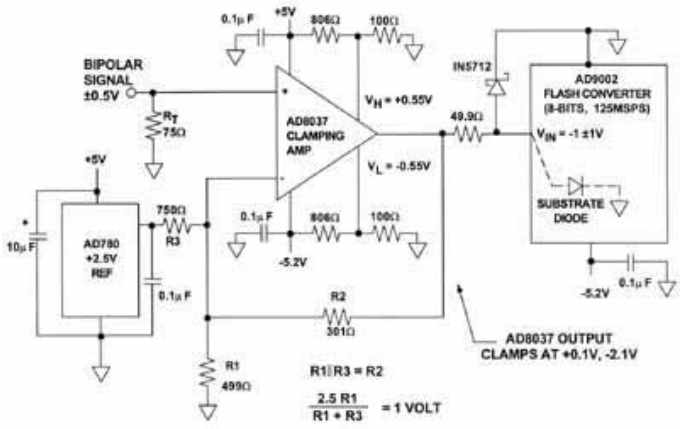


Figure 4.44

The feedback resistor, R2 = 301ohms, is selected for optimum bandwidth per the manufacturer's data sheet recommendation. In order to give a gain of two, the parallel combination of R1 and R3 must also equal R2:

$$\frac{R1 \cdot R3}{R1 + R3} = R2 = 301\Omega$$ (nearest 1% standard resistor value).

In addition, the Thevenin equivalent output voltage of the AD780 +2.5V reference and the R3/ R1 divider must be +1V to provide the –1V offset at the output of the AD8037.

$$\frac{2.5 \cdot R1}{R1 + R3} = 1\text{volt}$$

Solving the two simultaneous equations yields R1 = 499ohms, R3 = 750ohms (using the nearest 1% standard resistor values).

Other input and output voltages ranges can be accommodated by appropriate changes in the external resistors.

OTHER APPLICATIONS FOR CLAMPING AMPLIFIERS

The AD8036/AD8037's clamp output can be set accurately and has a well controlled flat level. This, along with wide bandwidth and high slew rate make them well suited for a number of other applications. Figure 4.45 is a diagram of a programmable level pulse generator. The circuit accepts a TTL timing signal for its input and generates pulses at the output up to 24V p-p with 2500V/µs slew rate. The output levels can be programmed to anywhere in the range between –12V to +12V.

PROGRAMMABLE PULSE GENERATOR USING AD8037 CLAMP AMP AND AD811 OP AMP

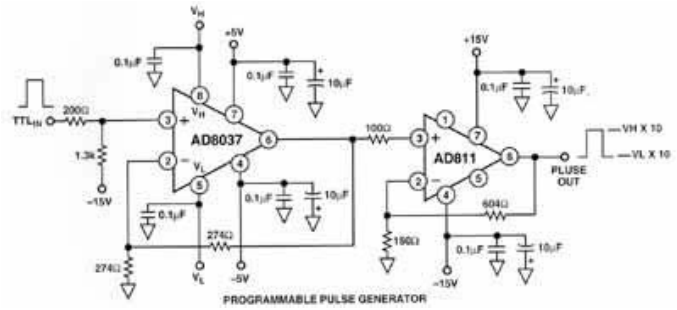


Figure 4.45

The circuit uses an AD8037 operating at a gain of two with an AD811 to boost the output to the ±12V range. The AD811 was chosen for its ability to operate with ±15V supplies and its high slew rate.

R1 and R2 act as a level shifter to make the TTL signal levels approximately symmetrical above and below ground. This ensures that both the high and low logic levels will be clamped by the AD8037. For well controlled signal levels in the output pulse, the high and low output levels result from the clamping action of the AD8037 and are not controlled by either the high or low logic levels passing through a linear amplifier. For good rise and fall times at the output pulse, a logic family with high speed edges should be used.

The high logic levels are clamped at 2 times the voltage at V_H, while the low logic levels are clamped at two times the voltage at V_L. The output of the AD8037 is amplified by the AD811 operating at a gain of 5. The overall gain of 10 will cause the high output level to be 10 times the voltage at V_H, and the low output level to be 10 times the voltage at V_L.

The clamping inputs are additional inputs to the input stage of the AD8036/AD8037. As such, they have an input bandwidth comparable to the amplifier inputs and lend themselves to some unique functions when they are driven dynamically.

Figure 4.46 is a schematic for a full wave rectifier, sometimes called an absolute value generator. It works well up to 20MHz and can operate at significantly higher

frequencies with some degradation in performance. The distortion performance is significantly better than diode-based full-wave rectifiers, especially at high frequencies.

FULL-WAVE RECTIFIER USING AD8037 CLAMP AMP

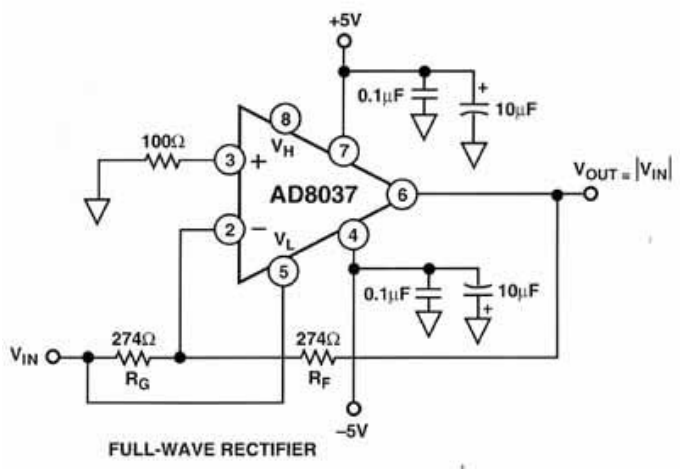


Figure 4.46

The AD8037 is configured as an inverting amplifier with a gain of unity. The input drives the inverting amplifier and also directly drives V_L, the lower level clamping input. The high level clamping input, V_H, is left floating and plays no role in the circuit.

When the input is negative, the amplifier acts as a unity-gain inverter and outputs a positive signal at the same amplitude as the input, with opposite polarity. V_L is driven negative by the input, so it performs no clamping action, because the positive output signal is always higher than the negative level driving V_L.

When the input is positive, the output result is the sum of two separate effects. First, the inverting amplifier multiplies the input by –1 because of the unity-gain inverting configuration. This effectively produces as offset as explained above, but with a dynamic level that is equal to –1 times the input. Second, although the positive input is grounded (through 100ohms), the output is clamped at two times the voltage applied to V_L (a positive, dynamic voltage in this case). The factor of two is because the noise gain of the amplifier is two.

The sum of these two actions results in an output that is equal to unity times the input signal for positive input signals as shown in Figure 4.47. An input/output scope photo with an input signal of 20MHz and an amplitude of ±1V is shown in Figure 4.48. Thus, for either positive or negative input signals, the output is unity times the absolute value of the input signal. The circuit can be easily configured to produce the negative absolute value of the input by applying the input to V_H rather than V_L.

FULL-WAVE RECTIFIER WAVEFORMS

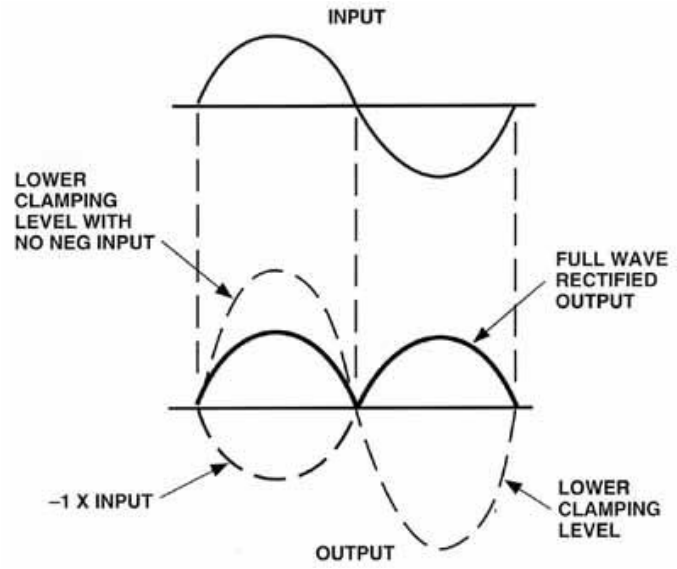


Figure 4.47

FULL-WAVE RECTIFIER INPUT/OUTPUT SCOPE WAVEFORM

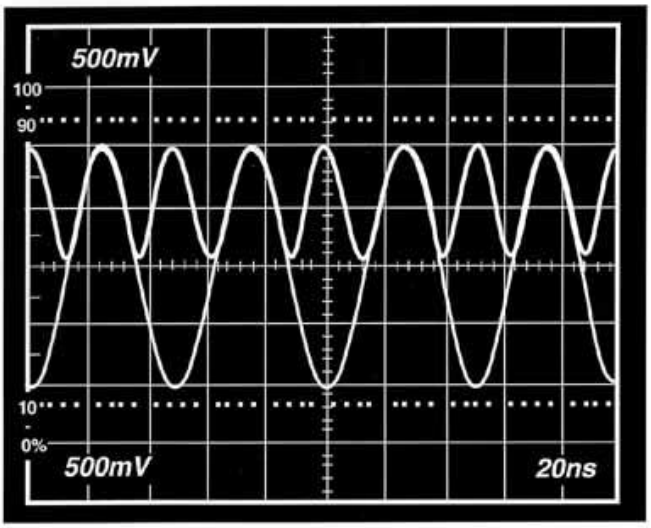


Figure 4.48

The circuit can get to within about 40mV of ground during the time when the input crosses zero. This voltage is fixed over a wide frequency range, and is a result of the switching between the conventional op amp input and the clamp input. But because

there are no diodes to rapidly switch from forward to reverse bias, the performance far exceeds diode-based full wave rectifiers.

The 40mV offset can be removed by adding an offset to the circuit. A 27.4kohm input resistor to the inverting input will have a gain of 0.01, while changing the gain of the circuit by only 1%. A plus or minus 4V dc level (depending on the polarity of the rectifier) into this resistor will compensate for the offset.

Full wave rectifiers are useful in many applications including AM signal detection, high frequency ac voltmeters, and various arithmetic operations.

The AD8037 can also be configured as an amplitude modulator as shown in Figure 4.49. The positive input of the AD8037 is driven with a square wave of sufficient amplitude to produce clamping action at both the high and low levels. This is the higher frequency carrier signal. The modulation signal is applied to both the input of a unity gain inverting amplifier and to V_L, the lower clamping input. V_H is biased at +0.5V.

AD8037 AMPLITUDE MODULATOR

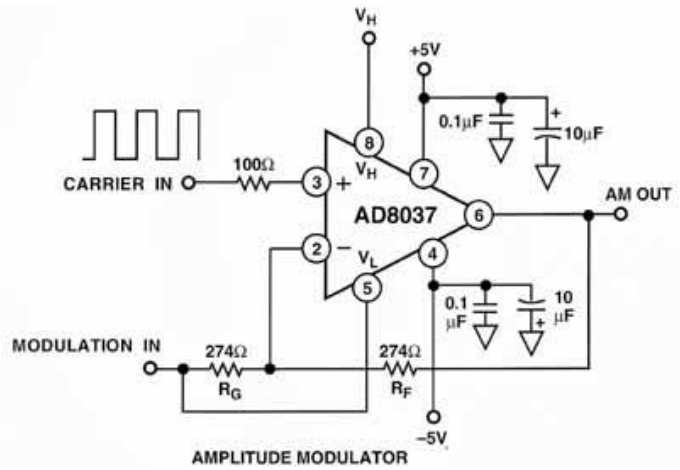


Figure 4.49

AMPLITUDE MODULATED WAVEFORM

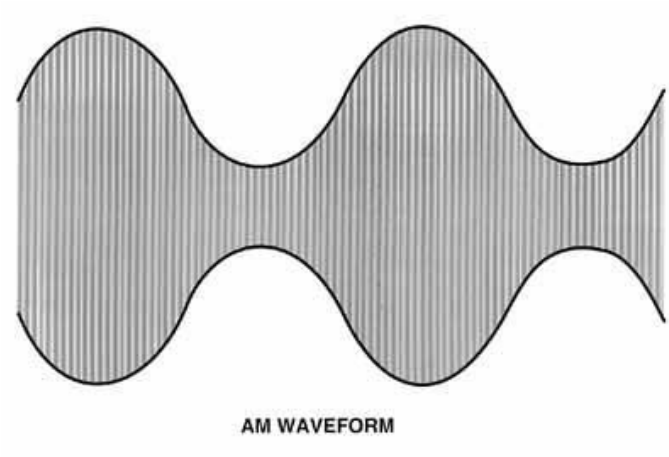


Figure 4.50

To understand the circuit operation, it is helpful to first consider a simpler circuit. If both V_L and V_H are dc biased at –0.5V and the carrier and modulation inputs driven as above, the output would be a 2V p-p square wave at the carrier frequency riding on a waveform at the modulating frequency. The inverting input (modulation signal) is creating a varying offset to the 2V p-p square wave at the output. Both the high and low levels clamp at twice the input levels on the clamps because the noise gain of the circuit is two.

When V_L is driven by the modulation signal instead of being held at a dc level, a more complicated situation results. The resulting waveform is composed of an upper envelope and a lower envelope with the carrier square wave in between. The upper and lower envelopes are 180° out of phase as in a typical AM waveform.

The upper envelope is produced by the upper clamp level being offset by the waveform applied to the inverting input. This offset is the opposite polarity of the input waveform because of the inverting configuration.

The lower envelope is produced by the sum of two effects. First, it is offset by the waveform applied to the inverting input as in the case of the simpler circuit above. The polarity of this offset is in the same direction as the upper envelope. Second, the output is driven in the opposite direction of the offset at twice the offset voltage by the modulation signal being applied to V_L. This results from the noise gain being equal to two, and since there is no inversion in this connection, it is opposite polarity from the offset.

The result at the output for the lower envelope is the sum of these two effects, which produces the lower envelope of an AM waveform. The depth of modulation can be modified by changing the amplitude of the modulation signal. This changes the amplitude of the upper and lower envelope waveforms. The modulation depth can also be changed by changing the dc bias applied to V_H. In this case, the amplitudes

of the upper and lower envelope waveforms stay constant, but the spacing between them changes. This alters the ratio of the envelope amplitude to the amplitude of the overall waveform.

NOISE CONSIDERATIONS IN HIGH SPEED SAMPLING ADC APPLICATIONS

High speed, wide bandwidth sampling ADCs are optimized for dynamic performance over a wide range of analog input frequencies. Because of the wide bandwidth front ends coupled with internal device and resistor noise, DC inputs generally produce a range of output codes as shown in Figure 4.51. The correct code appears most of the time, but adjacent codes appear with reduced probability. If a normal probability density curve is fitted to this distribution, the standard deviation will be equal to the equivalent rms input noise of the ADC.

OUTPUT HISTOGRAM OF AD9022 12-BIT, 20MSPS ADC SHOWS EFFECTIVE INPUT NOISE OF 0.57LSB FOR DC INPUT

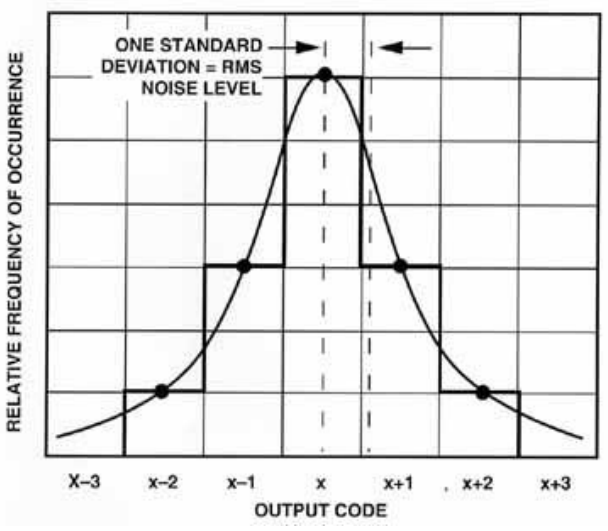


Figure 4.51

For instance, the equivalent input noise of the AD9022 12-bit, 20MSPS ADC is approximately 0.57LSB rms. This implies that the best full scale sinewave signal-to-noise ratio that can be obtained is approximately 68dB. (Full scale sinewave peak-to-peak amplitude = 4096LSBs, or 1448LSBs rms, from which the SNR is calculated as 20 log10[1448/0.57] = 68dB). In fact, the SNR of the ADC is limited by other factors, such as quantization noise and distortion.

When driving sampling ADCs with wideband op amps, the output noise of the drive amplifier can contribute to the overall ADC noise floor. A few quick calculations

should be made to estimate the total output noise of the op amp and see if it is significant with respect to the ADC noise.

The complete noise model for an op amp is shown in Figure 4.52. This model is accurate, provided there is less than 1 or 2dB peaking in the closed-loop output frequency response. Excessive peaking in the frequency response increases the effects of the wide band noise, and the simple approximation will give optimistic results.

GENERALIZED OP AMP NOISE MODEL

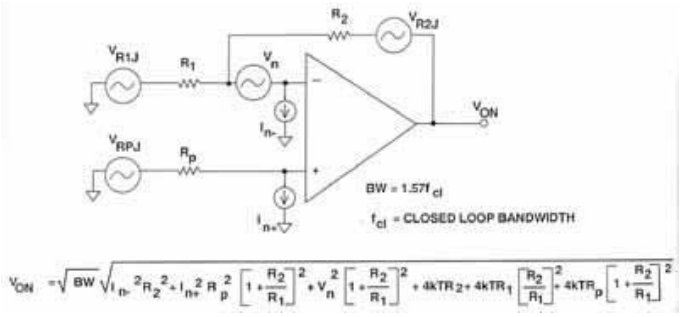


Figure 4.52

It is rarely necessary to consider all noise sources, since sources which have noise contributions 50% smaller than the largest can be neglected. In high speed systems, where the resistors of the source and the op amp feedback network rarely exceed 1kohm, the resistor Johnson noise can usually be neglected.

In the case of voltage feedback op amps, the input current noise can usually be neglected. For current feedback op amps operating at noise gains of approximately 4 or less, the inverting input current noise generally dominates. At higher noise gains, however, the effects of voltage noise become significant and should be included.

SIMPLIFICATIONS IN NOISE CALCULATIONS

- **Voltage Feedback Op Amps:**
  - **Neglect Resistor Noise if Resistors < 1kΩ**
  - **Neglect Input Current Noise**
- **Current Feedback Op Amps:**
  - **Neglect Resistor Noise if Resistors < 1kΩ**
  - **Neglect Non-Inverting Input Current Noise**
  - **Evaluate Effects of Both Input Voltage Noise (Dominates at High Noise Gains)**

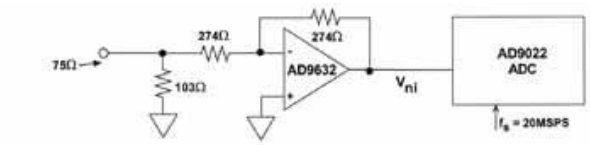
and

Inverting Input Current Noise (Dominates at Low Noise Gains)

Figure 4.53

As an example to show the effects of noise, consider the circuit shown in Figure 4.54, where the AD9022 12-bit, 20MSPS ADC is driven by the AD9632 low-distortion op amp. Because the AD9632 is a voltage feedback op amp and the external resistor values are less than 1kohm, only the voltage noise (4.3nV/rtHz) is significant to the calculation. Because the AD9632 is operated with a noise gain of 2, the output voltage noise is 8.6nv/rtHz (excluding any source noise).

NOISE CALCULATIONS FOR AD9632 OP AMP DRIVING AD9022 12-BIT, 20MSPS ADC



AD9632 OP AMP SPECIFICATIONS	AD9022 ADC SPECIFICATIONS
Input Voltage Noise = 4.3nV/√Hz	Effective Input Noise = 285μV rms
Closed-Loop Bandwidth = 250MHz	Input Bandwidth = 110Mhz

- AD9632 Output Noise Spectral Density = 2 × 4.3nV/√Hz = 8.6nV/√Hz
- Bandwidth for Integration = 110MHz (AD9022 Input Bandwidth)
- $V_{ni} = \frac{8.6nV}{\sqrt{Hz}} \bullet \sqrt{110 \times 10^6 \times 1.57Hz} = 113\mu V\ rms$
- Less than 50% of AD9022 Effective Input Noise (285μV rms)

Figure 4.54

The bandwidth for integration is either the op amp closed-loop bandwidth (250MHz), or the ADC input bandwidth (110MHz), whichever is less. This is an important point, because in most cases (especially when dealing with low-distortion, wide

bandwidth amplifiers), the input of the ADC acts as the low pass filter to the op amp noise.

The calculation for the op amp noise contribution at the ADC input is simple:

$$V_{ni} = \frac{8.6nV}{\sqrt{Hz}} \bullet \sqrt{110 \times 10^6 \times 1.57\,Hz} = 113\mu V \text{ rms}$$

The factor of 1.57 is required to convert the single-pole 110MHz ADC input bandwidth into an equivalent noise bandwidth. The op amp contribution of 113µV rms is less than one-half the effective input noise of the AD9022 (0.57LSB = 285µV rms), and can therefore be neglected.

In most high speed system applications, a passive antialiasing filter (either lowpass for baseband sampling, or bandpass for harmonic or undersampling) is required. Placing this filter between the op amp and the ADC will further reduce the effects of the drive amplifier noise.

PROPER POSITIONING OF THE ANITALIASING FILTER WILL REDUCE THE EFFECTS OF THE OP AMP NOISE

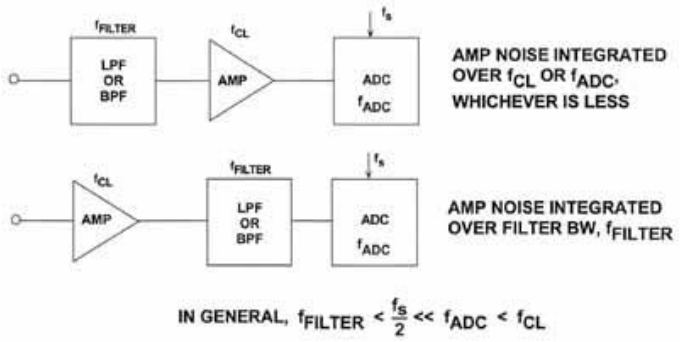


Figure 4.55

The op amp noise rarely limits the performance of high speed systems. The largest source of unwanted noise generally comes from improper attention to good high speed layout, grounding, and decoupling techniques.

ADC NOISE SOURCES

- **ADC Distortion and Quantization Noise**
- **ADC Equivalent Input Noise**
- **Internal SHA Aperture Jitter**
- **External Drive Amplifier**
- **Poor Grounding and Decoupling Techniques**
- **Poor Layout and Signal Routing Techniques**
- **Noisy Sampling Clock**
- **External Switching Power Supply**

Figure 4.56

Proper power supply decoupling techniques must be used on each PC board in the system. Figure 4.57 shows an arrangement which will ensure minimum problems. The power supply input (usually brought into the PC board on multiple pins) is first decoupled to the large-area low-impedance ground plane with a good quality, low ESL and low ESR tantalum electrolytic capacitor. This capacitor bypasses low frequency noise to the ground plane. The ferrite bead reduces high frequency noise to the rest of the circuit. You should then place one low-inductance ceramic capacitor at each power pin on each IC. Ideally, you should use surface-mount chip capacitors for minimum inductance, but if you use leaded ceramics, be sure to minimize the lead lengths by mounting them flush on the PC board. Some ICs may require an additional small tantalum electrolytic capacitor (usually between 1 and 5µF). The data sheets for each IC should provide appropriate recommendations, but when in doubt, put them in!

PROPER POWER SUPPLY DECOUPLING AT EACH IC ON THE PC BOARD IS CRITICAL TO ACHIEVING GOOD HIGH SPEED SYSTEM PERFORMANCE

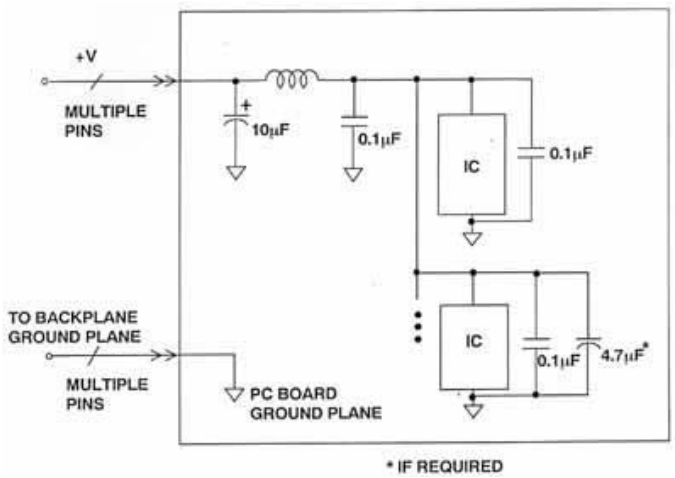


Figure 4.57

If a double-sided PC board is used, one side should be dedicated entirely (at least 75% of the total area) to the ground plane. The ICs are mounted on this side, and connections are made on the opposite side. Because of component interconnections, however, a few breaks in the ground plane are usually unavoidable. As more and more of the ground plane is eaten away for interconnections, its effectiveness diminishes. It is therefore recommended that multilayer PC boards be used where component packing density is high. Dedicate at least one entire layer to the ground plane.

When connecting to the backplane, use a number of pins (30 to 40%) on each PC board connector for ground. This will ensure that the low impedance ground plane is maintained between the various PC boards in a multicard system.

In practically all high speed systems, it is highly desirable to physically separate sensitive analog components from noisy digital components. It is usually a good idea to also establish separate analog and digital ground planes on each PC board as shown in Figure 4.58. The separate analog and digital ground planes are continued on the backplane using either motherboard ground planes or "ground screens" which are made up of a series of wired interconnections between the connector ground pins. The ground planes are joined together at the system *star ground* , or *single-point ground*, usually located at the common return point for the power supplies. The Schottky diodes are inserted to prevent accidental dc voltages from developing between the two ground systems.

SEPARATING ANALOG AND DIGITAL GROUNDS IN A MULTICARD, STAR GROUND SYSTEM

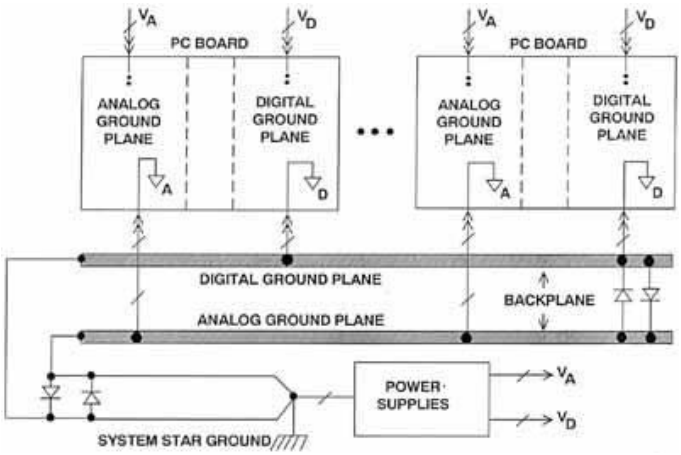


Figure 4.58

Sensitive analog components such as amplifiers and voltage references are referenced and decoupled to the analog ground plane. *The ADCs and DACs (and even some mixed-signal ICs) should be treated as analog circuits and also grounded and decoupled to the analog ground plane*. At first glance, this may seem somewhat contradictory, since a converter has an analog and digital interface and usually pins designated as analog ground (AGND) and digital ground (DGND). The diagram shown in Figure 4.59 will help to explain this seeming dilemma.

PROPER GROUNDING OF ADCs, DACs, AND OTHER MIXED-SIGNAL Ics

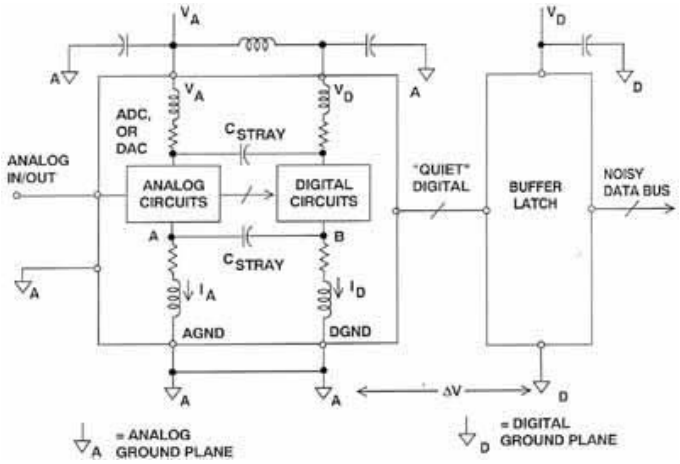


Figure 4.59

Inside an IC that has both analog and digital circuits, such as an ADC or a DAC, the grounds are usually kept separate to avoid coupling digital signals into the analog circuits. Figure 4.59 shows a simple model of a converter. There is nothing the IC designer can do about the wirebond inductance and resistance associated with connecting the pads on the chip to the package pins except to realize it's there. The rapidly changing digital currents produce a voltage at point B which will inevitably couple into point A of the analog circuits through the stray capacitance, C_{STRAY}. In addition, there is approximately 0.2pF unavoidable stray capacitance between every pin of the IC package! It's the IC designer's job to make the chip work in spite of this. However, in order to prevent further coupling, the AGND and DGND pins should be joined together externally to the *analog* ground plane with minimum lead lengths. Any extra impedance in the DGND connection will cause more digital noise to be developed at point B; it will, in turn, couple more digital noise into the analog circuit through the stray capacitance.

The name "DGND" on an IC tells us that this pin connects to the digital ground of the IC. It does not say that this pin must be connected to the digital ground of the system.

It is true that this arrangement will inject a small amount of digital noise on the analog ground plane. These currents should be quite small, and can be minimized by ensuring that the converter input/or output does not drive a large fanout. Minimizing the fanout on the converter's digital port will also keep the converter logic transitions relatively free from ringing, and thereby minimize any potential coupling into the analog port of the converter. The logic supply pin (V_D) can be further isolated from the analog supply by the insertion of a small ferrite bead as shown in Figure 4.60. The internal digital currents of the converter will return to ground through the V_D pin decoupling capacitor (mounted as close to the converter

as possible) and will not appear in the external ground circuit. It is always a good idea (as shown in Figure 4.60) to place a buffer latch adjacent to the converter to isolate the converter's digital lines from any noise which may be on the data bus. Even though a few high speed converters have three-state outputs/inputs, this isolation latch represents good design practice.

The buffer latch and other digital circuits should be grounded and decoupled to the digital ground plane of the PC board. Notice that any noise between the analog and digital ground plane reduces the noise margin at the converter digital interface. Since digital noise immunity is of the orders of hundreds or thousands of millivolts, this is unlikely to matter.

POWER SUPPLY, GROUNDING, AND DECOUPLING POINTS

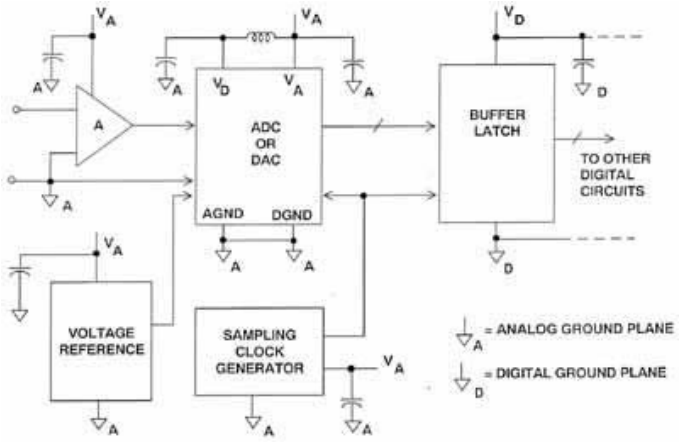


Figure 4.60

The sampling clock generation circuitry should also be grounded and heavily-decoupled to the analog ground plane. As previously discussed, phase noise on the sampling clock produces degradation in system SNR.

Separate power supplies for analog and digital circuits are also highly desirable. The analog supply should be used to power the converter. If the converter has a pin designated as a digital supply pin (V_D), it should either be powered from a separate analog supply, or filtered as shown in the diagram. All converter power pins should be decoupled to the analog ground plane, and all logic circuit power pins should be decoupled to the digital ground plane. If the digital power supply is relatively quiet, it may be possible to use it to supply analog circuits as well, but be very cautious.

A low phase-noise crystal oscillator should be used to generate the ADC sampling clock, because sampling clock jitter modulates the input signal and raises the noise and distortion floor. The sampling clock generator should be isolated from noisy digital circuits and grounded and decoupled to the analog ground plane, as is true for the op amp and the ADC.

It is evident that we can minimize noise by paying attention to the system layout and preventing different signals from interfering with each other. High level analog signals should be separated from low level analog signals, and both should be kept away from digital signals. We have seen elsewhere that in waveform sampling and reconstruction systems the sampling clock (which is a digital signal) is as vulnerable to noise as any analog signal, but is as liable to cause noise as any digital signal, and so must be kept isolated from both analog and digital systems.

SIGNAL ROUTING IN MIXED SIGNAL SYSTEMS

- **Physically separate analog and digital signals.**
- **Avoid crossovers between analog and digital signals.**
- **Be careful with sampling clock and ADC/DAC analog runs.**
- **Use lots of ground plane.**
- **Use microstrip techniques at high frequencies for controlled impedances and controlled return current paths.**
- **Use surface mount components in high frequency systems to minimize parasitic capacitance and inductance.**

Figure 4.61

If a ground plane is used, as it should in be most cases, it can act as a shield where sensitive signals cross. Figure 4.62 shows a good layout for a data acquisition system where all sensitive areas are isolated from each other and signal paths are kept as short as possible. While real life is rarely as tidy as this, the principle remains a valid one.

A PC BOARD LAYOUT SHOWING GOOD SIGNAL ROUTING

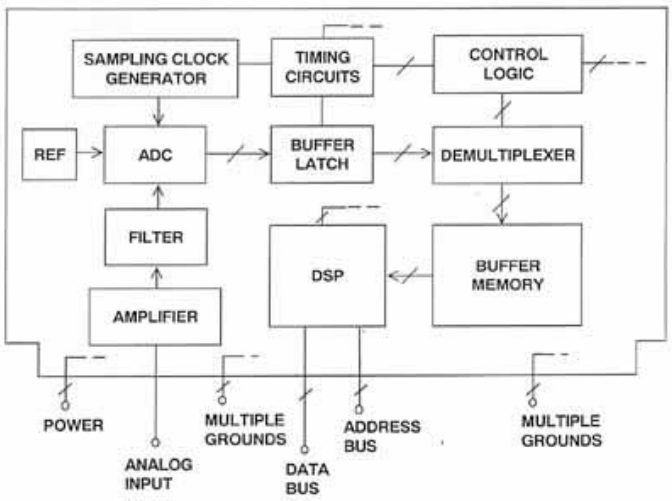


Figure 4.62

There are a number of important points to be considered when making signal and power connections. First of all a connector is one of the few places in the system where all signal conductors must run parallel - it is therefore a good idea to separate them with ground pins (creating a faraday shield) to reduce coupling between them.

EDGE CONNECTIONS

- **Separate sensitive signal by ground pins.**
- **Keep down ground impedances with multiple (30-40% of total) ground pins.**
- **Have several pins for each power line.**
- **Critical signals such as analog or sampling clocks may require a separate connector (possibly coax), or microstrip techniques.**

Figure 4.63

Multiple ground pins are important for another reason: they keep down the ground impedance at the junction between the board and the backplane. The contact resistance of a single pin of a PCB connector is quite low (of the order of 10 milliohms) when the board is new - as the board gets older the contact resistance is likely to rise, and the board's performance may be compromised. It is therefore well worthwhile to afford extra PCB connector pins so that there are many ground connections (perhaps 30-40% of all the pins on the PCB connector should be ground pins). For similar reasons there should be several pins for each power connection, although there is no need to have as many as there are ground pins.

It is tempting to mount expensive ICs in sockets rather than soldering them in circuit - especially during circuit development. Engineers would do well not to succumb to this temptation.

USE OF SOCKETS WITH HIGH PERFORMANCE ANALOG CURCUITS

- **DON'T! (If at all possible)**
- **Use "Pin sockets" or "Cage jacks" such as Amp Part No: 5-330808-3 or 5-330808-6 (Capped & uncapped respectively)**
- **Always test the effect of sockets by comparing system performance with and without the use of sockets.**
- **Do not change the type of socket or manufacturer used without evaluating the effects of the change on performance.**

Figure 4.64

Sockets add resistance, inductance and capacitance to the circuit and may degrade performance to quite unacceptable levels. When this occurs, though, it is always the

IC manufacturer who is blamed - not the use of a socket. Even low profile, low insertion force sockets cannot be relied upon to ensure the performance of high performance (high speed or high precision or, worst of all, both) devices. As the socket ages and the board suffers vibration, the contact resistance of low insertion force sockets is very likely to rise. Where a socket must be used the best performance is achieved by using individual pin sockets (sometimes called "cage jacks") to make up a multi-pin socket in the PCB itself (see Section 9).

It really is best not to use IC sockets with high performance analog and mixed signal circuits. If their use can be avoided it should be. However at medium speeds and medium resolutions the trade-off between performance and convenience may fall on the side of convenience. It is very important, when sockets are used, to evaluate circuit performance with and without the socket chosen to ensure that the type of socket chosen really does have minimal effect on the way that the circuit behaves. The effects of a change of socket on the circuit should be evaluated as carefully as a change of IC would be, and the drawings should be prepared so that the change procedures for a socket are as rigorous as for an IC - in order to prevent a purchase clerk who knows nothing of electronics from devastating the system performance in order to save five cents on a socket.

The switching-mode power supply offers low cost, small size, high efficiency, high reliability and the possibility of operating from a wide range of input voltages without adjustment. Unfortunately, these supplies produce noise over a broad band of frequencies, and this noise occurs as conducted noise, radiated noise, and unwanted electric and magnetic fields. When used to supply logic circuits, even more noise is generated on the power supply bus. The noise transients on the output lines of switching supplies are short-duration voltage spikes. Although the actual switching frequencies may range from 10 to 100kHz, these spikes can contain frequency components that extend into the hundreds of megahertz.

Because of the wide variations in the noise characteristics of commercially available switching supplies, they should always be purchased in accordance with a specification-control drawing. Although specifying switching supplies in terms of rms noise is common practice, you should also specify the peak amplitudes of the switching spikes under the output loading conditions you expect in your system. You should also insist that the switching-supply manufacturer inform you of any internal supply design changes that may alter the spike amplitudes, duration, or switching frequency. These changes may require corresponding changes in the external power-supply filtering networks.

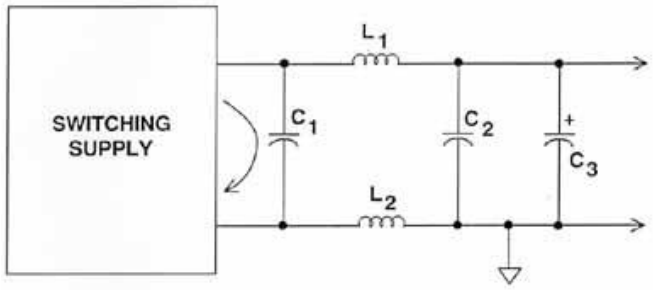
SWITCHING-MODE POWER SUPPLIES

- **Generate Conducted and Radiated Noise as Well as Electric and Magnetic Fields (HF and LF)**
- **Outputs Must be Adequately Filtered if Powering Sensitive Analog Circuits**
- **Optimum Filter Design Depends on Power Supply Characteristics. Beware of Power Supply Design Changes.**
- **Use Faraday Shields to Reduce HF Electric and HF Magnetic Fields**
- **Physically Isolate Supply from Analog Circuits**
- **Temporarily Replace Switching Supply with Low-Noise Linear Supply or Battery when Suspicious of Switching Supply Noise**

Figure 4.65

Filtering switching supply outputs that provide several amps and generate voltage spikes having high frequency components is a challenge. For this reason, you should place the initial filtering burden on the switching supply manufacturer. Even so, external filtering such as shown in Figure 4.66 should be added. The series inductors isolate both the output and common lines from the external circuits. Because the load currents may be large, make sure that the inductors selected do not saturate. Split-core inductors or large ferrite beads make a good choice. Because the switching power supplies generate high and low frequency electric and magnetic fields, they should be physically separated as far as possible from critical analog circuitry. This is especially important in preventing the inductive coupling of low frequency magnetic fields.

FILTERING A SWITCHING SUPPLY OUTPUT



- C_1 MUST HAVE LOW INDUCTANCE AND BE CLOSE TO THE SUPPLY TO MINIMIZE HF CURRENT LOOPS AND RESULTANT HF MAGNETIC FIELDS
- C_2 IS ALSO LOW INDUCTANCE, C_3 IS ELECTROLYTIC
- IF THE SWITCHING SUPPLY IS INTERNALLY GROUNDED, L_2 SHOULD BE OMITTED

Figure 4.66

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