FYS9220

Lab Exercise 4

NIOS II processor in FPGA

Note: Only mandatory for PhD students!

Introduction to the lab

The purpose of this lab exercise is to introduces you to the system development flow for the Nios II processor. Using the Quartus II software and the Nios II Embedded Design Suite (EDS) including the Altera SOPC builder, you are to build a Nios II hardware system design and create software programs that runs on the Nios II system and interfaces with components on the Altera DE2-70 development board.

The text ***"Introduction to the Altera Nios II Soft Processor"*** can be used as a reference for the architecture of Nios II and its instruction set (assembly language).

A lab report must be created, including the required material The required hand-in for each part of the lab is specified in the lab text.

1. Setup

Run the application program ***altera_upds_setup_vhdl*** to install the Altera Monitor Program; see the document "**Altera Monitor Program Tutorial"**.

2. SOPC builder

Complete the tutorial called ***"Introduction to the Altera SOPC Builder Using VHDL Design"***.

Required hand-in:

- **your design files (make a zipped folder of your project folder containing your design files).**
- **any comments (e.g. problems with the Altera tutorial or your opinion about the tutorial).**

3. Using SDRAM Memory

Complete the tutorial called ***"Using the SDRAM Memory on Altera's DE2-70 Board with VHDL Design"***.

Required hand-in:

- **your design files (make a zipped folder of your project folder containing your design files).**
- **any comments (e.g. problems with the Altera tutorial or your opinion about the tutorial).**