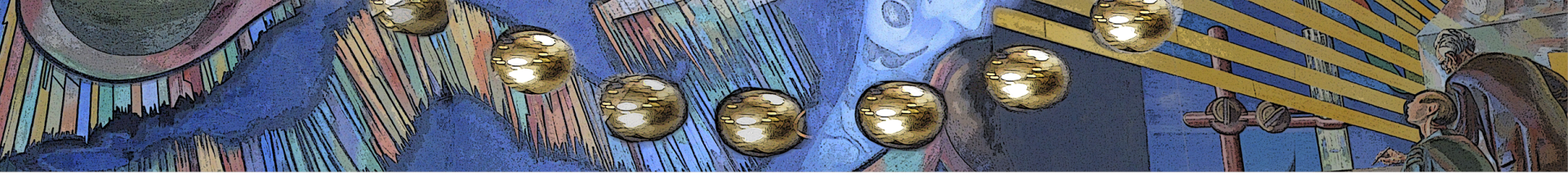
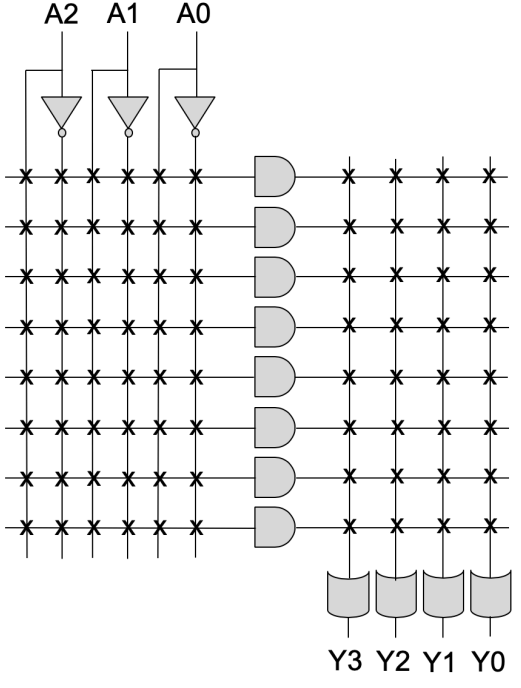


UiO : Department of Physics
University of Oslo

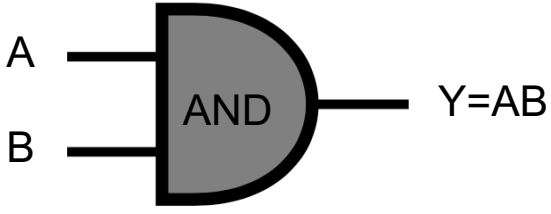
Programmable logic

- Logic gates, multiplexers, flip-flops
- Programmable logic devices
  - PROM, PLA, PAL, GAL, CPLD, FPGA
- Look-up Table (LUT)

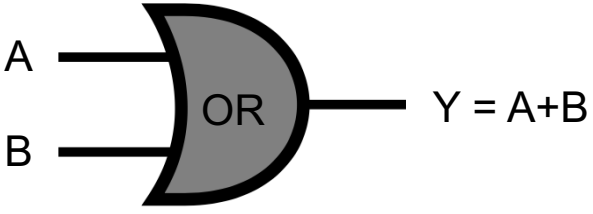


The Basic Logic Gates

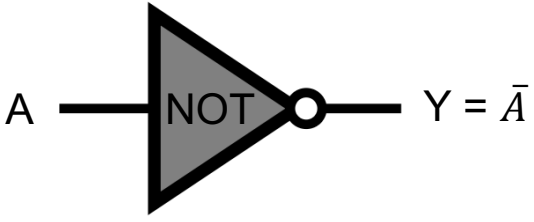
These three gates are logical sufficient to express any boolean operation!



A	B	Y
0	0	**0**
0	1	**0**
1	0	**0**
1	1	**1**



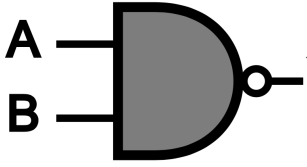
A	B	Y
0	0	**0**
0	1	**1**
1	0	**1**
1	1	**1**



A	Y
0	**1**
1	**0**

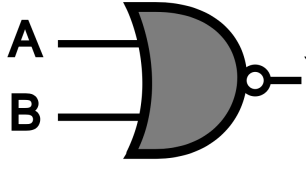
Other Logic gates

NAND



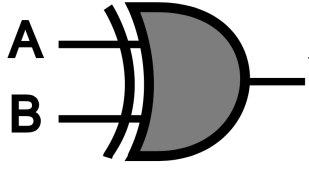
$$= \overline{AB}$$

NOR



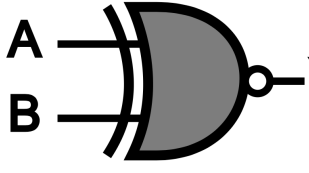
$$= \overline{A + B}$$

XOR



$$= \bar{A}B + A\bar{B} = A \oplus B$$

XNOR



$$= \overline{\bar{A}B + A\bar{B}} = \overline{A \oplus B}$$

Apollo Guidance Computer

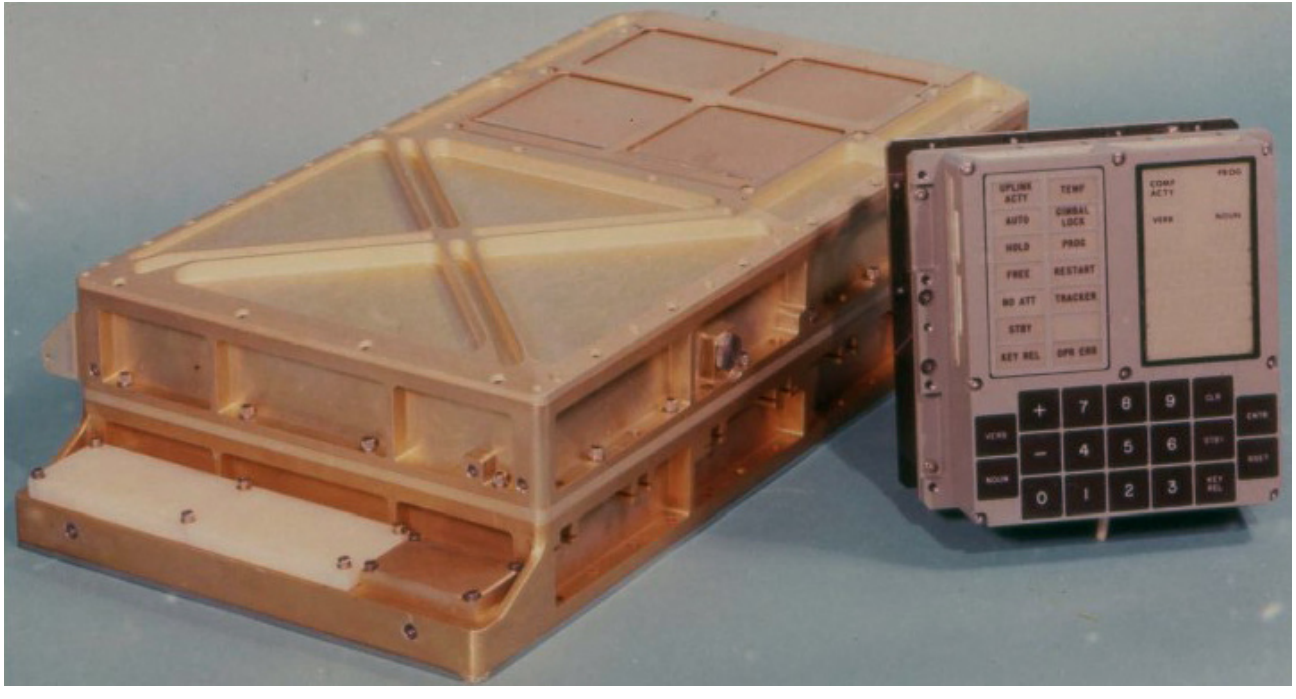
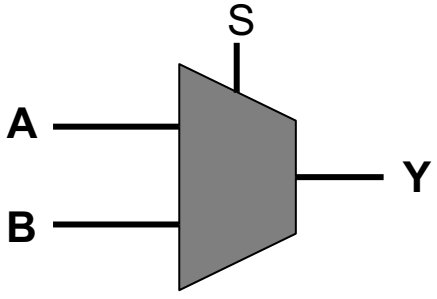


Image credit: NASA

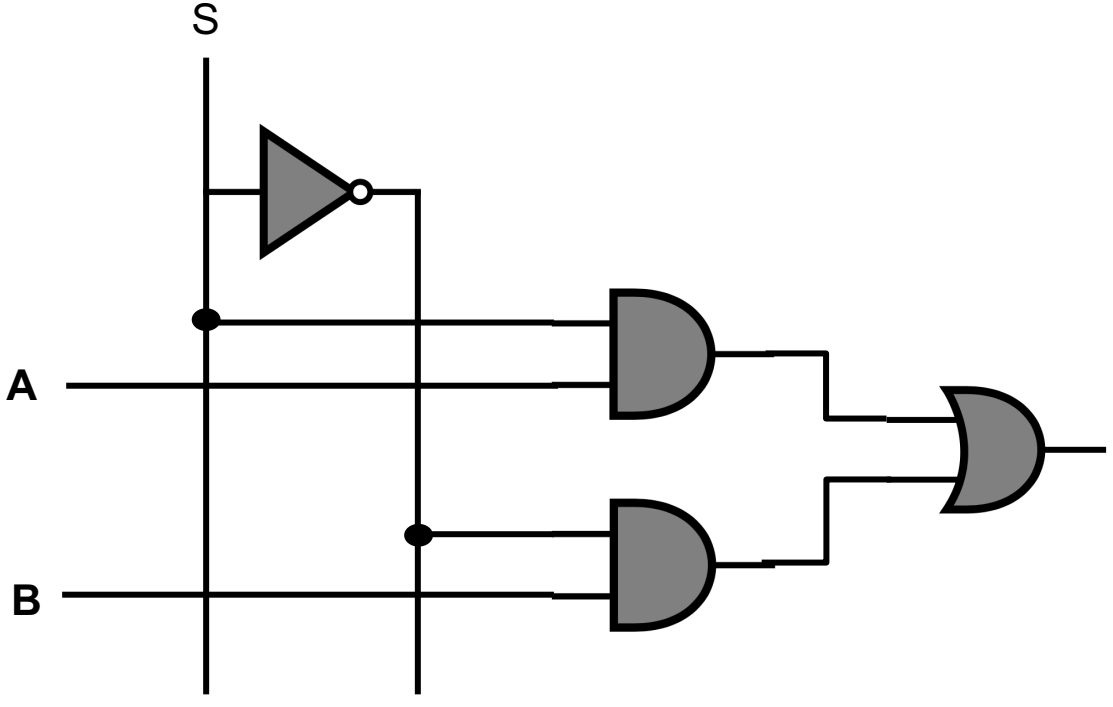
Sources:
http://history.nasa.gov/computers/Ch2-5.html
https://en.wikipedia.org/wiki/Apollo_Guidance_Computer
https://history.nasa.gov/computers/Ch2-5.html
http://www.ibiblio.org/apollo/
https://newatlas.com/apollo-11-guidance-computer/59766/

Multiplexer

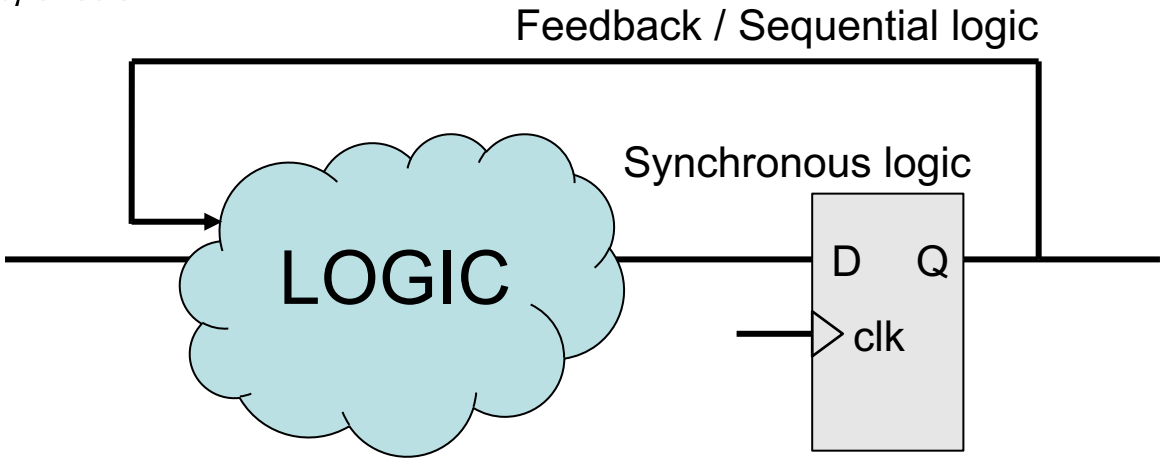


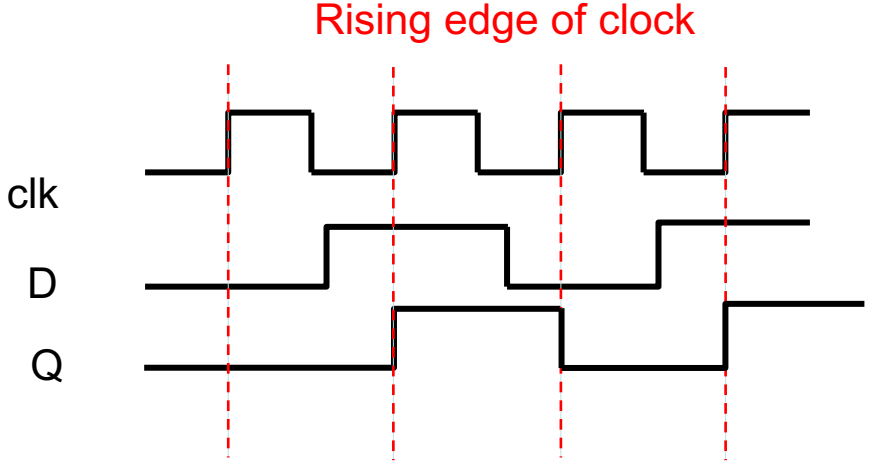
$$Y = AS + B\bar{S}$$

A	B	S	Y
0	0	0	**0**
0	0	1	**0**
0	1	0	**1**
0	1	1	**0**
1	0	0	**0**
1	0	1	**1**
1	1	0	**1**
1	1	1	**1**



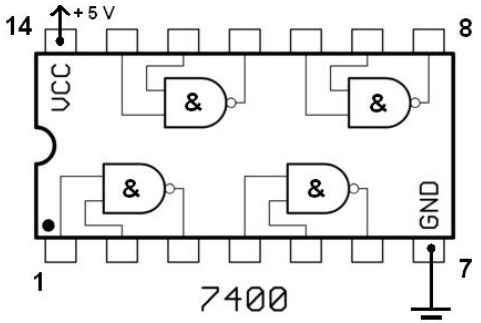
D flip-flop

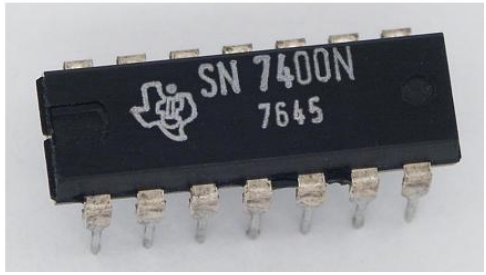

Feedback / Sequential logic
Synchronous logic
LOGIC
D
Q
clk

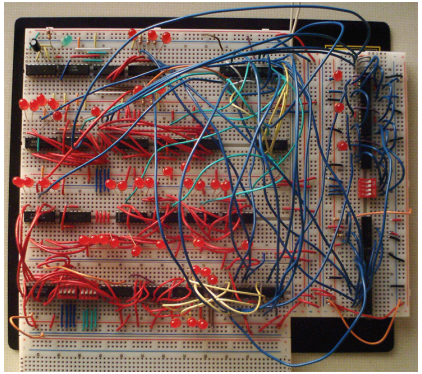

Rising edge of clock
clk
D
Q

Integrated Circuits

- Standard transistor-transistor logic (TTL) integrated circuits (mid 1960s)
- 100's of devices, ready for use, that provide e.g.
  - basic logic gates
  - Flip-flops & memory
  - Counters
  - Arithmetic Logic Units (ALU)
- "Programmability": wires!
- Glue logic in computers and industrial electronics





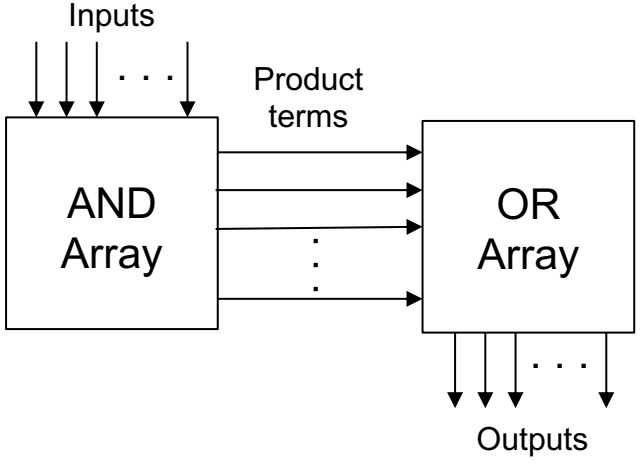


Source: wikipedia

Programmable Logic Devices (PLD)

- PROM: Programmable Read Only Memory
- PLA: Programmable Logic Array
- PAL: Programmable Array Logic

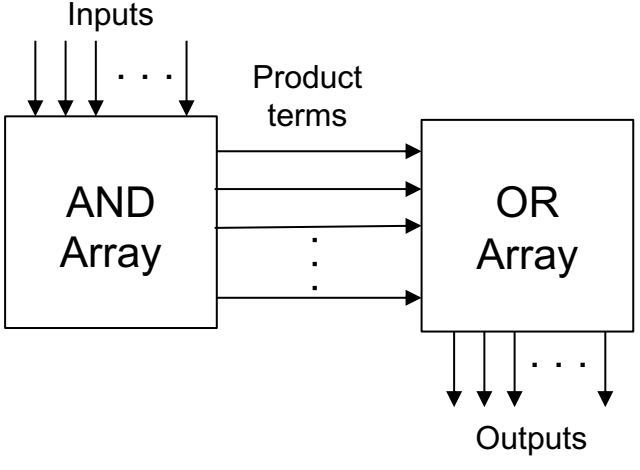
- GAL: Generic Array Logic

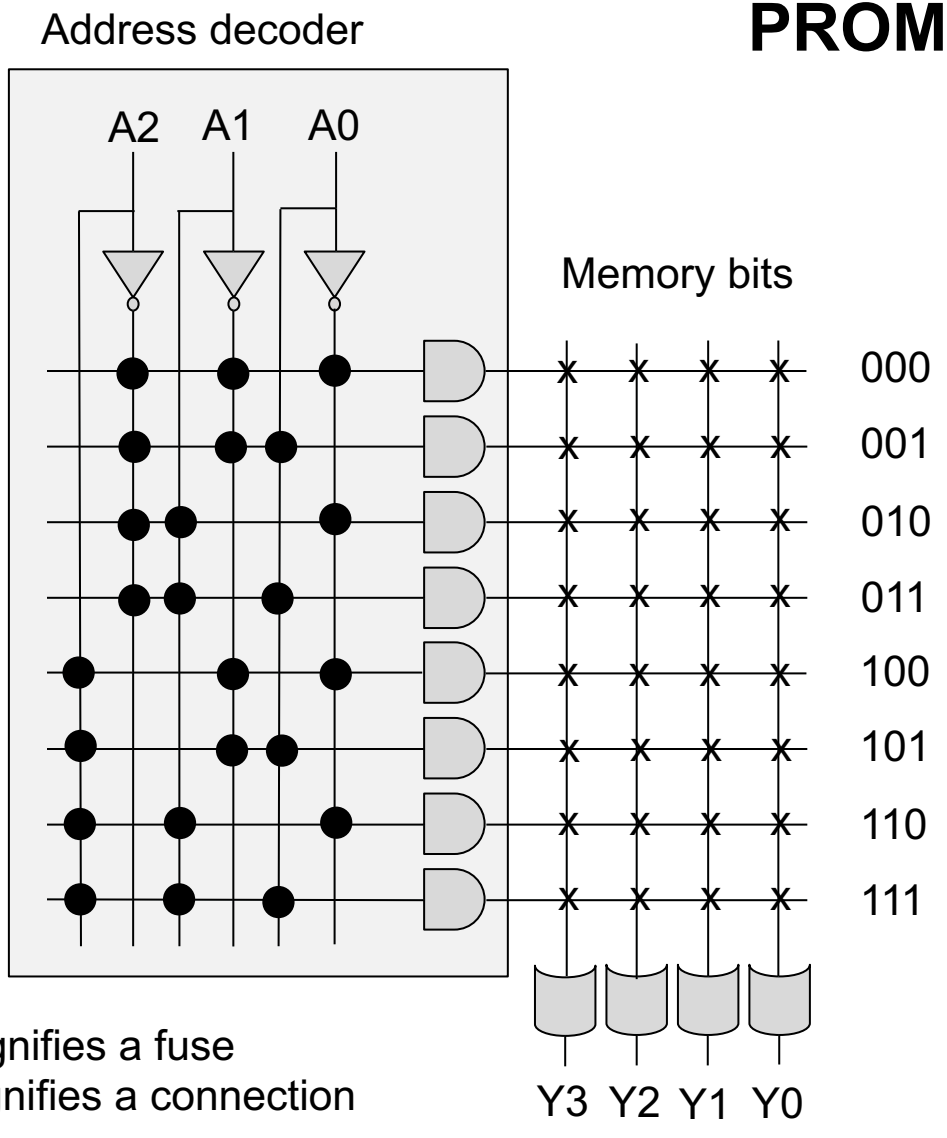


PROM

- First simple PLD

Can be viewed as a **fixed** array of **AND** functions driving a **programmable** array of **OR** functions

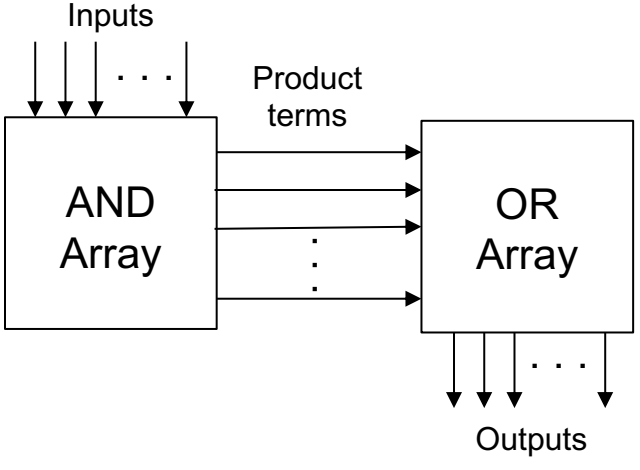


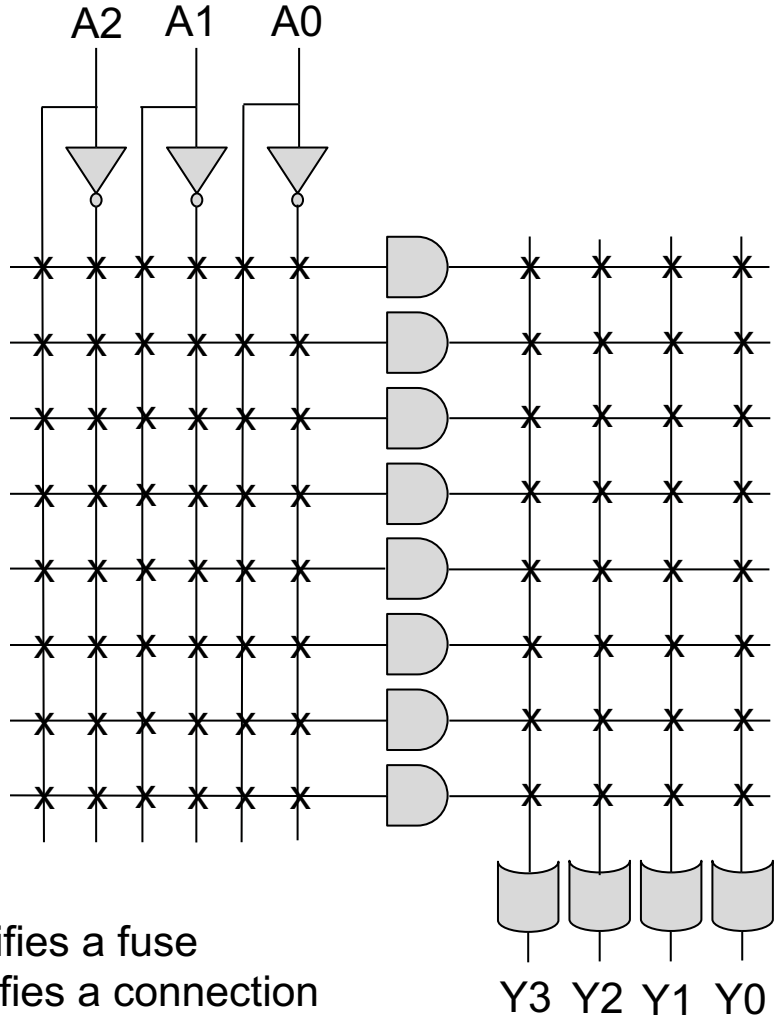


X signifies a fuse
● signifies a connection

Programmable Logic Array (PLA)

- Programmable AND & OR gate array

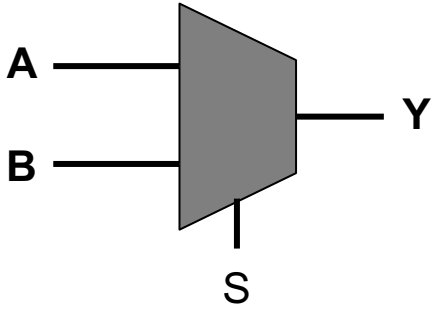




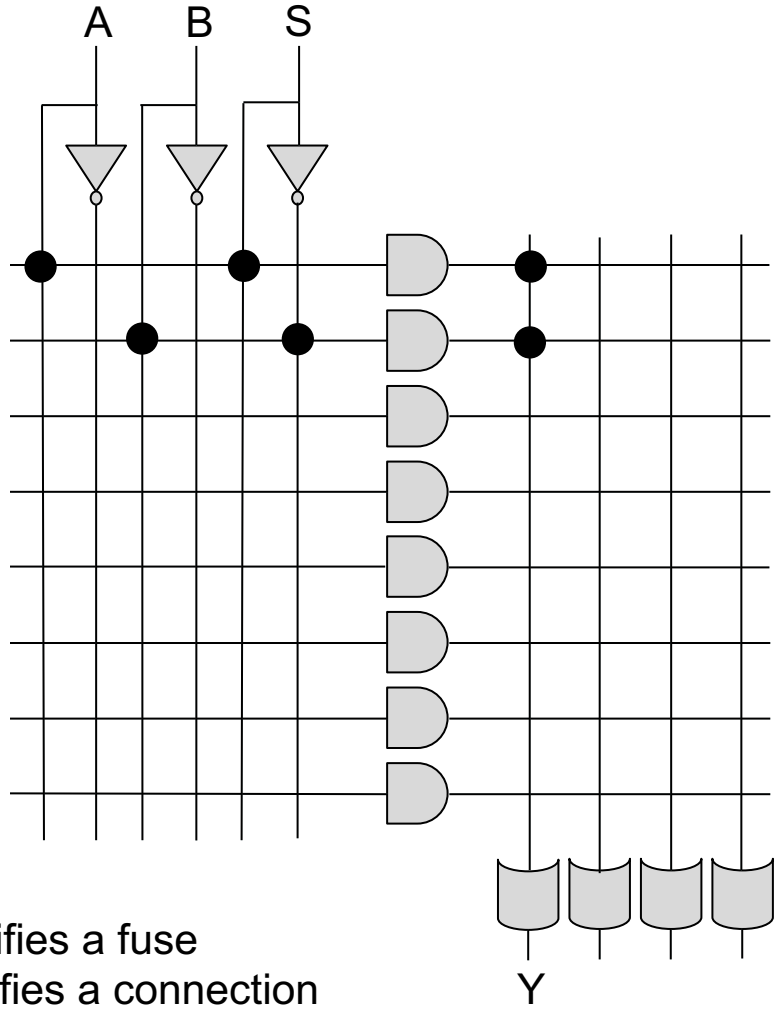
X signifies a fuse
● signifies a connection

Programmable Logic Array (PLA)

- Example of multiplexer



$$Y = AS + B\bar{S}$$



X signifies a fuse
● signifies a connection

Programmable Array Logic (PAL)

- Programmable AND & fixed OR

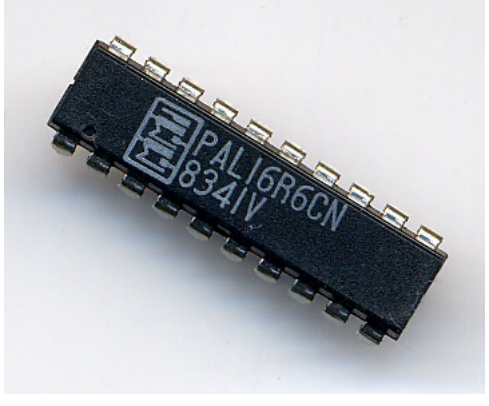
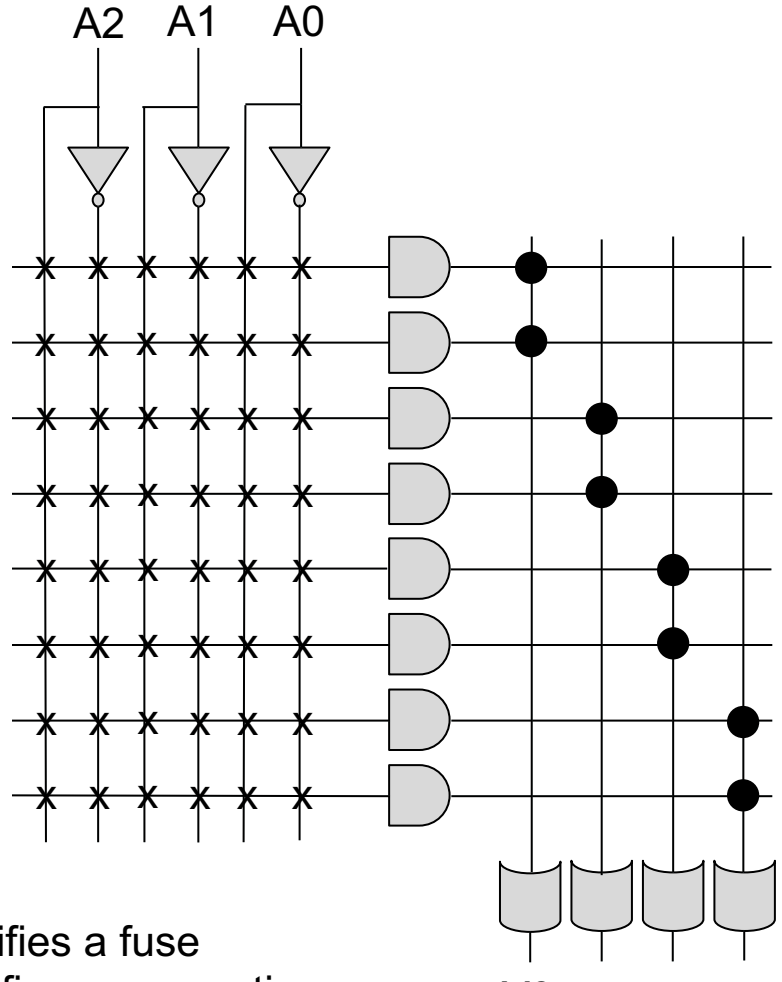
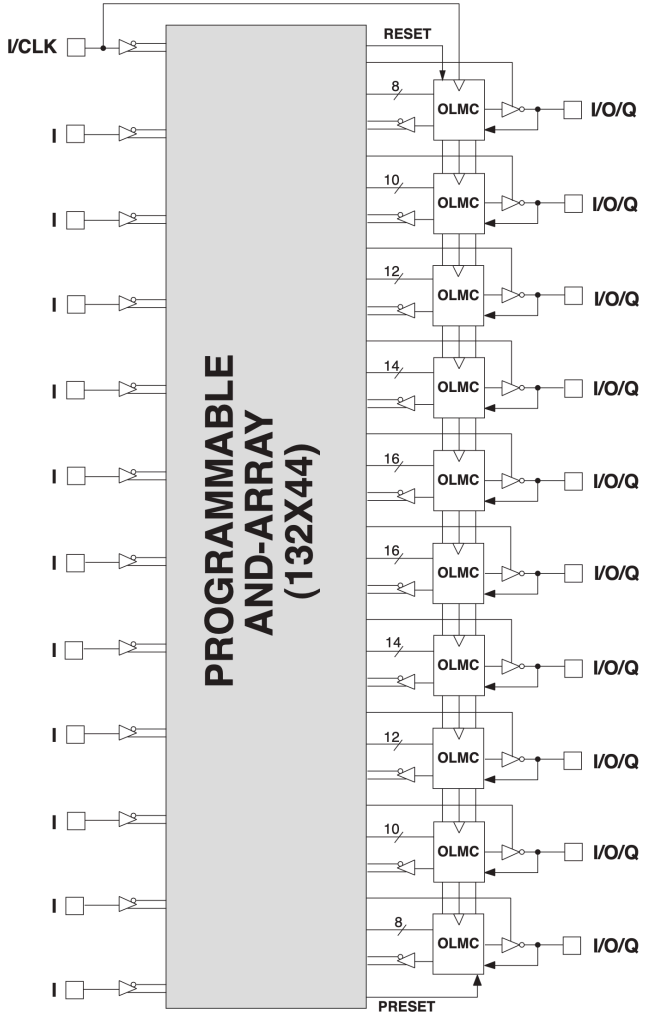


Photo: Michael Holley, 2006.
Accessed from: http://commons.wikimedia.org

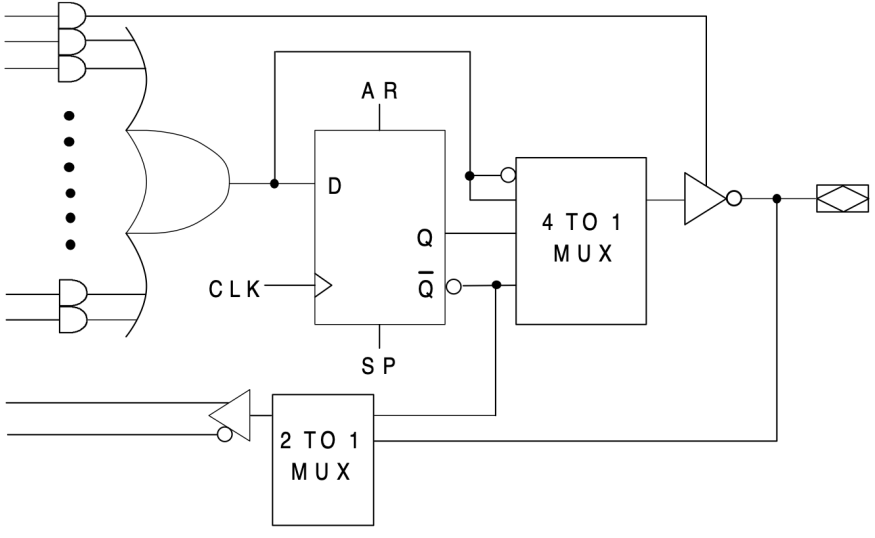


X signifies a fuse
● signifies a connection

Generic Array Logic



- PAL + output macrocell
  - w/ e.g flip-flop & mux



GAL22V10 OUTPUT LOGIC MACROCELL (OLMC)

Source: GAL22V10 datasheet . These devices are discontinued.

Complex PLDs

- More advanced PLDs (end 70s, beg. 80s)
  - CPLD: Complex Programmable Logic Devices (Array of PAL/GAL linked by programmable interconnections)
  - FPGA: Field Programmable Gate Array (Based on concept of Look-Up Table, LUT)

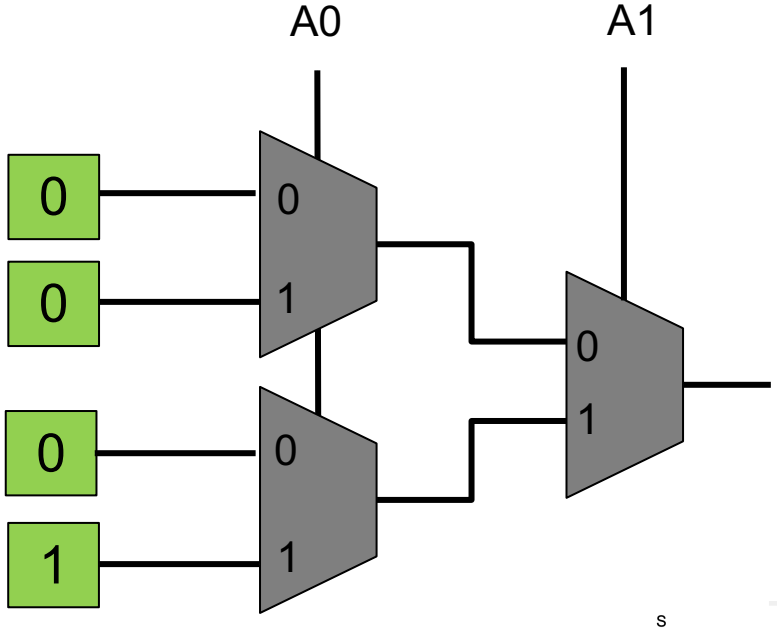
Photo: Altera Corporation

Photo: Xilinx

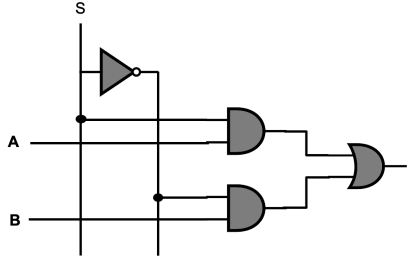
The FPGA was invented by Ross Freeman in 1984.
Inventor's hall of fame: https://www.invent.org/inductees/ross-freeman

Look-Up Table (LUT)

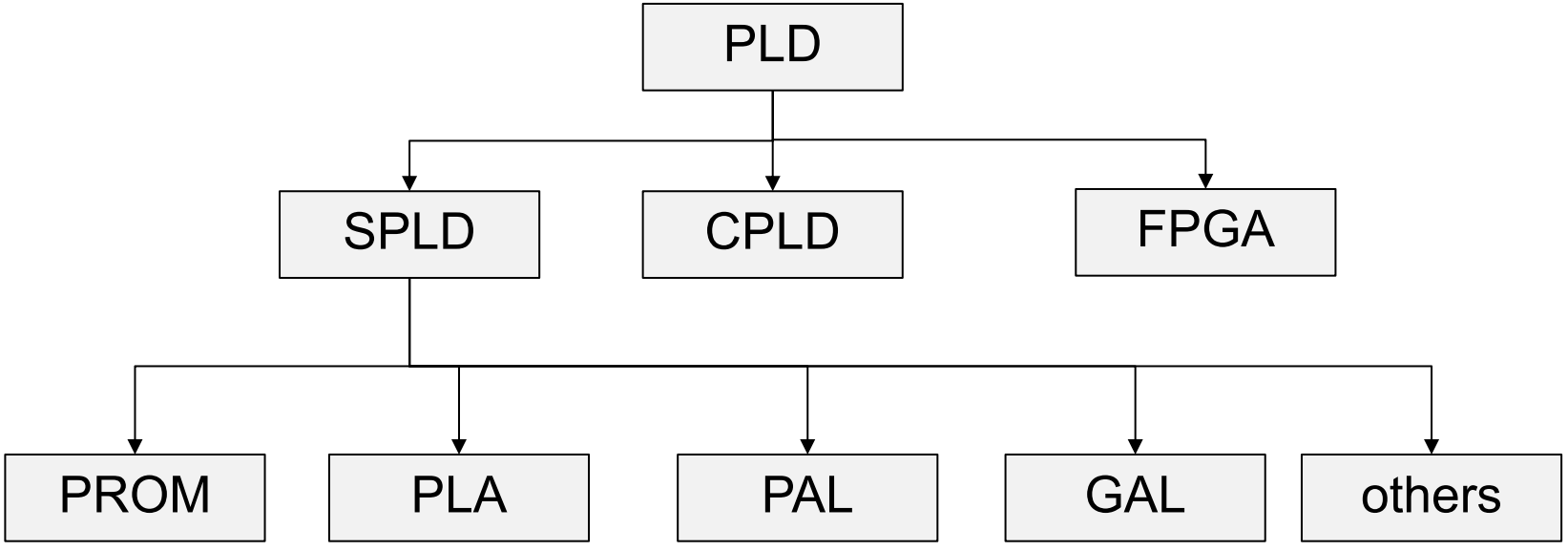
A1	A0	M
0	0	0
0	1	0
1	0	0
1	1	1



Two input AND-gate



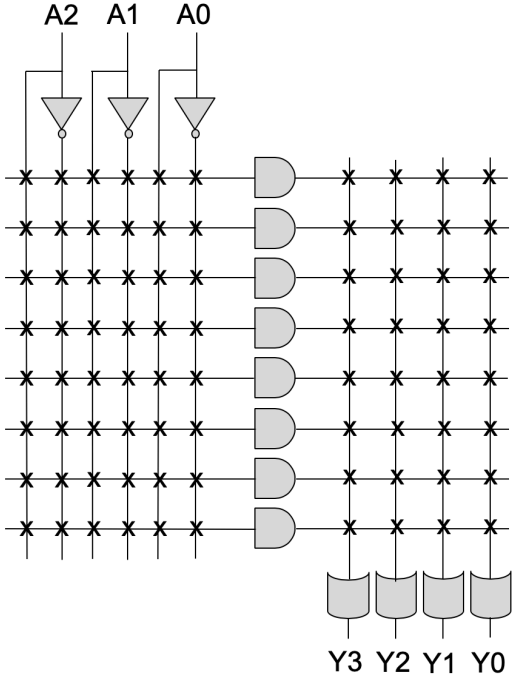
Programmable Logic Devices



Based on figure 16.19 in Clive Maxfield, “Bebop to the Boolean Boogie”, 3rd Edition, Elsiver.

Summary

- Logic gates, multiplexers, flip-flops
- Programmable logic devices
  - PROM, PLA, PAL, GAL, CPLD, FPGA
- Look-up Table (LUT)



Sources of material

- Clive Maxfield, “Who made the first PLD?”, EETimes, 2011. https://www.eetimes.com/who-made-the-first-pld/
- Clive Maxfield, “Bebop to the Boolean Boogie, 3rd Edition. Elsevier. Available online at UB.
- Wikipedia
- And links used elsewhere in this presentation.