CHAPTER 2

TECHNOLOGIES FOR ELECTRONICS - OVERVIEW

2.1 INTRODUCTION

In this chapter we shall give a survey of the mainstream technologies for hardware realisation of electronic systems. Most of the technologies will be presented in more detail in later chapters. Some, such as application specific ICs, are mentioned here for completeness, and will not be treated in detail.

Electronic systems can be implemented in a number of technologies. The optimal choice of technology or combination of technologies in a system is dependent upon a multitude of factors such as:

- Performance specifications: Speed of operation, accuracy, power consumption, weight, size, etc.
- Operating environment - corrosive media, high temperature, etc.
- Required reliability and lifetime of the product
- Production volume
- Need of reparability
- Cost

In each application the factors governing the choice of technologies for the product will have different importance. We illustrated this with some examples in Chapter 1.

2.2 HOLE MOUNTING TECHNOLOGY ON PRINTED WIRING BOARDS

In printed circuit boards (PCBs) with hole mounting, or insertion technology, the components are mounted by insertion through holes in a laminated substrate, the printed wiring board (PWB), and the pins are soldered to the substrate wiring on the backside. This is the traditional way to build electronic circuits, please refer to Figure 2.1.

The components are interconnected on the laminated substrate by conductor lines that are defined in a single layer or multiple layers of copper foil by etching techniques. The components are discrete devices (resistors, capacitors, transistors, switches, connectors, etc.) or integrated circuits. The dual-in-line package (DIP) having a center-to-center pin pitch of 0.1" (2.54 mm) is the most used package for integrated circuits.

Laminated glass/epoxy is the most used substrate material. This is made of several layers of woven fibreglass sheets in a matrix of epoxy. The substrate conductor pattern is single sided on the simplest printed wiring boards. Most used are double layer boards with conductor pattern on each side of the board and interconnections between the sides by metallised holes, through hole plating. Multilayer boards can also be made, by laminating several layers of glass epoxy substrates with copper conductor patterns on each one.

Fig. 2.1: Hole mounting (insertion-) technology printed circuit board.

Most often the components are mounted on the same side of the board - the primary -, or component side - and are soldered on the secondary - or soldering side of the board. The component insertion is most often done by automatic insertion machines.

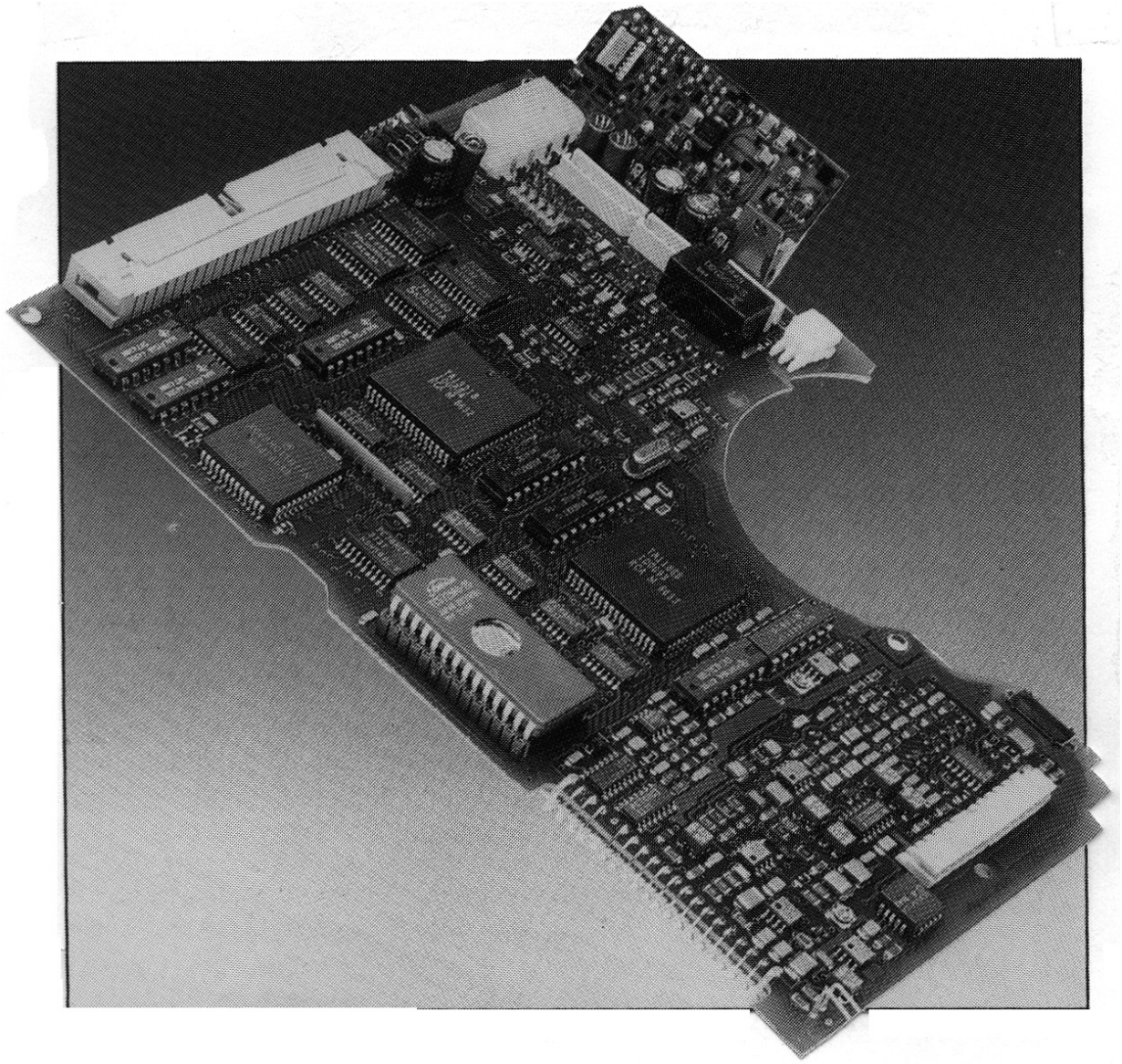


Fig. 2.2: Surface mount technology printed circuit board.

Wave soldering is the dominant soldering method. The printed circuit board with inserted components are passed through a wave of molten solder material. The wave wets the copper soldering pads and the component leads, and solder joints are established as the board leaves the wave. These solder joints make up both electrical contact and mechanical support.

2.3 SURFACE MOUNT TECHNOLOGY (SMT)

In this technology surface mounted devices (SMDs) are soldered to bonding pads on the surface of the substrate, Figure 2.2, in contrast to the hole mounted devices. This technology has been growing very fast since approximately 1980, and is expected to take over the lead from insertion technology as the dominating PCB mount technology, as shown in Figure 2.3. The most striking advantage of surface mount technology compared to insertion technology is the increased packaging density - the devices are smaller and the conductor pattern of the substrate is routed with a finer pitch.

The following are important advantages of surface mount technology:

- Increased packaging density: A surface mount printed circuit boards typically needs only 30 - 70% of the area required for insertion technology. The main reasons for the increased packaging density are more compact devices (Figure 2.4), mounting of devices on both sides of the printed circuit board and the avoidance of area-consuming holes for component insertion.

- Highly automated and cost-effective production: Surface mounted components are well suited for automation, and some of the manufacturing processes of insertion technology are avoided, e.g., sequencing, cutting and bending of component leads - see Chapter 7.

- Improved electrical characteristics: As a consequence of more compact devices and closer placement on the substrate, the parasitic resistances, capacitances and inductances of the interconnection lines are reduced, giving reduced time delays, see Figure 2.5, and noise. Electromagnetic compatibility is also improved, since both electromagnetic radiation and pickup are reduced.

- A potential for higher reliability: For some types of components, we have eliminated one of the material interfaces of the interconnections. Such interconnection interfaces of dissimilar materials are prone to failure. Plated through holes are also susceptible to failure - a reduction of their use also improves reliability.

- Expected lower component costs: Surface mount devices have the potential for being manufactured at lower cost, and this is expected to result in lower prices. (This has not yet fully come into effect - the market mechanisms have so far even resulted in higher prices for some surface mount devices.)

- The most complex circuits of the future will have to be assembled by surface mount technology. This is both because their lead pitch is too low for insertion technology - leaving insufficient room for through holes in the substrate - and because the number of leads is so high that an unacceptable large area would have to be used.

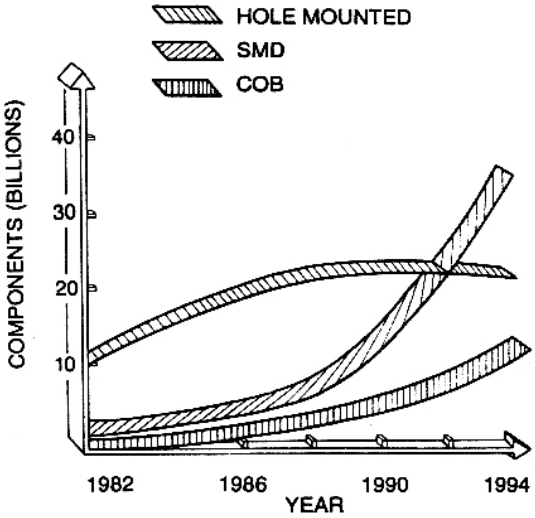
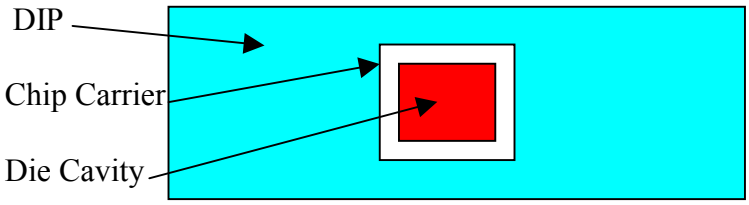


Fig. 2.3: Volumes of different kinds of components used 1980 - 94.



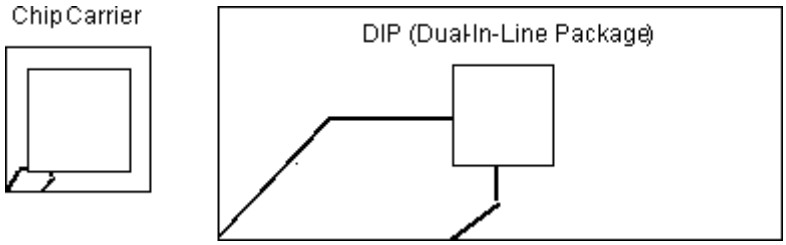
Lead Count	DIP Area : Chip Carrier Area
18	2.7 : 1
24	4.5 : 1
40	5.2 : 1
64	5.6 : 1

Fig. 2.4 a): Size comparison of different package types with approximately the same lead count which can be used for the same size of integrated circuit chip.

There are also some drawbacks with surface mount technology:

- In some cases reduced reliability due to thermal mismatch between substrate and components, because of the shorter component leads, or no leads at all, for surface mount devices.
- Reduced reliability due to higher power dissipation per unit area or volume as a consequence of higher packaging density.
- The components are exposed to high thermal strain during the soldering process in SMT, leading in some cases to reduced reliability.

- More complex test methods need to be implemented, due to smaller components, inaccessible terminals and components on both sides of the board.



Lead Count	Longest Conductor DIP : Longest Conductor Chip Carrier
18	2 : 1
24	4 : 1
40	5 : 1
64	6 : 1

Fig. 2.4 b): The smaller dimensions of surface mount technology packages result in smaller parasitic capacitance and inductance, and therefore improved high frequency performance. Both electromagnetic radiation and electromagnetic susceptibility are also reduced.

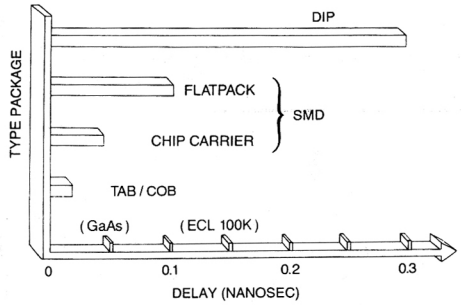


Fig. 2.5: Typical time delay for different component package types, and for Tape Automated Bonding (TAB)/wirebonding of naked chips. Shown on the abscissa: typical time delay on the semiconductor chip with Si ECL (Emitter Coupled Logic) with 100 kgates and GaAs technologies.

Usually, components are placed on both sides of the board when using surface mount technology. This approximately doubles the component density for the whole printed circuit board, when compared to single-sided component placement. However, this calls for a substantially more complex production process. The components on the secondary side can be wave soldered, just like insertion technology processing, but the SMDs must be attached to the board with adhesive beforehand, to stay on the board during soldering, at which time they are hanging underneath the board.

Soldering of the SMDs on the primary side is usually done with reflow soldering. This process is based upon screen printing of solder paste on the solder pads of the board before component placement. This is an adaptation of the general screen printing process used for graphical work of art, etc. The solder paste is squeezed through openings of the printing screen with a "squeegee", see Chapter 8. Next, the components are placed with the leads on the corresponding

solder pads. Thereafter, the assembly is heated until the solder paste melts and forms soldered joints between the component leads and the bonding pads on the substrate.

The supply of SMDs is still incomplete, making it necessary to use of both SMDs and insertion mounted devices - "mixed technology". Using this process, the hole mounted components are wave soldered in the same process step that is used to solder the SMDs on the secondary side of the board.

Both leaded and unleaded SMDs are available. Standard, small-size resistors and capacitors usually have leadless ceramic bodies with solder terminals on both ends. Plastic packaged active devices are normally leaded. Hermetically sealed integrated circuits are specified in some high-end applications, and in these cases ceramic packages are used. The ordinary ceramic packages are leadless, giving rise to mechanical stresses, because the normal glass/epoxy wiring board has a much higher thermal coefficient of expansion (TCE) than the ceramic. This can result in catastrophic failure, after the soldering process, or fatigue stressing of the solder joints after long time in operation.

One way to avoid susceptibility to such strains when using large ceramic packages is to use other types of substrate materials than the normal glass/epoxy laminate.

Surface mount technology is now in widespread use as an established technology in the electronics industry.

2.4 CHIP ON BOARD

Naked silicon chips can be mounted directly on the PWBs or other types of substrates, without encapsulation. This technology is called "Chip on board" (COB) The three most used electrical connection methods between the chip and substrate are visualised in Figure 2.6.

Wire bonding is done in the same way as for chip connection in packages: A gold or aluminium wire is bonded between each bonding pad of the chip and the corresponding pad on the substrate. After mounting and bonding, process steps to establish corrosion protection and mechanical protection of the chip are needed, either by hermetic sealing of the assembled board, or locally by "glob top" sealing with a droplet of sealing material, e.g., epoxy. Wire bonding of bare chips is used in hybrids, most often with a ceramic substrate. Chip on board is also used with glass/epoxy laminates in some consumer applications (pocket calculators, watches, smart cards, etc.), and occasionally in professional applications.

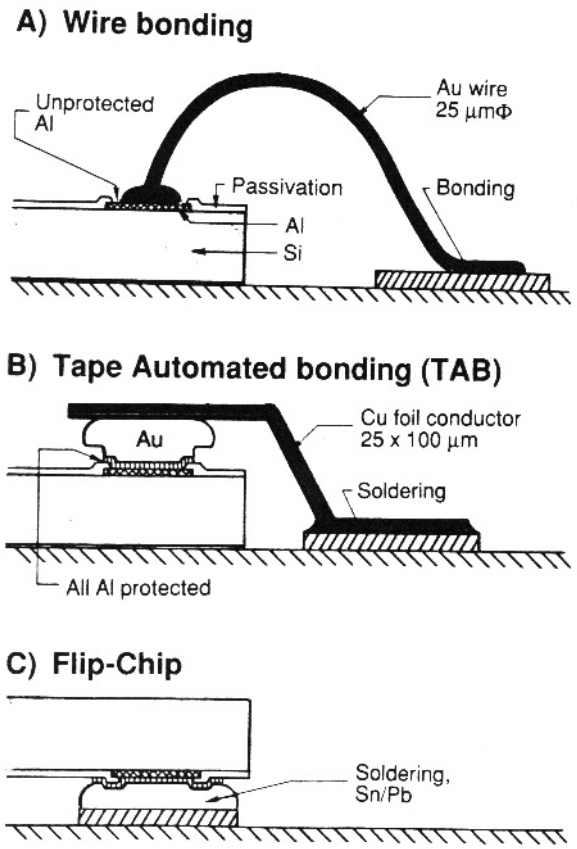


Fig. 2.6: Chip connection by wire bonding, tape automated bonding (TAB) and flip chip, schematically.
- Wire bonding (Chip and wire)
- Tape Automated Bonding (TAB)
- Flip chip.

Tape Automated Bonding (TAB) has a conductor pattern of copper as interconnections between chip and substrate. The conductor pattern is pre-processed from a continuous copper tape on a dielectric carrier film. It is first bonded to gold "bumps" on the silicon chip (inner lead bonding). Mounting of the chip on the substrate is done after cutting off the copper fingers from the tape just outside the chip area. The leads are soldered to the substrate with a specialised tool called thermode ("Impulse soldering") TAB is in widespread use in liquid crystal displays, electronic watches and other high volume consumer products. Other TAB applications are VLSI circuits with a high lead count and other high-end needs.

Flip chip is done by mounting the chip upside down on the substrate, after having deposited solder bumps on all interconnection pads of the chip. The chip is soldered directly onto the substrate, calling for close thermal matching of the chip and substrate. Flip chip technology gives the highest packaging density of the different interconnection methods, It gives excellent electrical characteristics and high reliability when properly used, but it is a very demanding technology both to establish and operate. Initial costs are high, favouring high-volume or high-end applications.

2.5 THICK FILM HYBRID TECHNOLOGY

2.5.1 High temperature thick film hybrid technology

In hybrid technology, chips are interconnected on a substrate with the capability of including passive components such as resistors, capacitors and insulators as an integrated part of the substrate. The hybrid technologies have packaging density between integrated circuit technology and printed circuit board technology.

High temperature thick film hybrid technology generally uses sintered Al_2O_3 (alumina, ceramic aluminium oxide) as the substrate material. Conductors, resistors and insulators are made as thin layers, deposited by screen printing. Use of thick film pastes with low resistivity gives conductors, while pastes with a higher resistivity give resistors. Insulators are made with dielectric pastes. An example is shown in Figure 2.7

Capacitors are screen printed in a three-stage process. First, a conductive layer is printed as the bottom electrode. Thereafter a thin layer of dielectric material is printed, and finally a second conductive layer as the top electrode.

The thick film pastes for conductors and resistors are made up of conductive particles (metals or metal oxides) in a matrix of glass particles, organic filler materials and solvents. After each printing step, the hybrid substrate is dried and heat treated at a high temperature (700 - 900°C) to remove the solvent and the organic vehicles by evaporation. Mean while the glass melts to make up a homogenous mixture of conductive filler in a glass matrix.

Surface mount technology devices are solder to the thick film substrate by reflow soldering. Bare silicon chips can also be used. They are most often mounted with adhesive and electric contact to the substrate is provided by wire bonding.

Features of the high temperature thick film hybrid technology are high reliability and stability of both components and interconnections. The packaging density is also high, with the capability of multilayer conductor patterns and printed components integrated in the substrate area underneath the mounted components.

One of the drawbacks is a relatively high cost. The ceramic substrates are much more expensive than the typical glass/epoxy laminates used for printed circuit boards. Alumina is a brittle material prone to breakage. There may also be a slight warpage due to mechanical stress. Therefore the maximum substrate area is normally limited to 100 x 150 mm or less. Some of the thick film pastes contain precious metals, making them expensive.

Electronics circuits made by high temperature thick film hybrid technology constitute approximately 5% of all electronics when measured in value. Thick

film hybrid manufacturers are typically small and medium size enterprises, serving first the local markets where closeness to the customer is a competitive edge.

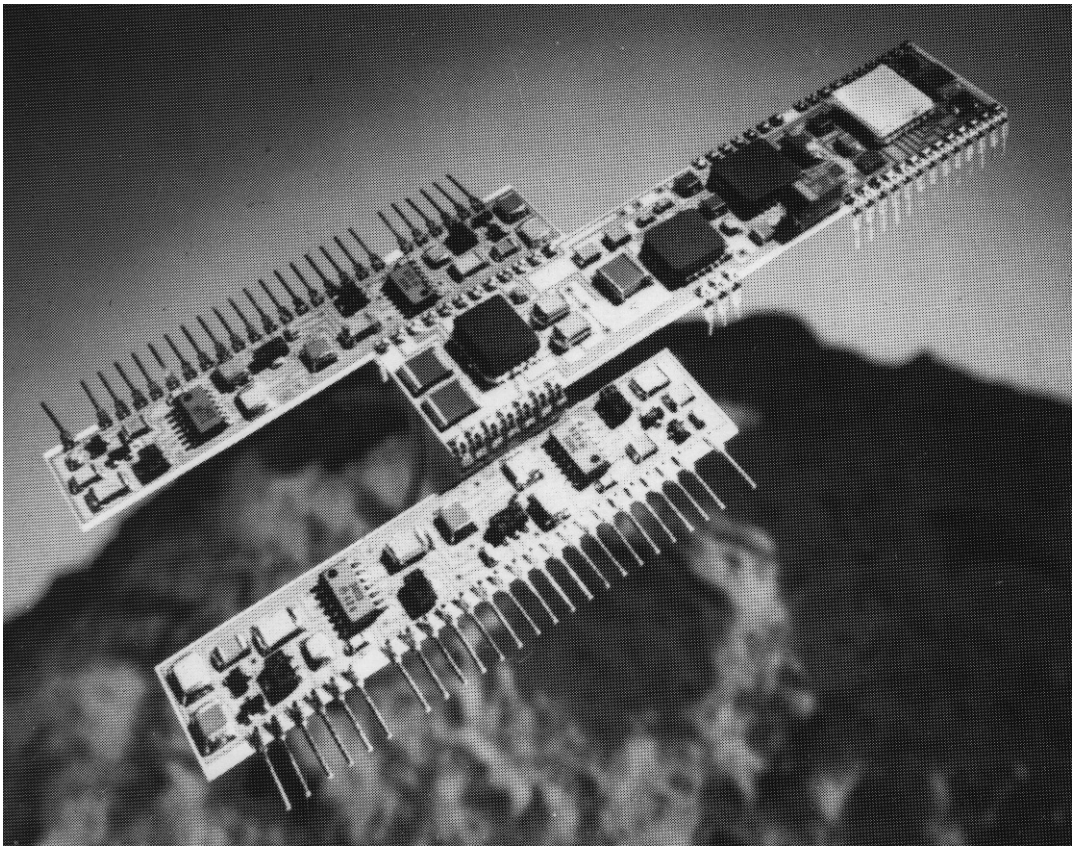


Fig. 2.7: Thick film hybrid circuits.

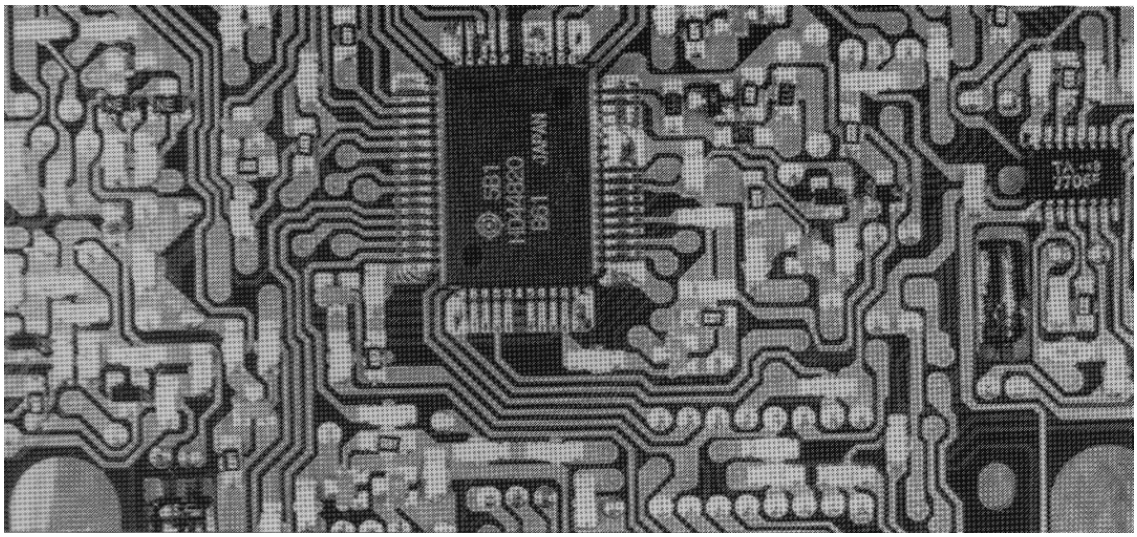


Fig. 2.8: Polymer thick film hybrid circuit.

2.5.2 Polymer thick film hybrid technology

The relatively high cost of the thick film hybrid technology is related to the high temperature processing temperature. The high temperature makes it necessary to use costly ceramic substrates and pastes with precious metals. The high processing temperatures are needed to melt the glass particles in the paste into the matrix of the thick film.

As a way to cut costs, alternative thick film pastes are developed making use of organic, polymer materials instead of glass as matrix material. Such "polymer thick film" pastes can be printed on ordinary glass/epoxy laminates and cured at 150-200 °C. The polymer thick film technology (PTF) can therefore be combined with traditional printed circuit board technology, Figure 2.8. The conducting particles in the pastes are silver, copper or carbon.

PTF has inferior long term reliability compared to traditional hybrid technology and printed circuit board technology, and relatively poor long term stability of the printed resistors. The PTF technology is in widespread use in Japan, especially in consumer applications. So far the PTF technology has not gained widespread use in the western industrialised world.

2.6 THIN FILM HYBRID TECHNOLOGY

In thin film hybrid technology, the conductors, resistors and capacitors are also processed on the substrate, like in thick film technology, but the materials used and deposition techniques are different. The layers are generally well below 1 μm in thickness - this explains the term "thin film". Examples of thin film hybrids are shown in Figure 2.9.

Glass and alumina are the most common substrate materials. Conductors are made by deposition of a thin film of metal, with a typical thickness of 1 μm, most often gold or aluminium. This is done by evaporation or sputtering deposition. These methods are presented in Chapter 3.

The conductor pattern is defined by photolithography, see Chapter 3, and the metal is etched off, using photoresist as etch mask.

The resistors are made in a similar way, using mostly thin film layers of NiCr alloys or Ta_2N.

Insulating layers and dielectric layers for capacitors can be Si_3N_4, SiO_2, etc. They are made by different processes described in Chapter 3.

Traditional thin film circuits are made with one layer of conductor lines and one resistor layer. Recently, the more complicated multilayer thin film hybrid technology has increased in use. With multilayer technology, higher packaging density and higher complexity can be achieved. Electrical characteristics can also be improved by adding separate ground and power supply conductor layers, giving better shielding and possibility to obtain controlled characteristic impedance in high frequency applications, etc.

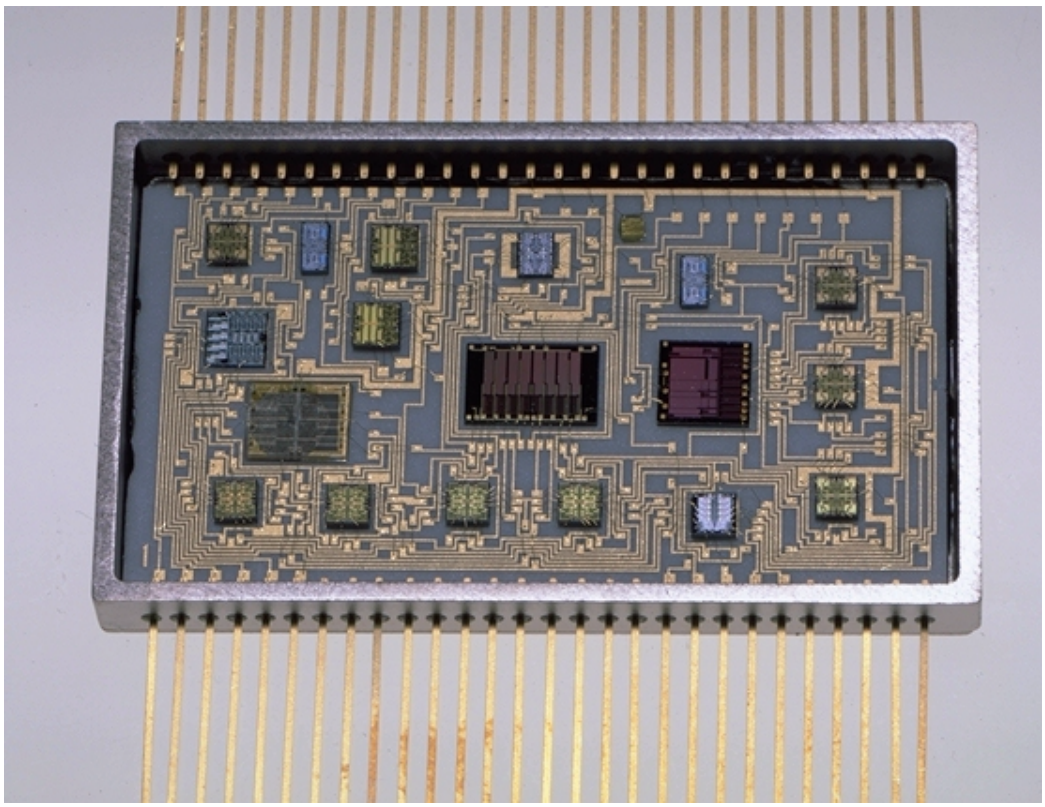


Fig. 2.9: A thin film hybrid circuit.

Most thin film hybrid circuits are using transistors and integrated circuits in the form of bare silicon chips, which are mounted with adhesive and connected by wire bonding. Usually, the complete circuit is packaged in a hermetic metal- or ceramic package.

Thin film technology offers a substantial increase in packaging density compared to thick film hybrid technology. It has excellent electrical characteristics and high reliability. Thin film technology is a specialised technology with relatively few suppliers.

2.7 MULTICHIP MODULES

The continuing increase in maximum operating speed, number of in- and outputs and power dissipation of the semiconductor IC chips requires higher performance in the next level of interconnection. The following needs are of particular importance:

- Fine-line conductor dimensions with short conductor lengths
- Controlled characteristic impedance

- Low thermal resistance to heat sink
- Matched thermal expansion coefficients,
- Etc.

Some of these features can be met by using advanced multilayer printed circuit boards made of advanced materials with special processing. Nevertheless, printed circuit board technology has inherently limited performance. As an example, narrow conductors are difficult to make, and 100 μm a typical minimum line width for printed circuit boards, compared to less than 1 μm for silicon integrated circuits. Conventional thin film, and the most advanced thick film technologies have minimum line widths smaller than that of printed circuit boards, but are still far from the line widths of integrated circuits.

The maximum achievable interconnection density may be defined as the maximum total line length per unit area when using minimum line width and line spacing times the no. of conductor layers, - e.g., cm line length per cm^2 area. There is a "technology gap" in interconnection density between the conventional substrate technologies and semiconductor technology. This is shown in Figure 2.10.

New technologies are emerging to give substrates with increased interconnection density as well as higher speed and improved thermal characteristics for high performance system modules: Multichip module (MCM) technology [2.9]. A multichip module is a structure consisting of two ore more integrated circuit chips electrically connected to a common circuit base and interconnected by conductors in that base.

The main driving forces behind MCMs are the rapid developments in semiconductor technology that make ever more advanced electronic systems possible. Some important trends for the systems development are:

- Smaller critical dimensions, i.e. line widths and distances on the IC and module/PCB.
- Increasing packaging density, i.e. more and more electric functions are possible to implement in a given area or volume.
- Increasing maximum operating speed. (frequency/bit rate)
- Increasing power dissipated per unit area and -volume.
- Increased possibility to realise complex circuit functions with standard hardware in combination with programming software.
- Ever lower price per electrical function.

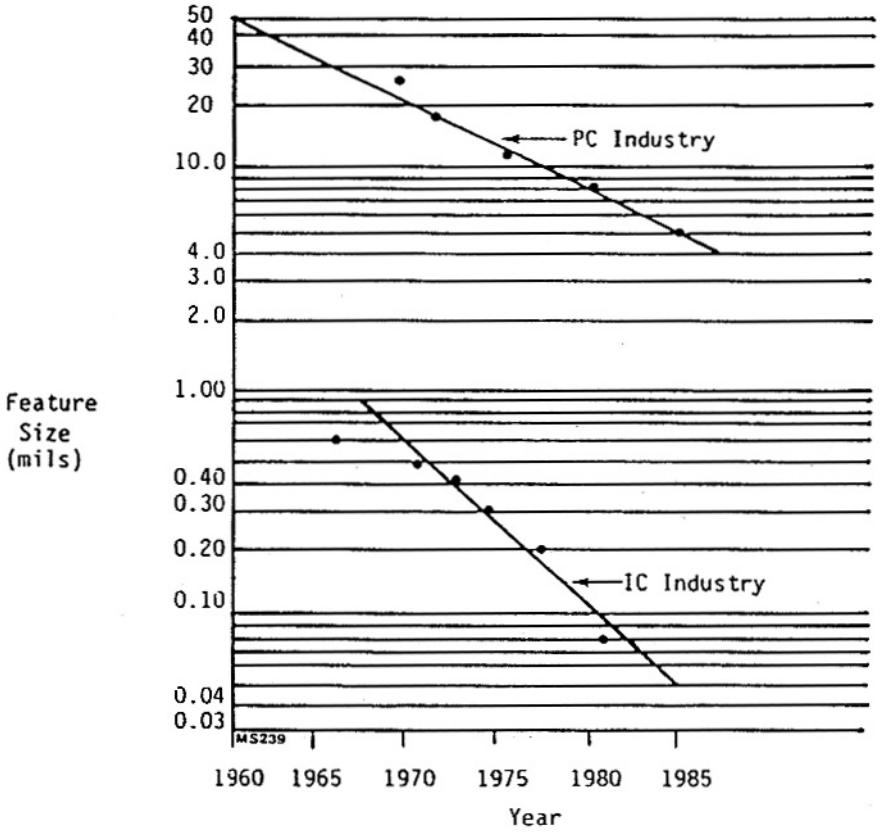


Fig. 2.10: Trends in leading edge fine line pitches for printed circuit boards and integrated circuits from 1965 to 1985 show a widening gap. [2.5].

The MCM technologies make up a family of substrate technologies, which can be divided into the following 4 main groups with the following definitions:

1) MCM-Z (Z for Zero): Modules using no substrates with direct chip-to-chip interconnection and direct chip-to-package connection.
2) MCM-L (L for Laminate): Modules using fine-lined printed wiring board technologies to form the copper conductors on plastic laminate-based dielectrics.
3) MCM -C (C for Ceramic): Modules constructed on cofired ceramic substrates using thick film (screen printing) technologies to form the conductor patterns. ("Cofired" means that the conductors and the ceramic are all heated in an oven at one time) In addition, we include here modules made by thick film printing of conductor pattern on prefired bulk ceramic substrates with no previous conductor pattern.
4) MCM-D (D for Deposited) are modules whose interconnections are formed by the thin film deposition of metals on deposited dielectrics, which may be polymers or inorganic dielectrics. Ceramic, glass, silicon or metal are used as base substrate. The denotion MCM-S is sometimes used for MCM-D on silicon substrate.

Typical achievable interconnection densities for these as well as some other technologies are shown in Figure 2.11. Typical cost per unit substrate area is also included.

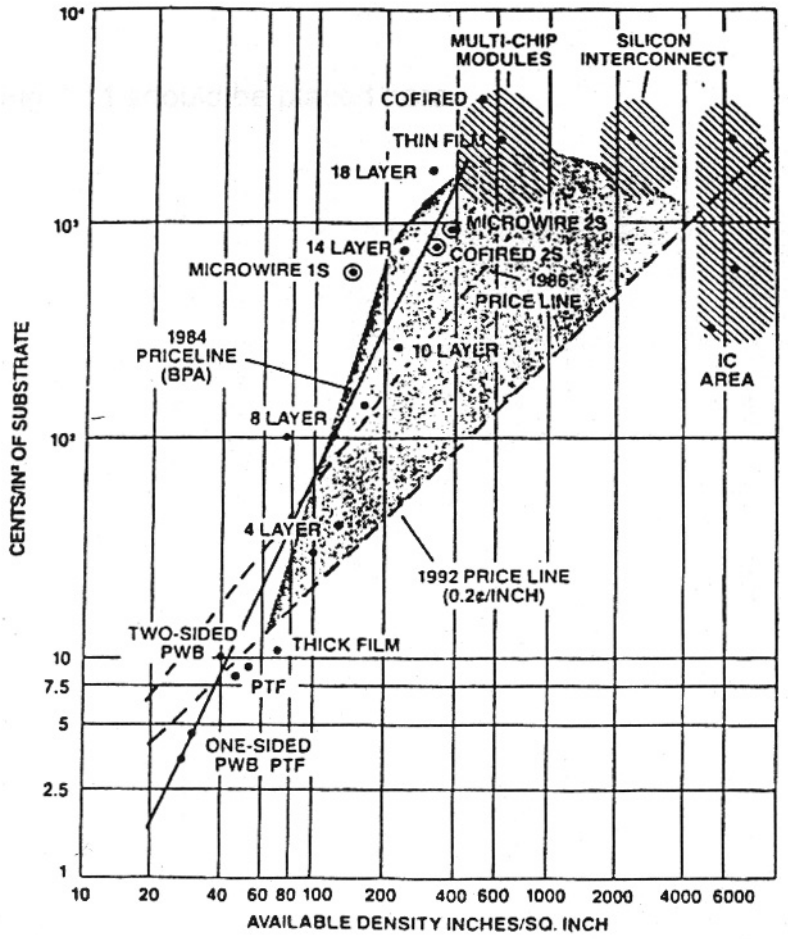


Fig. 2.11: Interconnection density (inches of conductive path length per square inch area) for different kinds of technology. The Y-axis gives the typical price in cents per square inches area for each technology. [2.6]. (The price in the figure can be misinterpreted because the number of circuit functions per area is also strongly dependent of the interconnection density. Therefore, for a given, complex circuit function, the technologies towards the right side usually are the most competitive.)

2.7.1 Multilayer ceramic modules

Multilayer ceramic modules are made by stacking up many layers of unsintered ceramic sheets - "green tape" - with screen printed conductor pattern on one side and metallised via holes as interconnections to the next layer. All the layers are sintered together at high temperature, making up a compact multichip substrate with very good electrical and thermal characteristics.

Packaged surface mount devices or bare IC chips are mounted on top of the substrate, or in recesses - "cavities" - which are made during the ceramic processing, Figure 2.12. This technology is developed from the technology that is used to make ceramic chip carrier packages or multilayer ceramic capacitors.

At present, there is a limited availability of custom designed multilayer ceramic modules. World-wide there are only a few vendors. The technology is expected to get more widespread use when lower temperature materials have been developed, which are compatible with some of the materials and processes used

in thick film hybrid technology. The technology is described in more detail in Chapter 8.

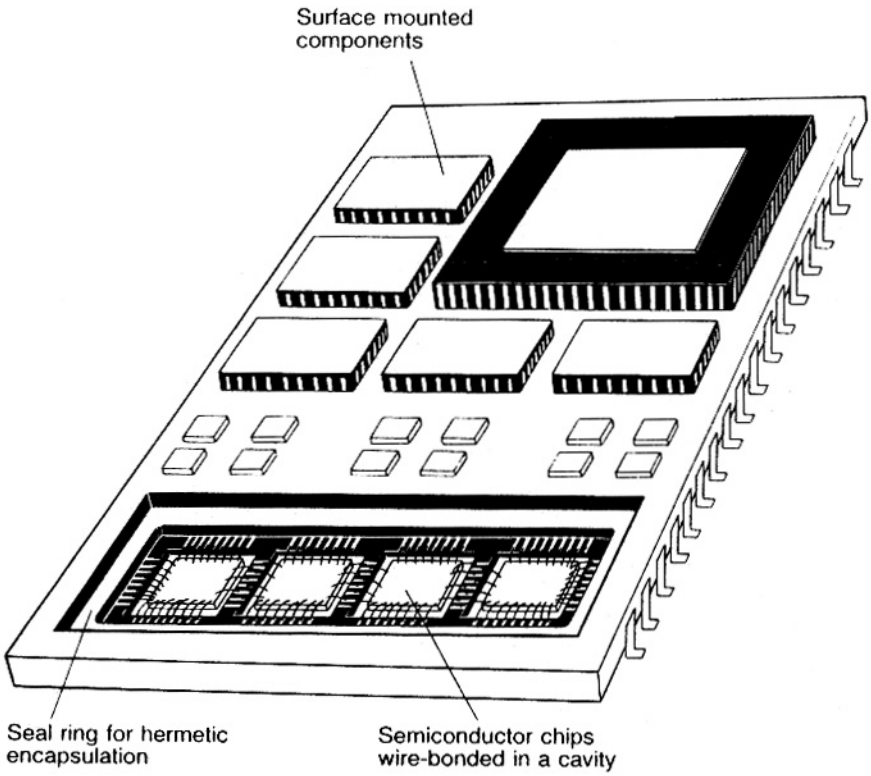


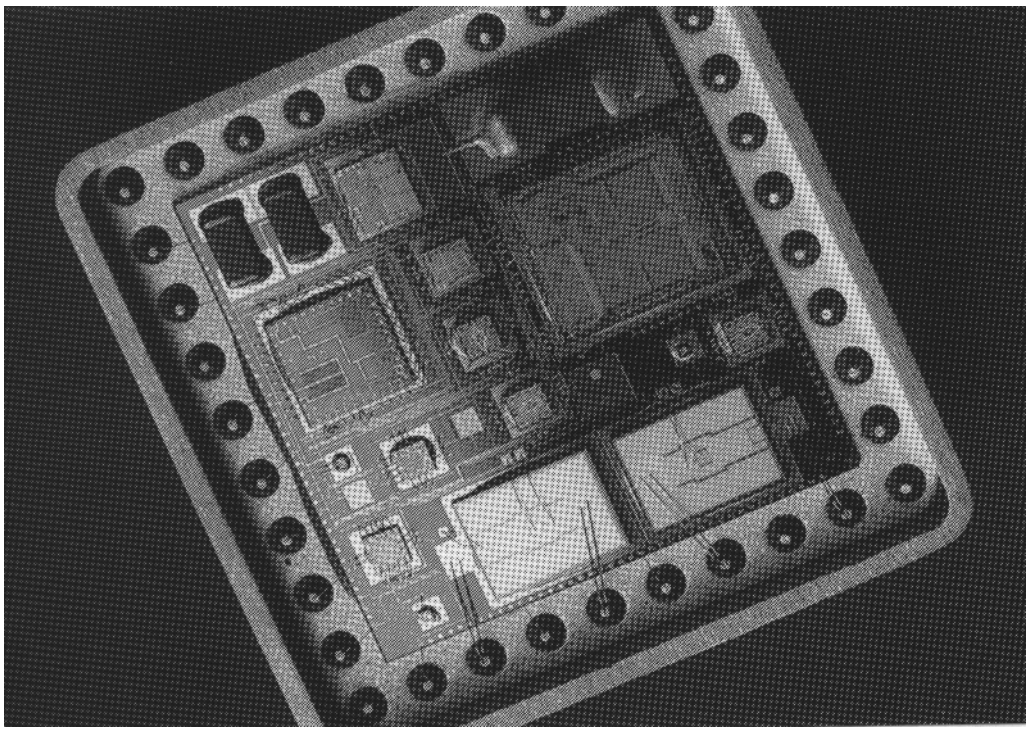
Fig. 2.12: With the multilayer ceramic module it is possible to combine hermetically sealed, wirebonded Si chips in a cavity with lid, soldered, surface mounted packaged chips, and soldered passive components.

2.7.2 Multilayer thin film modules, silicon as a substrate

Silicon multichip modules are using silicon as the substrate material for multilayer thin film modules, see Figure 2.13. Dielectric and conductive layers are deposited on top of the silicon wafer using straightforward or modified thin film technology. Polyimide, that is spin coated, is the most used dielectric. For more details, please refer to Chapter 8. The IC chips are interconnected by wire bonding, tape automated bonding (TAB) or flip chip soldering.

Distinct features of this technology are perfect matching of thermal expansion coefficients of the substrate and the silicon chips, high thermal conductivity, and an industrial infrastructure already established to serve the silicon integrated circuit market. Minimum feature sizes are typically 10 - 20 μm.

The silicon multichip module technology is still immature, with a low market penetration. However, there is a growing R&D activity world-wide giving a technology push. Many successful products are already using the technology, e.g., the VAX 9000 computer from Digital.



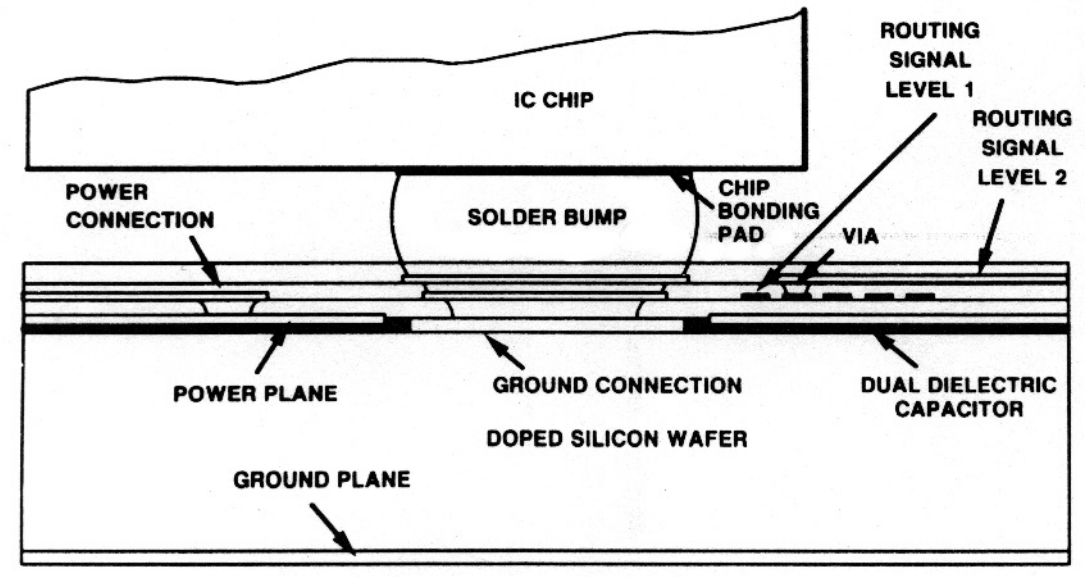


Fig. 2.13: A silicon multichip module. The top figure shows a complete module with wirebonded Si chips and glued passive components, in a hermetic metal package. The bottom figure shows schematically a Si substrate with multilayer thin film and a Si chip mounted with flip chip technology.

Ceramic can be used as an alternative substrate material for multilayer thin film technology, giving approximately the same features.

Multilayer thin film and multilayer ceramic technologies can be combined, implementing each part of the system in the most suitable technology, e.g., silicon multichip technology for the most critical parts calling for high

interconnection density and high speed operation, while the less critical parts are implemented in multilayer ceramic technology.

2.7.3 Wafer scale integration (WSI)

In wafer scale integration [2.8, 2.9] all the integrated circuits constituting the module are interconnected on the same wafer - in practice integrated into one very large integrated circuit using the whole wafer area. Due to defects originating both from the substrate and the processing, redundancy must be built into the circuitry, allowing for elimination of defect circuit parts by choosing only operating parts. This can be achieved by some kind of decoupling scheme, e.g. laser cutting.

So far, WSI technology is not been used commercially to any extent, in spite of large R&D efforts. The production yield problems have not been solved.

2.7.4 Silicon sensor technology

Another specialised application of silicon substrate technology is in silicon sensor technology.

Silicon sensor technology takes advantage of the following features of silicon:

- Si is an excellent mechanical material with high strength and almost perfect elasticity until it breaks.
- The physical properties of Si permit many sensor principles.
- Si is an excellent electronic material, and the sensor elements can be combined with integrated electronics, giving "smart sensors".
- Three-dimensional structuring can be done by anisotropic etching, etc. This is a new field called micromechanics in silicon.
- The Si microelectronics manufacturing technology infrastructure can be adapted.

2.8 APPLICATION SPECIFIC INTEGRATED CIRCUITS (ASICs)

Usually, an electronic designer will build up his design using standard devices, with specifications listed in the data sheets of the supplier.

However, integrated circuits can be tailored for each specific application, either by designed modification of pre-processed chips or by full custom design.

2.8.1 PROM, PAL, GAL, field programmable gate arrays

Programmable integrated circuits are a class of chips that the designer can modify by programming standard chips. Programmable memories are the most used type of such circuits: Programmable Read Only Memory (PROM), Erasable PROM (EPROM), etc., are supplied as standard chips and programmed

more or less permanently. One way of programming is cutting, or "defusing", of interconnections by electrical voltage pulses.

This principle has been adapted for logical circuits in Programmable Array Logic (PAL). The initial standard chip is made out of an array of logical AND and OR elements, all interconnected. By defusing, the specified logical function can be made, see Figure 2.14. Both the PROM and the PAL concepts have been developed by Monolithic Memories, and are implemented in bipolar technology.

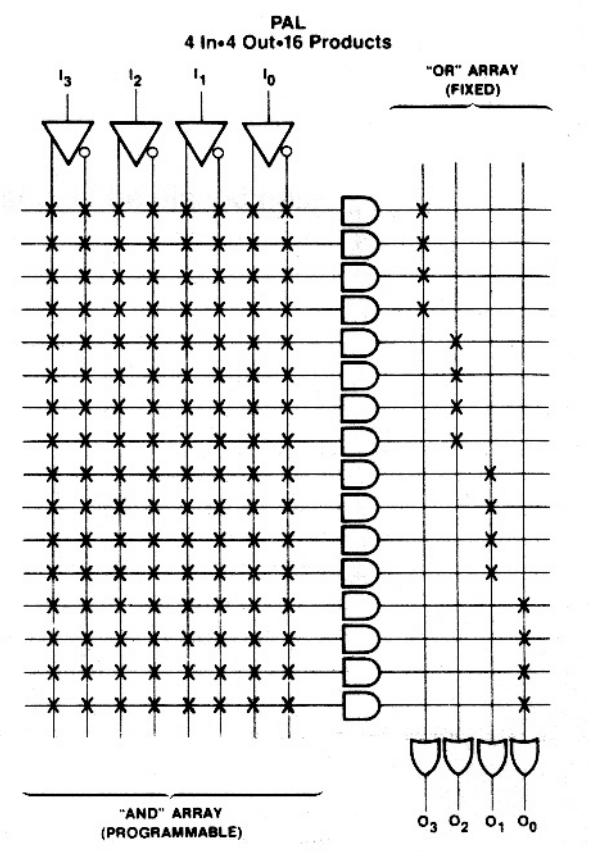


Fig. 2.14: The logical structure of a PAL (Programmable Array Logic). Programming is done by disconnecting elements in the "AND" array [2.12].

Generic Array Logic (GAL) uses CMOS technology. Here the interconnection network from the standard logical array is established by electrical programming of floating MOS switches. This way of non-destructive programming gives the technology high flexibility, since reprogramming is straightforward. GAL was introduced by Lattice Semiconductor Corporation.

The "field programmable gate array" consists of two chips. The main chip has configurable logic blocks as well as an on-chip random access memory. The other chip is a PROM. The user programs the PROM according to the desired circuit function. At start-up the PROM program is loaded into the RAM that configures the logic array for the specific application. Program errors or modifications in the application can be handled by programming a new cheap PROM, whereas the valuable main chip may be used for any number of applications. This powerful concept is used in the devices from XILINX [2.13], and similar principles are used by several other companies.

2.8.2 Custom design ICs

During the last 10 years, custom design of integrated circuits (silicon or GaAs monolithic integrated circuits) has become increasingly common for the most critical part of electronic systems. After the design by the user or special design houses, the chips are fabricated by semiconductor processing companies ("silicon foundries").

Custom designed ICs are classified in three main types:

- Gate array custom design
- Standard cell custom design
- Full custom design

A gate arrays is made up of a prefabricated layout of transistors and basic logical elements. The customer needs only to design the conductor pattern in the way that meets the specified electrical functions. Since most of the wafer processing steps are common to all users and are manufactured as a high volume process, this method is inexpensive, and the "personalisation" is fast. However, it gives limited electrical performance and limited design flexibility.

For standard cell custom design the silicon foundry has available a set of predesigned and characterised electrical building block - the standard cells - that can be combined to give the desired function of the chip. The standard cell library is available to the customer as computer aided design (CAD) layouts and/or net lists with documentation of function and performance. In this way the customer has fast access to complex and debugged circuit blocks, saving time and costs.

Full custom design is performed by designing the circuits in full detail down to the transistor level. This makes it possible to optimise electrical performance and minimise the silicon chip area for the particular application. Properly used, full custom designs give the best electrical characteristics and highest packaging density, but it requires a strong design know how, advanced equipment, and it is time consuming. Therefore, this design method is best suited for high volume or high-end applications.

In practice, many designs can be classified somewhere between standard cell custom design and full custom design; whenever appropriate, standard cells are used, but in combination with full custom design of critical parts where availability or performance of the standard cells is insufficient.

A rough outline of the design methodology for a custom designed integrated circuit is as follows [2.11]:

The semiconductor chip processing company (the foundry) supplies design rules for each of their processes available for custom designed ICs. The rules are supplied in hard copy or implemented in CAD tools. The customer generates in his CAD system a schematic capture, he simulates the functionality and makes a net list describing the circuit elements and interconnections. Alternatively he designs a graphical layout describing each of the photolithographic masks used during wafer processing.

The foundry makes the masks and fabricates chip prototypes that are packaged and sent to the customer for evaluation. For gate arrays, most of the processing is already done, and only the masks describing the custom designed interconnection patterns are made specifically for each customer. At receipt of prototypes, the customer tests functionality and other specifications. If needed, design errors are corrected, modifications are made and new prototypes fabricated. When specified performance is achieved, full scale production is done. Modern ASIC design is impossible without powerful computer aided design tools. One class of tools focuses on maximising the automation of the design cycle - this class of tools is named silicon compilators.

At the present time there are only a few major semiconductor chip processing companies that offer ASIC processing services world wide, while system companies and local or small design companies focus on having the design knowledge in-house. This is because of the extremely high cost of building, updating and operating a modern silicon processing line. On the other hand, IC design requires much smaller resources and is considered by most system companies as strategically important.

The industry structure in Norway illustrates this. Norway has no semiconductor integrated circuit processing company, but some 20 or 30 % of the Norwegian electronics producing companies have designed ASICs during the last years.

2.9 OPTOELECTRONICS PACKAGING TECHNOLOGY

Optoelectronics is a promising, fast-growing technology, partly replacing purely optical systems or electrical systems, and partly opening up new applications. The solid state laser and the low loss optical fibre are its key elements. Achievable frequency bandwidths in optoelectronics systems are several orders of magnitude higher than in purely electrical systems. We find typical applications in telecommunications systems, e.g. optical fibre networks, high speed computer networks, video cameras, etc.

Optical interconnect inside electronics systems, i.e. replacement of conductive paths with optical paths can give enhanced performance, such as higher speed, galvanic isolation, etc. [2.16]. This requires new methods and materials for the packaging, in order to maintain both electrical and optical performances. For example, packages must have optical input/output paths, such as optical windows in lasers and detectors or fibre interconnections for optical interconnects, without interfering with electrical characteristics. Examples of optoelectronic components and interconnection technology are shown in Figure 2.15

2.10 TECHNOLOGY TRENDS

The development in semiconductor technology makes ever more advanced electronic systems possible. Some important trends for the systems development are:

- Smaller critical dimensions, i.e. line widths and distances on the IC and module/PCB

- Increasing packaging density, i.e. more and more electric functions are possible to implement in a given area or volume
- Increasing maximum operating frequency/bit rate
- Increasing power dissipated per unit area and -volume
- Increased possibility to realise complex circuit functions with standard hardware by programming software
- Ever lower price per electrical function

The established technology cannot satisfy the needs and requirements, and new technology always appears. It seems as if we hit physical limits on many fronts [2.14, 2.15]. However, earlier, when such limits have appeared, new ideas and new principles have been found. This will probably also happen in the future and will make the field of microelectronics dynamic and exciting in the future, for scientists as well as for users.

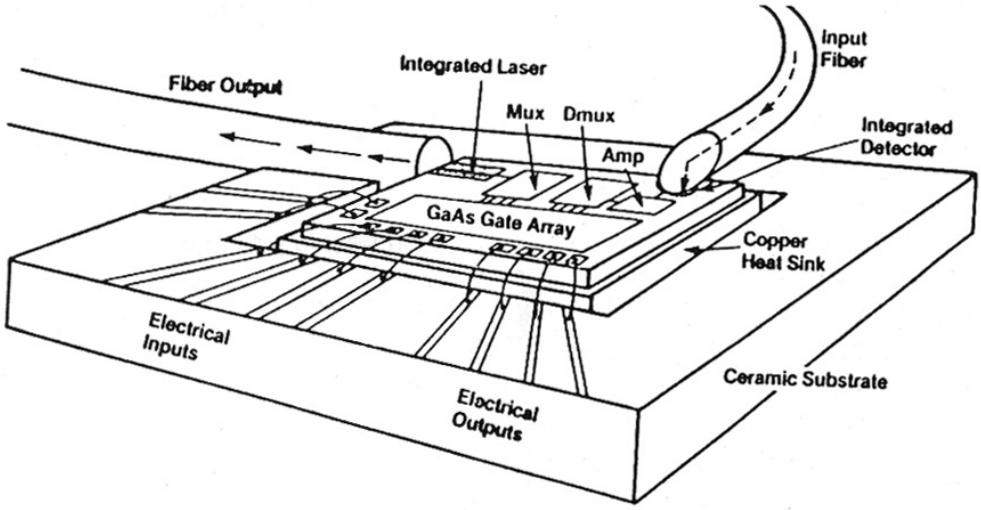
2.11 SELECTING THE OPTIMAL TECHNOLOGY

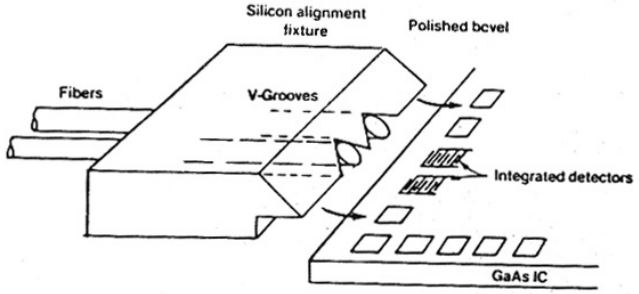
All the technologies described in this chapter have their specific advantages and drawbacks, most of which will be dealt with in more detail later. Each technology has applications where they are well suited. Starting up a product development, it is important to make technology assessments early, to pick the most suitable technology and make the design optimised for production with the chosen technology or technologies. Then the development costs can be minimised, production can be done cost-effectively, and a product with high performance/price ratio is put on the market as fast as possible.

The technology assessment should be done based upon detailed system specifications and other requirements for the product:

- Electrical specifications
- Reliability and lifetime
- Operating and environment conditions for the product. Temperature, vibrations, electromagnetic radiation, etc.
- Production volume
- Available area/volume
- Maintenance and reparability considerations
- Acceptable price/cost level
- Time-to-market
- Etc.

System level computer modelling [2.16] may be of help in the analysis and comparisons of technology choices.





Electrooptic coupler

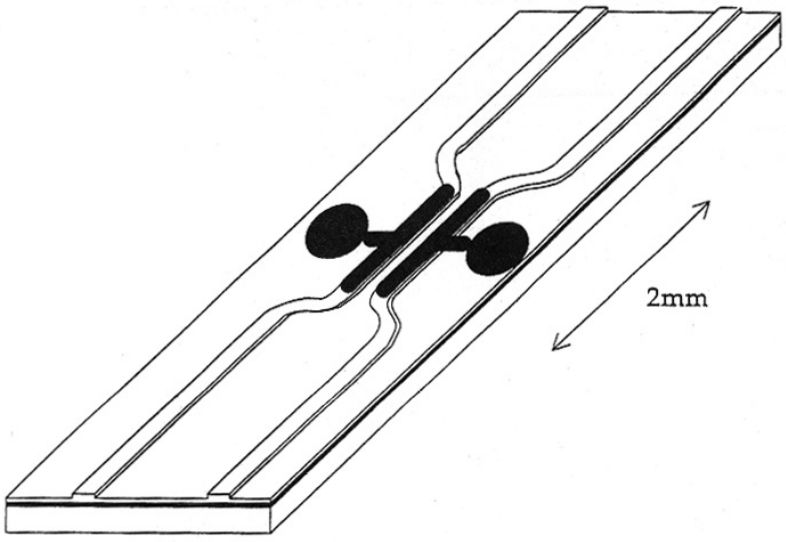


Fig. 2.15: Optoelectronics: The top figure shows different electronic and optical electronic functions in the same circuit. The middle figure shows one way to couple incoming light by reflection in 45 degree angle fixture ends, and use of a Si fixture with anisotropically etched alignment grooves. The bottom figure illustrates manipulation of light in a coupler with "light guides". By electric signals a variable interference and coupling between the two light guides can be achieved.

Traditional design philosophy took it for granted that a product should be designed based upon an established assortment of standard components interconnected with traditional printed circuit board technology. Today, a system design approach has to be taken, considering from the start the combination of electronics, mechanics, production, test, repairs, and maintenance. Selecting the technologies that give an optimal solution. This process is multidisciplinary and should involve personnel from all these fields, as well as people with intimate knowledge of the application and market- and user preferences. This interdisciplinary group should also be involved in the whole development cycle, to make optimised use of the chosen technologies.

2.12 FUTURE TRENDS FOR USERS AND DESIGNERS OF ELECTRONIC SYSTEMS

Some main trends in the evolution of technology for electronic products can be observed:

- The assortment of standard components is ever increasing, with availability of more and more complex integrated circuits and modules as standard components, with improved performance. Programmable standard components can be customised to specific applications.

- Emerging of industrial standards for specifications and documentation of standard technologies for easier communication between users, designers, producers, and subcontractors, with effective communication network based upon information technology. This infrastructure simplifies both bidding procedure and production by subcontractors, with decreasing importance of geographical closeness.

- Advanced technologies are emerging offering a broader range of features from high-end specifications to low cost than available in traditional technologies.

- Such advanced niche technologies are more specialised, making it inconvenient for most companies to have it as an in-house capability. This opens up a market with specialised subcontractor services.

- New product development should take technology assessment as an important task to be dealt with in detail with system optimisation in focus, all the way the initiation of the development.

- The market lifetime of the product is getting shorter and shorter, and therefore time-to-market must be minimised to obtain sufficient market penetration.

These factors have had a large impact of the industry structure of the electronics business the last years - a restructuring that will probably continue for at least the next 5 - 10 years.

REFERENCES

[2.1] S. M. Sze: "Physics of Semiconductor Devices". (John Wiley, 2nd Ed. 1981.)

[2.2] S. M. Sze: "VLSI Technology". (McGraw Hill, 2nd. Ed. 1988.)

[2.3] As an example: W. L. Harrod and W. E. Hamilton: "The Fastech Integrated Packaging System" (AT&T). Solid State Technology, June 1986, p. 107, and AT&T Technical Journal. July/August 1987.

[2.4] A multitude of examples of interconnection and packaging in established electronic products are given in: R. Tummala and E. J. Rymaszewski: "Microelectronics Packaging Handbook". (Van Nostrand, 1989.)

[2.5] BPA (Technology and Management) Ltd: "Compass Programme", 1986, Vol. 3.

[2.6] G. Messner: "Derivation of Uniform Interconnection Density Analysis". Proc. 7th Int. Electronics Packaging Conf., Boston, Nov. 1987, p. 833.

[2.7] IBM J. of Res & Dev. 1983; Scientific American 1983.

[2.8] As an example: S. K. Tewksbury and L. A. Hornak: "Wafer Level System Integration: A Review". IEEE Circuits and Devices Magazine, 1989.

[2.9] R. Wayne Johnson et al., eds.: "Multichip Modules - Systems Advantages, Major Constructions, and Materials Technologies". Selected reprints, IEEE Press 1991.

[2.10] A. Hanneborg og P. Ohlckers: "SIs smarte silisiumsensor". Elektro, nr. 15 - 1985. (In Norwegian)

[2.11] Y. Lundh, O. Søråsen, M. Bayegan og J.E. Pedersen: "Konstruksjon av integrerte kretser" (Universitetsforlaget, 1983).(In Norwegian)

[2.12] Monolithic Memories: "PAL Handbook".

[2.13] Xilinx handbook: "The Programmable Gate Array Databook."

[2.14] R. C. Landis: "Electronic Packaging for the Year 2000". Proc. IEPS 1988, p. 535.

[2.15] J. D. Meindl: "Opportunities for Gigascale Integration". Solid State Technology, Dec. 1987, p. 85.

[2.16] H. B. Bakoglu: "Circuits, Interconnections and Packaging for VLSI" (Addison-Wesley, 1990).