CHAPTER 3

MATERIALS AND BASIC PROCESSES

3.1 INTRODUCTION

In this chapter we have included several general topics as a background for the later chapters. We will discuss material properties for important materials, processes that are used in several types of technology and methods for assembly or interconnection of components to achieve mechanical and electrical contact.

MATERIALS

Metals, semiconductors, inorganic insulators, such as ceramics and glasses and organic materials and plastics are important for various areas of usage in electronic systems. There are tough demands on the electrical, mechanical, chemical, and metallurgical properties, as well as low flammability, corrosion resistance, stability and compatibility with other materials used. Weight, price and ease of processing are important. Low absorption of moisture may be of great importance for specific areas of applications where the materials must tolerate harsh environments and tough use.

We shall look at selected properties and applications for certain important materials. Among these materials are plastics, which are steadily increasing in importance. Most electronic engineers know little of their properties and behaviours. The tables 3.1 a)..e) give some general properties for many types of materials [3.1, 3.2].

3.2 INORGANIC MATERIALS

3.2.1 Metals

Metals are used for their good electrical and thermal conductivity. They also serve as mechanical construction materials. Copper is a particularly important element in electronics because of its very high electrical and thermal conductivity and is used in foil conductors, lead frames in component packages, thick film conductor materials, heat sinks in power electronic modules, etc. Aluminum has similar advantages, as well as low weight and price. Aluminum is commonly used for mechanical carrying structures, heat sinks, cooling towers. In semiconductor components it is used for bonding wires and circuit metallisation, etc.

The pure metals have thermal coefficient of expansion (TCE) 15 - 30 ppm per degree centigrade, much higher than the semiconductors and most ceramics. Chemical reactivity varies from very low (Noble metals like gold and platinum), to highly reactive. Mechanical properties also vary widely: pure gold, silver and indium are soft, while some of the others are very hard. Mechanical properties may depend on the processing (heat treatment, rolling, etc.), and change with small amounts of additives from other elements.

Table 3.1 a): Properties of some important materials in electronics: Conductors[3.1].

Metal/Conductor	Melting Point [°C]	Electrical Resistivity [10^{-8}Ohm•m]	Thermal Exp. Coeff. [10^{-7}/°C]	Thermal Conductivity [W/m·°K]
Copper	1083	1.7	170	393
Silver	960	1.6	197	418
Gold	1063	2.2	142	297
Tungsten	3415	5.5	45	200
Molybdenum	2625	5.2	50	146
Platinum	1774	10.6	90	71
Palladium	1552	10.8	110	70
Nickel	1455	6.8	133	92
Chromium	1900	20	63	66
Invar	1500	46	15	11
Kovar	1450	50	53	17
Silver-Palladium	1145	20	140	150
Gold-Platinum	1350	30	100	130
Aluminium	660	4.3	230	240
Au-20%Sn	280	16	159	57
Pb-5%Sn	310	19	290	63
Cu-W(20%Cu)	1083	2.5	70	248
Cu-Mo(20%Cu)	1083	2.4	72	197

Table 3.1 b): Properties of important materials in electronics: insulators [3.1].

Non Organics	Relative Dielectric Constant	Thermal Exp. Coefficient [10^{-7}/ °C]	Thermal Conductivity [W/ m·°K]	Approximate Processing Temp.[°C]
92% Alumina	9.2	60	18	1500
96% Alumina	9.4	66	20	1600
Si3N4	7	23	30	1600
SiC	42	37	270	2000
AlN	8.8	33	230	1900
BeO	6.8	68	240	2000
BN	6.5	37	600	>2000
Diamond - High Pressure	5.7	23	2000	>2000
Diamond - Plasma CVD	3.5	23	400	1000
Glass-Ceramics	4-8	30-50	5	1000
Cu Clad Invar (10%Cu)/ (Glass Coated)	-	30	100	800
Glass coated Steel	6	100	50	1000
Organics				
Epoxy-Kevlar(x-y) (60%)	3.6	60	0.2	200
Polyimide-Quartz (x-axis)	4.0	118	0.35	200
Fr-4(x-y plane)	4.7	158	0.2	175
Polyimide	3.5	500	0.2	350
Benzocyclobutene	2.6	350-600	0.2	240
Teflon (™DuPont Co.)	2.2	200	0.1	400

Table 3.1 c): Properties of ceramics, Si, Si_3N_4 and SiO_2 and polyimide.

Characteristic	Al_2O_3	AlN	SiC	Si	SiO_2	Si_3N_4	Polyimide
Specific Resistance (Ohm•cm)	$>10^{14}$	$4x10^{11}$	10^{13}	10^{-4} 10^{+4}	10^6	10^{12}	10^{16}
Relative Permittivity	9.8	10	15 45	11.9	3.9	7.5	3-4
Thermal Conductivity (W/m °K)	10 35	140 170	270	150	1.5	10 40	0.4
Thermal Expansion Coefficient (10^{-6}/°K)	5.5	2.65	3.7	2.6	0.3 0.5	2.5 3	20 70
Breakdown Field Strength (V/cm)	10^5	10^5	700	10^5	10^6 10^7	10^6 10^7	10^6
Loss Factor (tan δ)	$3x10^{-4}$	$5x10^{-4}$ 10^{-3}	$5x10^{-2}$	$4x10^{-3}$ $4x10^{-2}$	$3x10^{-2}$	–	–
Modulus of Elasticity (kN/mm^2)	300 380	300	380	170	70 72.5	280 320	3

Table 3.1 d): Elastic modules and thermal conductivity of some materials [3.1].

Material	Modulus of Elasticity E [GPa]	Thermal Conductivity k [W/cm °C]	Application
90-99% Al2O3	262	0.17	Substrate
Beryllia (BeO)	345	2.18	Substrate
Common Cu alloys	119	2.64	Leadframe
Ni-Fe Alloys(42 alloys)	147	0.15	Leadframe
Au-20% Sn	59.2	0.57	Die bond attach and lid sealant
Au-3% Si	83	0.27	Die bond attach
Pb-5% Sn	7.4	0.63	Flip chip bonding
Silicon	13.03	1.47	Electronic circuit
Au	78	3.45	Wire metallurgy
Ag-loaded epoxy	3.5	0.008	Die bond adhesive
Epoxy (Fused silica filler)	13.8	0.007	Moulding Compound

Table 3.1 e): Properties of low temperature ceramics [3.2, pages 461 and 465].
Burnout and firing conditions

System	Matrix	Filler	Metallisation	Burnout [°C/h]	Firing [°C/h]	Atmosphere	Shrinkage [%]
High-temperature cofired ceramic							
IBM	Alumina	…	Molybdenum	…	1560/33	H_2/N_2	17
Low-temperature cofired ceramic							
Asahi glass	Ba-$Al_2O_3SiO_2$-B_2O_3	Al_2O_3 Forsterite	…	…	900/1	Air	12
DuPont	Alumina silicate	Al_2O_3	Silver, Gold	350/1	850/0.3	Air	12
Fujitsu	Borate glass	Al_2O_3	Copper	…	950 to 1000/-	Reducing	.....
Matsushita	$0.35NaAlSi_3O_8$-$0.65CaAl_2Si_2O_8$	…	Copper	550/4(a) (in air)	900/0.3	Nitrogen	.....
Murata	BaO-B_2O_3-Al_2O_3-CaO-SiO_2	....	Copper	…	950/-	Reducing	13.5
Narumi	CaO-Al_2O_3-B_2O_3-SiO_2	Al_2O_3	Silver, gold(top)	…	880/0.3	Air	16
NEC	Lead borosilicate	Al_2O_3	Silver, palladium	…	900/-	Air	13
Shoei	$BaZr(BO_3)_2$	SiO_2	Copper	600/- (in air)	980/2.5	Nitrogen	12
Taiyo Yuden	CaO-MgO-Al_2O_3-SiO_2-B_2O_3	…	Copper	…	950/-	Reducing	.....

(a) Followed by a reduction step in N_2/H_2, 350°C, 0.3h

Physical properties

System	Dielectric constant	Dissi-pation factor	Insulation resistance, [Ohm•cm]	Coefficient of thermal expansion [10^{-6}/°K]	Thermal Conduc-tivity [W/m°K]	Fracture trength [MPa]	Breakdown voltage [kV/mm]
High-temperature cofired ceramic							
IBM	9.4		$>10^{14}$	6.5	16.7	275	
Low-temperature cofired ceramic							
Asahi glass	6.3	0,001	…	3,8-6,8	…	245	…
DuPont	7.8	0,002	$>10^{13}$	7,9	2,9	206	40
Fujitsu	4.9			4,0	…	…	50
Matsushita	7.4	0,002	10^{14}	6,1	2,9	245	
Murata	6.1	0,0007	$>10^{14}$	8,0	4,2	196	20
Narumi	7.7	0,0003	10^{14}	5,5	2,5	196	88
NEC	7.8 3.9	0,003 0,003	$>10^{14}$ $>10^{13}$	7,9 1,9	… …	343 137	… …
Shoei	7.0	0,001	$>10^{14}$	7,7	3,3	196	…
Taiyo Yuden	6.7	…	…	5,8	6	245	…

Alloys have poorer conductivity, both electrical and thermal. They are used to achieve better mechanical properties, or often to custom-tailor a desired thermal expansion coefficient: Invar, Table 3.1 a), (64 weight % Fe, 36 weight % Ni) has TCE of only 1.5 ppm/°C, Kovar (53 Fe:17 Co:29 Ni) has 5.3 ppm/°C, matched to glass, "Alloy 42" (42 Ni: 58 Fe) has 4.9 ppm/°C, close to that of silicon, and it is used for lead frames in component packages, etc. Alloys also have a lower melting point than the elements in them and they are used as soldering metals.

Most common is the solder metal that is a eutectic mixture of tin (approximately 63 %) and lead (37 %). Figure 3.1 shows the phase diagram for Sn/Pb.

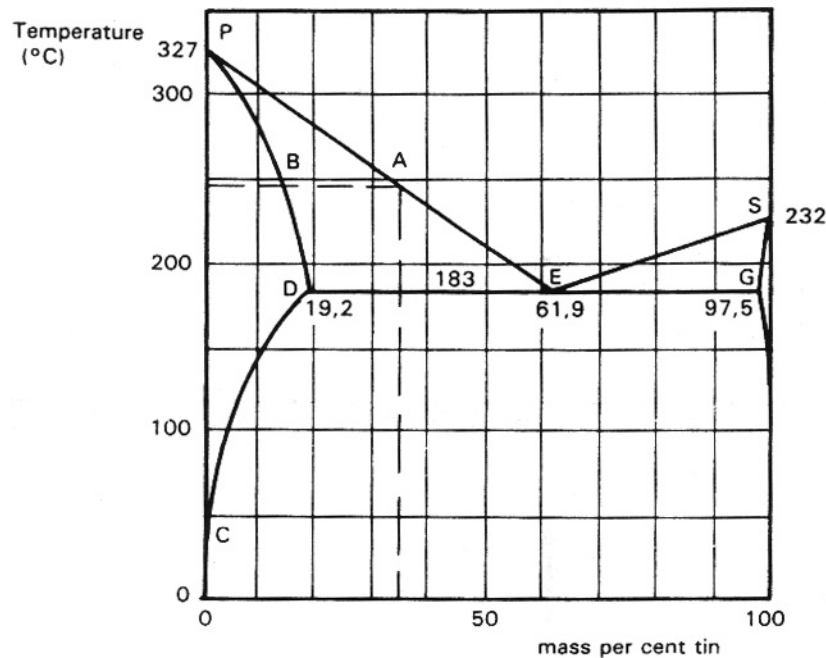


Fig. 3.1: Phase diagram for Sn/Pb. The eutectic mixture 63%/37% has a melting point of 183°C [3.13].

3.2.2 Semiconductors

The semiconductors that are most common, Si and GaAs, also have high thermal conductivity. They have very low TCE. Their electrical conductivity may be changed over many orders of magnitude by controlled doping. Silicon can be "machined" in very interesting ways by anisotropic etching. It has many exciting possibilities as a "mechanical" material. The material keeps its elastic properties practically until it breaks. It is also important for Si that it makes an oxide with very good properties, SiO_2 [3.3].

3.2.3 Inorganic insulators, ceramics and glasses [3.1, 3.2, 3.4, 3.5]

Ceramics

Ceramics are defined as "inorganic and non-metallic materials that are artificially manufactured, by high temperature reactions" (>600 °C). Among those most interesting for electronics are alumina (Al_2O_3), aluminium nitride (AlN), beryllia (BeO), silicon carbide (SiC), and glass ceramics.

Ceramics are made by the powder method: The material is made into a powder, mixed with glass particles, organic binders and solvents, by pressing or a special casting process "tape casting". Afterwards the material is sintered (heat treated) at temperatures 800 - 1600 °C. During the sintering the binder and solvents are evaporated and the powder particles are bound together (molten, in case of glasses). During the process the material typically shrinks 15 - 20 % linearly.

The tape casting process [3.1] is used for manufacturing of thin layers of ceramic. From a slurry of for example alumina powder, glass, solvents and binders a thin soft layer is made in the desired width as the material moves through an opening in the bottom of the slurry container, down on a moveable transport band. The distance between the bottom of the opening in the container and the band is controlled with great precision, and it determines the thickness of the layer of ceramic. The consistency is soft and pliable, and the ceramic in this form is called "green tape". After being cut to desired lengths, the material is further processed, by metallisation, punching of holes, etc. Often many layers are laminated on top of each other under pressure, and they are sintered at high temperature, as mentioned above. The material gets a hard brittle consistency after sintering. This process, used for multilayer ceramic substrates, will be further discussed in Chapter 8.

Ceramics are brittle and crack easily. They may have high electric resistivity and some of them have very high thermal conductivity. The relative dielectric constant may vary from 4-5 to many thousands, please refer to Tables 3.1 c) and 3.2. They are chemically stable and have a good stability in their mechanical properties up to high temperatures. However, they are often difficult to machine after sintering, and they tolerate little mechanical shock.

An important electrical parameter for non-perfect dielectric materials is the dielectric loss. This may be characterised by the loss angle δ. Tan δ is the ratio between resistive and capacitive current, and assuming we have the circuit model of Figure 3.2 with the parallel resistance Rp as the only parasitic, it may be written:

$$\tan \delta = (1/R_p)/\omega C_p = 1/\ \omega R_p C_p\ = 1/Q,$$

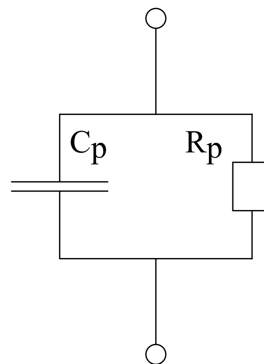


Fig. 3.2: Circuit model for dielectric loss.

Where R_p is the ohmic resistance, $1/\omega C_p$ is the capacitive impedance at frequency ω, Q is the ratio between stored energy and dissipated energy in a capacitor based on the dielectric. Tan δ is related to the complex dielectric constant:

$$\varepsilon = \varepsilon_0(k' - jk'')$$

by

$$\tan \delta = k''/k'.$$

Tables 3.1 c), 3.2, 3.4 and 3.5 show tan δ for some ceramic and other materials.

Table 3.2: Relative dielectric constant (and tan δ) for ceramics and other materials [3.4].

Material	Dielectric Constant
Teflon	2.1
Silica glass	3.8
PVC	4.6
Al_2O_3	9.9
$MgTiO_3$	20
TiO_2	100
$CaTiO_3$	160
$SrTiO_3$	320
$BaTiO_3$	1000-2000
$Ba(TiZr)O_3$	10,000
$Pb(Mg_{1/3}Nb_{2/3})O_3$	18,000

	Dielectric Constant (1Mhz)	Dissipation factor (1Mhz)
Borosilicate-E-glass	6.33	0.001
Fused Silica	3.7	0.0001
Aluminium oxide 99.5% (sintered)	9.4	0.0001
Beryllium oxide 99.5% (sintered)	6.8	0.0003
Epoxy resin	3.3-4	0.03-0.05
FR4 Laminate	4.3	0.019

Electronic uses of ceramics are, among other things, as substrates in hybrid technology, for component packages, base material in surface mounted resistors, dielectric in capacitors, piezoelectric components, magnet cores (ferrites), etc. In the future it is anticipated that superconductive oxide ceramics will play a very important role in electronics.

Table 3.1 c) shows some material parameters for some important ceramics. Alumina (Al_2O_3, 90 - 99 %) dominates as substrate for thick film and thin film hybrid circuits and hermetic component packages. The high thermal conductivity compared to organic substrate materials is very favourable. Low thermal coefficient of expansion gives a good thermal match to Si. AlN, BeO and SiC have higher thermal conductivity, and they are used in applications where the power dissipation is particularly high. However, BeO is very poisonous and AlN is more difficult to process than Al_2O_3. SiC has a very high dielectric constant. AlN, BeO, SiC are costly materials compared to Al_2O_3.

Used as a high frequency component substrate or dielectric the high dielectric constant in most ceramics may be unfavourable. For dielectric in capacitors, however, we need the high dielectric constant, and for example bariumtitanate in mixtures with other elements is used, please refer to Chapter 4.

During the last 5-6 years new ceramic materials have been developed, especially suitable for multilayer ceramic circuits. They are based on glass (calcium-, magnesium-, and silicate-), alumina and other materials, see Table 3.1 e), and they have the following advantages:

- Lower process temperature than alumna (ca. 800 °C compared to 1700)
- Lower dielectric constant (e_r down to 4 - 5)
- Thermal expansion almost equal to that of Si and GaAs

- Compatibility to noble metal metallisation (see Chapter 8).

A disadvantage is a lower thermal conductivity than for high temperature ceramic materials. Additional information is given in Chapter 8.

Glasses
A glass is an amorphous, supercooled liquid, i.e. it normally has no regular crystalline structure, and it becomes fluid when re-heated. Some materials called devitrifying glasses, or glass ceramics, convert to a crystalline state after heating, but do not reflow upon reheating.

Among the uses of glass materials are as matrix in thick film pastes (lead borosilicate, $PbO.B_2O_3.SiO_2$; cadmium borobismuthate $CdO.B_2O_3.Bi_2O_3$; bismuth sesquioxide, Bi_2O_3, etc.) [3.8]. Glasses are also used for low temperature multilayer ceramic substrates, most often in combination with the ceramics mentioned above. (See Table 3.1 e) and [3.1 p. 50 and 3.2]).

Glasses made from K-, Na-, Pb- and other metal silicates are used for hermetic, electrically insulating metal seals, providing good match of the TCE of various metal alloys. In low power thin film circuits glass is often used as substrate material.

Other insulators
Important insulating materials on the Si chips are SiO_2 and Si_3N_4, Table 3.1 c).

3.3 ORGANIC MATERIALS, PLASTICS [3.1, 3.2, 3.6]

Plastic (Greek: "plastikos", which means shaping or forming), is a large group of organic materials that harden and keep their shape after a moulding or forming process with heat and pressure [3.6]. They can be custom tailored to give good electrical, mechanical, and chemical properties, and great progress is taking place for these materials in electronic applications.

Many types of plastics are used in electronics as structural materials (boxes, component substrates, connectors, etc.), for thin dielectric layers, encapsulation of components, etc. Plastics are also used in electrically conducting or insulating glues, as process materials in production processes (photoresist, etch resist, etc.), and as binder for printing pastes in hybrid technology. A summery is given in Table 3.3. The materials can be reinforced for better mechanical strength. The many different types of plastics have properties that are becoming increasingly important to understand and use in modern electronics.

Some of the requirements for the plastics may be:
- High electrical resistivity, high breakdown field, low dielectric losses, low dielectric constant
- Thermal and mechanical stability up to the working temperature of the electronics
- Thermal expansion compatible with other materials (Si, metals,..)
- High mechanical strength for certain applications, softness and flexibility for other applications

- Chemical resistance to solvents, etc.
- Good adhesion to other materials
- Ease of processing
- Low water absorption and small change of the properties during the effect of moisture

Table 3.3 a): Plastics in various types of electronics applications.

Integrated circuits, transistors, diodes, and other discrete devices	Transfer moulding compounds, injection moulding compounds, castings, potting, dip and powder coating compounds, and die attach adhesives. Photoresists. Junction coatings.
Wires and cables	Sleevings, coatings, varnishes, intermetal dielectrics.
Connectors	Transfer moulding, injection moulding, compression moulding compounds.
Hybrids	Conductive and non conductive adhesives, sealants, conformal coatings.
Transformers, coils, bushings	Transfer moulding compounds, coatings, potting compounds, coil impregnates, wire insulation.
Printed circuit boards	Laminates, conformal coatings, solder masks, masking tapes, component attachment adhesives, and vibration dampers. Photoresists.

Table 3.3 b): Types of plastics for various purposes.

USE	SUITABLE MATERIALS
Transfer moulding	Epoxides, silicones, phenolics, polyimides.
Injection moulding	Polyethylene, polypropylene, polyphenylene sulphide.
Encapsulation/casting	Epoxides, polyurethanes, silicones.
Adhesives	Epoxides, polyimides, cyanoacrylates, polyesters, polyurethanes.
Coatings	Silicones, fluorocarbons, epoxides, polyxylylenes, polyurethanes, polyimides.
Films	Polyesters, polypropylene, polystyrene, polyimides.
Sealants	Silicones, polysulphides, polyurethanes, epoxide-polyamides, and fluoro-silicones.

3.3.1 Basic composition

Plastics are synthetic polymers. They consist of very long and complex organic molecules. A basic building block normally is the benzene molecule, see Figure 3.3. By replacing an atom in an organic molecule (built from carbon and hydrogen) with a benzene ring, one can make other molecules, which are often called monomers, please refer to Figure 3.4. When such monomers are bound together in a periodic structure, in a "polymerisation process", we get the analogous polymer composition. If we replace another atom in the same basic molecule, we get another monomer (and another polymer). By addition of smaller amounts of other elements or compositions, selected properties can be changed and improved considerably.

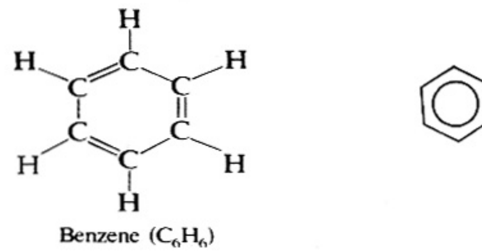


Fig. 3.3: Benzene molecule, its chemical structure and symbol.

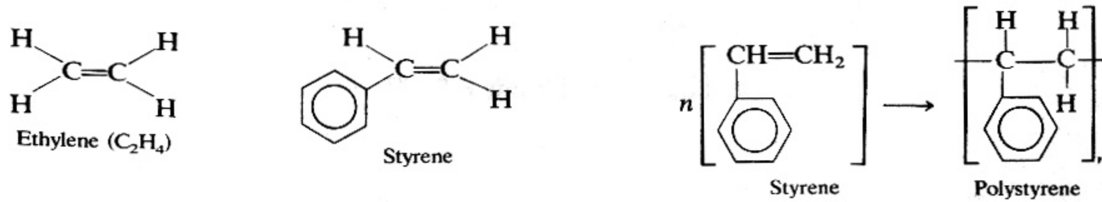


Fig. 3.4: If an H-atom in ethylene is replaced by benzene, we get styrene monomer, which can be converted to polystyrene.

The polymers may be linear, branched, or cross-linked, Figure 3.5. The cross-linking gives the best chemical stability. Two important groups of plastics are the thermoplastic and the thermosetting materials, see Figure 3.6. The first type melts when it is heated in a reversible process. Teflon (PTFE), polysulfones, polyesters are examples of thermoplastic materials. The thermosetting materials are irreversibly cross bound during the polymerisation process, and they can not be brought back to their original state.

Some examples of monomers/polymers are shown in Figure 3.7.

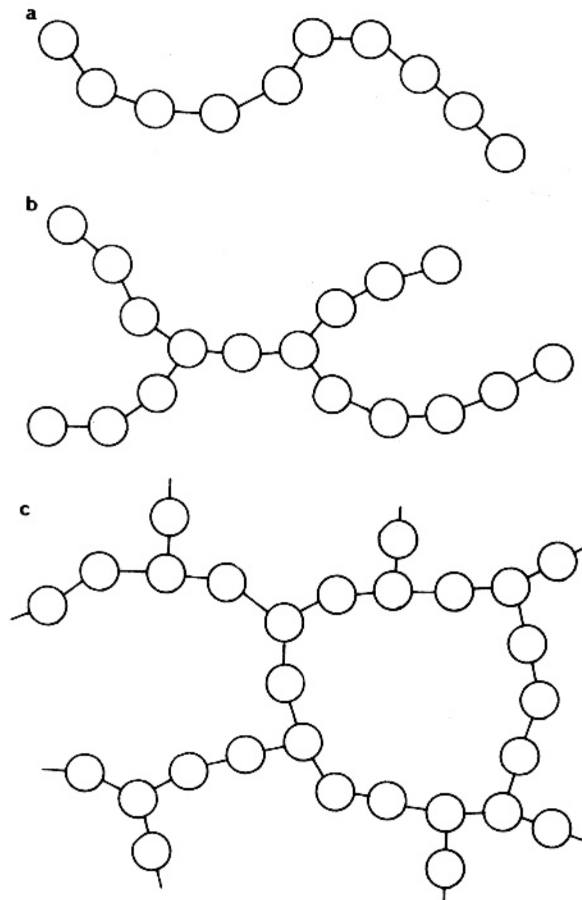


Fig. 3.5: Linear, branched and cross-linked structures in polymers.

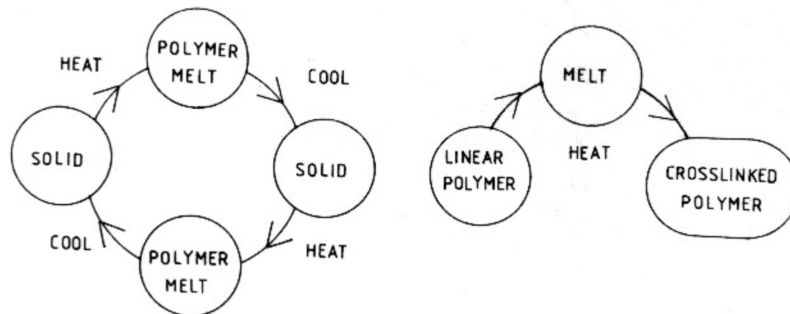


Fig. 3.6: The effect of heating on thermoplastic and thermosetting materials.

Structural unit

Polyphenylene sulphide

Polyether sulphone

Polycarbonate

Nylon 66

Polyethylene terephthalate

Silicone: R = CH_3: Methyl, C_6H_5: Phenyl, CH_2: Vinyl, OH: Hydroxyl

Polymide: Bismaldeimide

Fig. 3.7: The structural unit of certain monomers/polymers.

3.3.2 <u>The polymerisation process</u>

In some materials the polymerisation takes place during heat and some times pressure, for example for phenolics and epoxy. Other materials polymerise by exposure to UV-radiation. Often two components are stored separately, and the curing starts immediately when they are mixed, even at room temperature (two component system).

The polymerisation process may take place in several steps and may be quite complex. As an example we shall mention the process for phenolic resin, that is

used in low price printed wiring board laminates [3.7]. The starting materials are phenolic and formaldehyde. In the first stage of polymerisation the formaldehyde molecules react with the aromatic rings in the phenolic. Water is lost, and we have "A-stage" phenol resin. Further reaction gives off more water, and we get "B-stage" material, which can still melt, and which is still soluble in suitable solvents.

When the B-stage material is exposed to more heat and more pressure, in the presence of suitable activators, more water is given off. The resin hardens to a stage where it will no longer melt, and it is not soluble in ordinary solvents. In this process the long macro-molecules from the B-stage resin are cross-linked, such that the whole body of material may be treated as one big macro-molecule.

3.3.3 Electrical properties

Plastics are often used as dielectric, electrically active materials, because of their high electrical resistivity, low dielectric constant, low dielectric losses, and high dielectric strength. Values of these parameters for certain plastic materials are given in Table 3.4.

Table 3.4: Electronic properties of plastics [3.6].

Polymer	Permittivity ε_r	Tan δ	Dielectric strength [MV cm^{-1}]	Volume resistivity [Ohm•cm]
Polyethylene	2.3	-10^{-3}	5.3	$>10^{16}$
Polypropylene	2.3	$3x10^{-4}-10^{-3}$	0.24	$10^{16}-10^{17}$
Polymethyl methacrylate	3.6	0.62	0.14	$>10^{15}$
Polyvinyl chloride Unplasticised	3.5	0.031	0.24	10^{15}
Plasticised	6.9	0.082	0.27	10^{13}
Polystyrene	2.5	$1.5x10^{-4}$	0.2-0.3	$10^{17}-10^{19}$
Polyethylene terephthalate	3.3	$2.5x10^{-3}$	2.95	10^{18}
Nylon 6 (dry)	3.5	$6.5x10^{-3}$	1.5	10^{15}
Nylon 66 (dry)	3.6	$8.5x10^{-3}$	1.5	$>10^{15}$
Polytetra-fluoroethylene	2.1	$2x10^{-4}$	0.18	$>10^{15}$
Phenol-formaldehyde resin General purpose	6-10	0.1-0.4	0.06-0.12	$10^{10}-10^{12}$
Low electrical loss	4-6	0.03-0.05	0.1-0.14	$10^{11}-10^{14}$
Typical epoxide	4.5-5.5	0.01-0.02	0.2	$10^{14}-10^{15}$
Silicone rubber	3.6	$2x10^{-3}$	0.2	10^{16}

3.3.4 Mechanical, physical and chemical properties

Polymers are not perfectly elastic, and they are called "visco-elastic". Their hardness and strength vary greatly. Generally they are highly resistant to inorganic chemicals. However, exposed to water and organic chemicals they may change important parameters and they may swell, soften, crack, etc. Many polymers are hygroscopic, and water will penetrate into the material over time.

As structural materials plastics have the advantage of low weight (density typically 1.0 - 1.5 g/cm^3). Low thermal conductivity is a disadvantage when they are used as component substrates, but it may be an advantage for other applications. A typical range of values is 0.2 - 0.4 W/°C m, please refer to Table 3.1, but it can be increased by addition of metal-, ceramic- and other types of particles. The thermal coefficient of expansion is in the range of 30 - 300 ppm/°C, significantly higher than for metals and semiconductors. This may give high material stress and possibly cracking. The thermal coefficient of expansion may be reduced by additives.

3.3.5 Glass transition temperature

It is typical of many polymers in their cured form that important properties change above a characteristic temperature, the "glass transition temperature", T_g. Here the polymer changes from its glass-like state to a softer rubber-like state. The material does not melt, but T_g is the temperature where the molecular bonds are weakened. For electronic applications T_g should not be exceeded over long periods of time (many minutes), otherwise the material properties may be damaged permanently. As an example we show in Figure 3.8 the thermal expansion below and above T_g for epoxy and for other types of plastics. The changes may cause cracks, delamination and other reliability problems (for example: plated via-holes in very thick printed wiring boards).

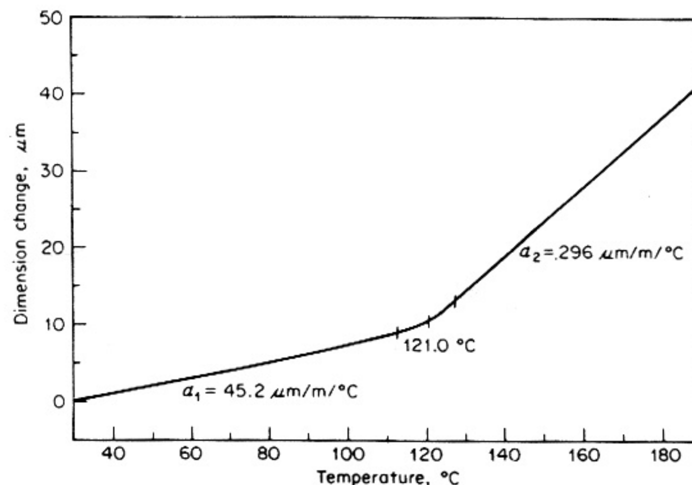


Fig. 3.8 a): Thermal expansion below and above the glass transition temperature, T_g, for epoxy [3.6].

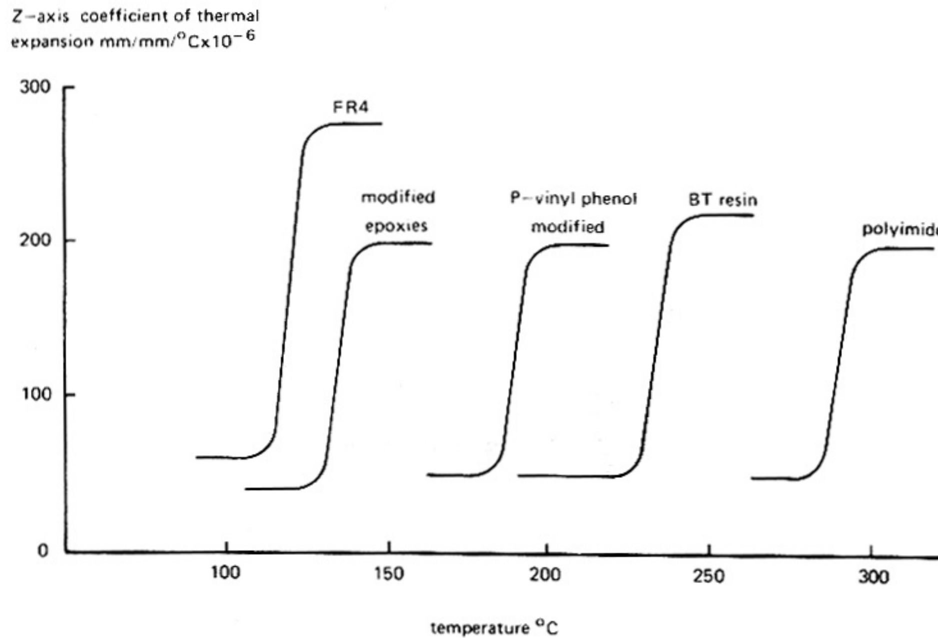


Fig. 3.8 b): The thermal coefficient of expansion below and above T_g for various types of plastics [3.23].

3.3.6 Specific materials [3.1, 3.2, 3.6, 3.8]

Below we will highlight some important groups of polymers. There are many types with varying properties within each group.

Epoxy

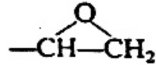
Epoxy has a wide range of molecule structures and properties, but all with epoxide atom groups. Please refer to Figure 3.9 a). 90 % of printed wiring board laminates used today are epoxy based. Bisphenol epoxy is used the most, with addition of epoxy novolac, see Figure 3.9 b). Also adhesives, structural plastics, etc. are made from epoxy. For moulded plastic encapsulation of components, epoxy of the type novolac is the most used. [3.2, p.474]

Moisture will penetrate epoxy over time and may cause corrosion in the presence of alkali ions. As hardener epichlorohydrin is often used. It can leave chlorine in the cured epoxy. Together with moisture this gives HCl, which creates corrosion and reliability problems over long time. Low chlorine content (a few ppm) is therefore a common requirement for epoxy in electronic applications. Silica particles are added to the epoxy to reduce the thermal coefficient of expansion from 40 - 50 to approximately 20 ppm/°C. This will reduce the thermal stress near the silicon chip and the metal in the package. Br is added as a flame retardant, but it also gives corrosion when moisture is present.

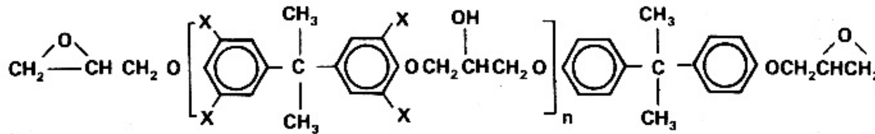
Epoxy normally is strong and hard. For certain applications it should be soft to reduce mechanical stress. This can be achieved by adding special oils, elastomers of the type akrylonitrile-butadiene-styrene, silicone or polyurethane, before the curing.

Many other modifiers and additives are used to optimise epoxy for various applications.

a)

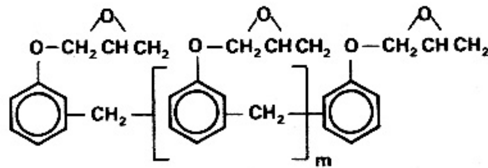


b)



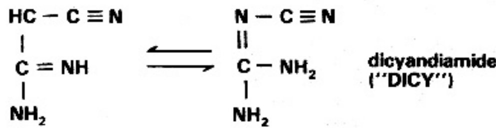
Bisphenol A (X = H) and Tetrabromobisphenol A (X = Br) copolymer. Br content 15%-20% of resin weight for adequate fire retardance in glass cloth/epoxy resin composites.

c)



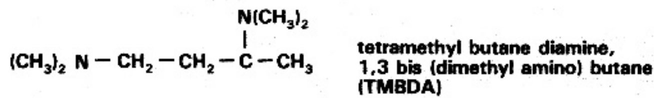
Epoxy novolac resin. Added 10-20% of total epoxy resin weight to increase crosslink density.

d)



Curing Agent Dicyandiamide

e)



Catalyst, Accelerator

Fig. 3.9: a):The epoxide group, which is the building block in epoxy, b) - e): Starting materials for epoxy: b): Bisphenol A, which constitutes most of the starting material. The H-atoms in the places X are often replaced with Br to reduce the flammability; c): Epoxy novolac; d): The hardener dicyandiamide; e): The catalyst [3.1].

Phenol

Phenol is used for low price printed wiring board laminates with relaxed environmental and performance requirements (consumer products). Phenol is also the matrix for several materials that are screen printed in polymer thick film technologies (see Chapter 8), and for adhesives.

Polyimide

Polyimide is a group of plastics in rapid development. Among the applications are high performance printed wiring boards, dielectric films for insulation in thin film hybrid circuits and silicon integrated circuits, flexible printed circuit board substrates (e.g. known under DuPont´s trade mark Kapton). Polyimides are strong and mechanically stable. High T_g permits a high working temperature. They are suitable for high frequency dielectrics because of low dielectric constant and low dielectric losses. Many polyimides have the disadvantage that they are hygroscopic and absorb up to 2 % moisture. Electrical and mechanical properties change in the presence of moisture, and corrosion can occur.

Teflon

Teflon (Polytetrafluorethylene, PTFE) is extremely resistant against chemicals. It is used, among other things, as dielectric in high frequency substrates because of its low dielectric constant (e_r = 2.1) that is nearly independent of frequency and temperature. The loss tangent is also low. Because the material is so chemically inert and has poor adhesion to almost all materials (please refer to the use of Teflon coating in household frying pans), it is difficult to process [3.6]. Teflon is a thermoplastic material.

Polyester

Polyester (polyethylene terephthalate, PET) is a thermoplastic material melting around 260 °C. It has good dimensional stability below T_g that is at approximately 70 °C, but it shrinks above T_g. Polyester has good chemical resistance, high mechanical strength, favourable electrical properties and low price characterises polyester. It is used for low price flexible substrates, (membrane switch panels, etc.), printing screens, dielectric in capacitors, moulding material, surface protection material ("conformal coating"). It is not usable at temperatures for normal soldering processes because of uncontrolled shrinkage. Polyester is made by DuPont under the trade name Mylar.

Silicone

Silicone has the structure shown in Figure 3.7, where R can be similar or dissimilar organic groups, often methane (CH_3) or phenyl (C_6H_5). Some types of silicone are flexible over a large temperature range. They are hygroscopic, but they can be made with very high purity (below 5 - 10 ppm halogen content). Their high dielectric strength and high electrical resistivity are also useful. However, they have a high thermal coefficient of expansion, low mechanical strength and -stability, and they are not especially resistant against solvents and other chemicals. Often they have poor adhesion to other materials, and they may be costly. Silicones are made as liquid, as "grease", gel or elastomer (rubber like). They are used for passivating by conformal dip coating or as deposited, thin layers. They give very good environmental protection. Power electronic modules often have epoxy on top of a layer of silicone gel to give mechanical strength (the epoxy) as well as environmental protection and low stress on the chip (the silicone) [3.24]. Before curing the silicone adheres and spreads very easily and it can contaminate soldering areas and ruin the solderability in PWBs, etc. Silicones can be made to cure at room temperature, at high temperature, or under UV-exposure.

Polyurethane
Polyurethane gives good adhesion, it cures fast, it is flexible at low temperatures, and has low moisture penetration. However, the thermal coefficient of expansion is high, it is difficult to remove and it shrinks at curing. Its uses are primarily as moulding material for mechanical protection.

Parylene (paraxylylene)
Parylene is used for dip coating as protection. Good resistance against solvents and low water penetration characterise Parylene. Certain properties for parylene and other materials for dip coating are given in [3.2, p. 783, 3.8, p. 225].

Acrylic
Acrylic of suitable composition cures in UV-radiation. Various types of acrylic are used for photoresist, UV-curing adhesives, in addition to dip coating, etc.

Table 3.5: Properties of high temperature moulding plastics [3.6, page 307].

Property	Poly-sulphone (Udel)	Polyether sulphone (Victrex)	Poly--phenylene sulphide (Ryton)	Polyether--imide (Ultem)	Ultem +20% glass reinforced
Flexural strength [x10^{-3}psi]	15.4	18.6	25	21	30
Flexural modulus [x10^{-6}psi]	0.39	0.37	1.7	0.48	0.9
Tensile strength [x10^{-3}psi]	10.2	12.2	16.2	15.2	20
Dielectric constant [1 MHz, 25°C]	3.03	3.45	3.8	3.1	3.5
Dissipation factor [1 MHz, 25°C]	0	0.008	0.0014	0.006	0.0015*
Volume resistivity [x10^{-17} Ohm•m]	50	100	45	6.7	0.7
Electrical strength [kV/mm]	17	16	17.7	28	26.5
Deflection temperature [^{o}C] at 264 psi	174	202	243	200	209
Thermal expansion coefficient [ppm/^{o}C]	56	55	40	56	25
Water absorption [%] (24h)	0.3	0.4	0.05	0.25	0.26
Maximum continuous temperature [^{o}C]	160	170-200	170	170	170

* 1kHz

Polysulphone, polyethersulphone, polyetherimide
These are high temperature thermoplastic materials with good thermal and mechanical stability, favourable electrical properties, but limited chemical resistance to certain solvents. They are used for moulding structural materials and for printed wiring board materials. These materials are increasingly being

used for 3-dimensional PWBs, please refer to Section 5.13 .Their properties are shown in Table 3.5 [3.1, 3.6, p. 308].

BASIC PROCESSES

3.4 TRANSFER OF PATTERNS BY PHOTOLITHOGRAPHY [3.8, 3.9]

Photolithography is used for transfer and definition of patterns. Accuracy and resolution down to 0.2 µm can be achieved, with improvement of resolution as a main bottleneck challenged by the IC industry.

The starting point is a pattern generated from a CAD system or similar, on a photographic film, the photomask or artwork. The film substrate is a plastic foil, or a glass plate when high precision is required. The pattern on this film is made by exposure with a computer controlled photo plotter, laser (or a computer controlled electron beam, for sub-micron resolution), see Chapter 5.

Figure 3.10 shows the procedure for transfer of the pattern. A thin layer of photosensitive material, photoresist, may be deposited on the object surface by spinning. This process consists of depositing a few drops of photoresist by dispenser. Then the object is rotated fast, and the resist is spread over the surface by the centrifugal force. Alternative methods are spraying, screen printing (see below), or laminating on the resist in the form of a dry film. The surface is illuminated through the photo mask. Afterwards the resist is developed and cured by heating.

Two classes of photoresist behave differently: Positively and negatively acting resist. The negative resist is dissolved by the developer where it is not illuminated (Figure 3.10). Thus we remain with hardened resist in the reverse (negative) pattern relative to what is black on the photo mask. The positive resist behaves the opposite way: We get the same resist pattern remaining on the substrate or wafer as the black areas on the photomask. Positive resists generally give the best definition, but they are more costly than the negative ones.

The cured resist is resistant to many etchants, and it protects the material underneath from the etchant. Thus, when we want to etch a metal layer, the photoresist may be used as etching mask. When the etching process is completed the rest of the photoresist is dissolved in a suitable solvent.

Photolithography is used for printed wiring boards, in hybrid technology and on semiconductor wafers. In addition to etch masking, it is also suitable as a mask during plating, and in the fabrication of screens for screen printing.

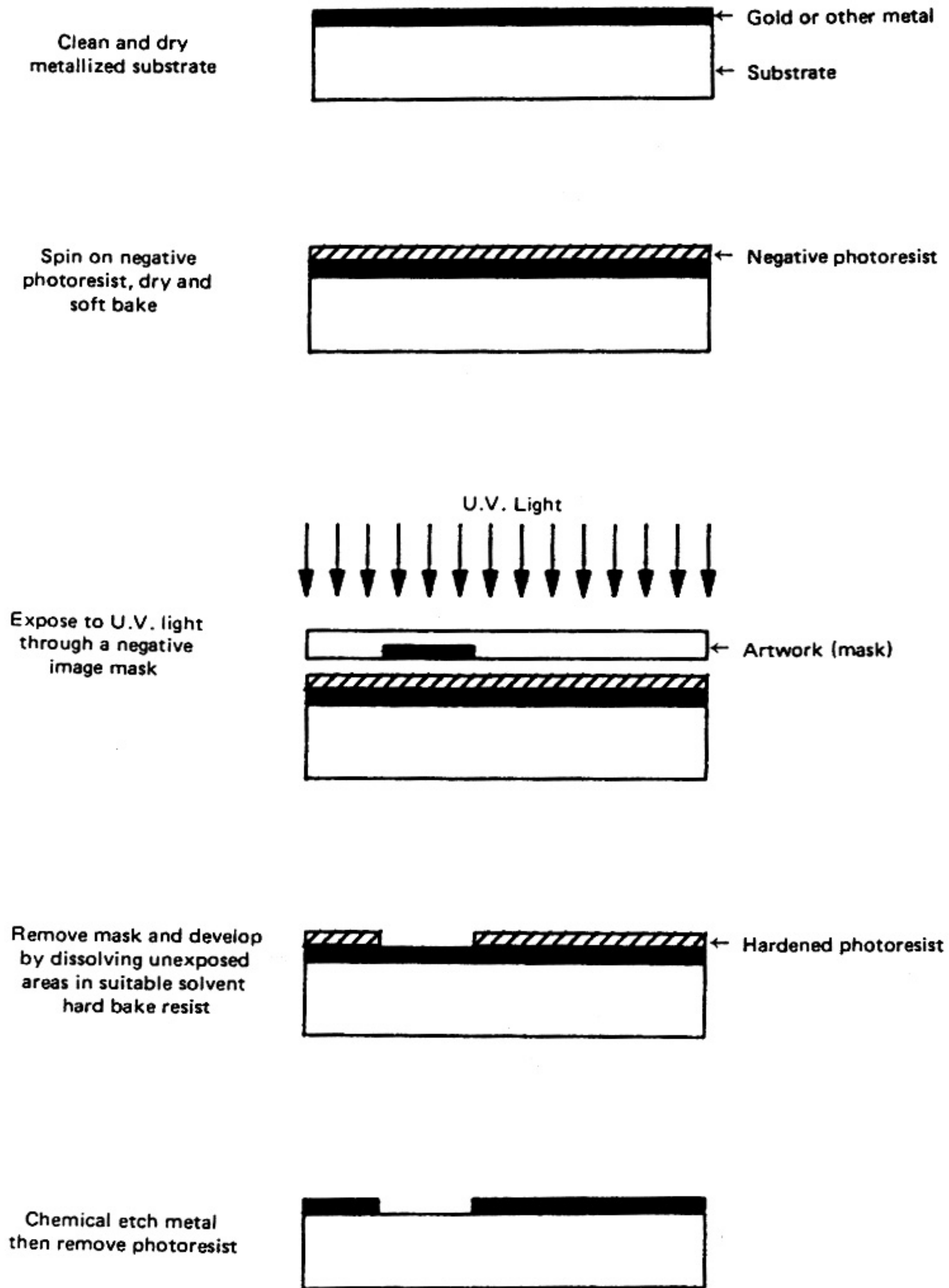


Fig. 3.10: The steps in photolithographic transfer of patterns and the subsequent etching of metal films with negative photoresist. If positive resist is used, it is the illuminated part of the photoresist, which is removed during the development.

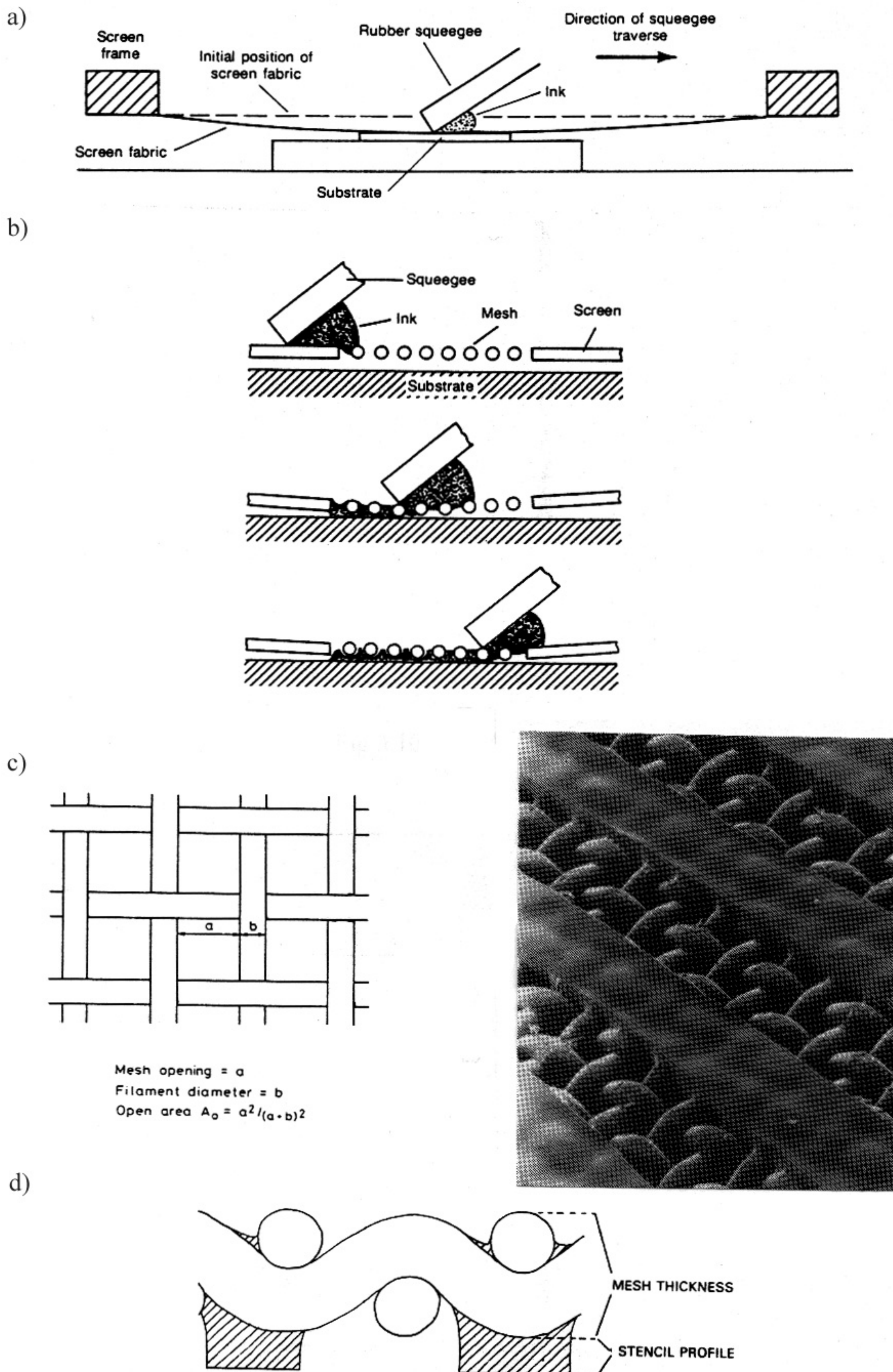


Fig. 3.11: Screen printing: a) and b): Printing process, c) and d): Details of the screen [3.2, 3.11].

3.5 SCREEN PRINTING AND STENCIL PRINTING

Transfer of patterns and deposition of materials by screen printing, or "silk" printing, consist in pressing material in paste form through the openings in a printing screen. This is analogous to the process used in reproduction of art. Earlier a screen of silk was used and the name is still left, even though woven screens today are made from polyester filaments or metal wires. The screen is stretched and tensioned on a metal frame, as shown in Figure 3.11.

The preparation of the printing screen consists of depositing a photo sensitive film (emulsion) with desirable thickness on the screen. The emulsion may be polyvinyl alcohol or -acetate, made light sensitive by additives, e.g. sodium bicarbonate. It softens in water and penetrates into the woven structure. After drying it is exposed through a photomask with the desired pattern, dried, developed and cured like the resist in photolithography.

The paste that is to be printed is forced over the screen by a squeegee, as seen in Figure 3.11, which is made of polyurethane rubber or similar material. Normally there is a distance of a few millimetres between screen and substrate ("snap-off"), and the screen is forced into contact with the substrate by the pressure of the squeegee. Where there are openings in the resist on the screen, the paste is pressed down onto the substrate.

Screen printing is a craftmanship that requires experience and knowledge to give good and reproducible results. The process can also be modelled theoretically by hydrodynamic theory [3.10].

Important factors for good definition, accurate pattern placement and correct amounts of paste are, among others:

- Fineness of the screen and the wire (the number of wires per unit length, "mesh", and the wire diameter)
- Thickness of the resist, Figure 3.11 d)
- Squeegee hardness, angle and speed of motion
- Tension in the screen and snap-off
- Viscosity and printing properties ("rheology") of the paste

Certain materials are added to the paste to give high "thixotropy", in the same way as in modern paints. This means that the paste will flow easily under the pressure of the squeegee, but it has high viscosity without pressure [3.2, p. 838, 3.11]. With high thixotropy narrow printing patterns will get steep walls after printing. This makes it possible to print patterns down toward 0.1 mm widths and distances. The dimensional control is limited by the wires in the weaving, the screen deformation during the printing and the accuracy in the registration of the mask relative to the substrate.

The amount of paste that is printed, is the gross area multiplied by the fraction that is not covered by wires, Figure 3.11 c), and the thickness of the mask.

Screen printing is used in the production of printed wiring boards, thick film hybrid circuits, printing of solder paste for surface mounting, etc. Typical screen parameters for thick film hybrid technology are 80 - 400 mesh (number of wires per inch), wire diameter 20 - 100 μm. For solder paste printing 40 - 120 mesh is

typically used, with wires 60 - 120 µm diameter, and approximately 50 % open area. With this information, and screen thickness, the volume of solder paste can be calculated.

High mesh count, thin wire and thin emulsion will give high resolution but a thin printed layer and a more fragile screen that is easily damaged. Details are found in [3.8, page 80, 3.11, page 173, and 3.12].

For printing of solder paste to high precision, the printing screen is replaced with a thin plate of metal or plastic. The openings are etched in a photolithography process, or they are punched, see Section 7.3. Such printing stencils have better dimensional stability and better wear properties than woven screens. However, one cannot make enclosed patterns or long patterns with short widths, and printing stencils are not suitable for printing of conductor patterns.

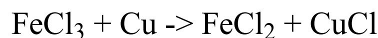
3.6 ETCHING [3.7]

3.6.1 Wet, chemical etching

The most common method for making conductor patterns is to first cover the whole board area with conductor metal. Then, masking by screen printing or photolithography, and removing the metal where it is not desired by dipping the sample in a chemical bath that dissolves the material, with the other parts of the surface being covered with an etch resist that is not attacked by the etchant. The etchants normally are aqueous acidic or alkaline solutions. This is called subtractive processing. The etchant can also be sprayed on to the surface to get good circulation and uniform etching. The speed of etching depends on the temperature, the composition and concentration of the etchant, how long the etching bath has been in use, circulation, etc. Control and reproducibility may be critical.

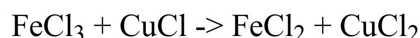
The choice of etch composition depends on what is to be etched and what is not to be etched, namely the etch resist. Some examples of etching reactions can be given:

Etching of copper: Several etching compositions are used. One of them is iron chloride, with the following reactions:



$FeCl_3 + Cu \rightarrow FeCl_2 + CuCl$

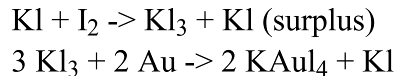
In addition the following reaction takes place:



$FeCl_3 + CuCl \rightarrow FeCl_2 + CuCl_2$

This etchant does not attack organic films that may be used as etch resists. However, tin/lead is etched and is therefore not usable as "masking" for pattern definition, as is common (please refer to Sections 5.5 - 5.6). Regeneration of the etchant is difficult, and the bath has to be discarded when its composition gets out of the specified range, giving a pollution problem. Other possibilities are sulphuric acid/peroxide, copper chloride, sodium chloride, and ammonium persulfat. For details see [3.7, p. 283].

Etching of gold: Potassium iodide and iodine are common etchants:



$Kl + I_2 \rightarrow Kl_3 + Kl$ (surplus)
$3\ Kl_3 + 2\ Au \rightarrow 2\ KAul_4 + Kl$

This etchant is used for thin film metallisation by gold on top of nickel/chromium (Chapter 8). To avoid that the etchant also attacks NiCr, one adds inhibitors of ammonium phosphate, etc. [3.8, page 74].

3.6.2 Dry etching

Wet, chemical etching is normally isotropic, which means that it etches in all directions with approximately the same speed. If we are to etch through a 10 µm thick layer, it also etches approximately 10 µm in the horizontal direction. The smallest lateral dimensions that can be etched are therefore in the same order of magnitude as the thickness. "Dry" plasma etching, or reactive ion etching, may give anisotropic etching, with an etching speed that is substantially greater vertically than laterally. Such etching is done with an etching gas in plasma form. The etching gas is ionised at low pressure in a closed etching chamber with a vacuum pumping system and controlled supply of gas. Reactive ion etching is done with a chemically active gas. The ions react with the surface and generate reaction products in gas form, which are pumped away. By means of electrodes and an electric field in the chamber one manages to get the ions to hit the surface with a preferred direction, which gives anisotropy in the etching. Under suitable conditions one can also etch in a sputter chamber "sputter etching", see Section 3.8.2.

3.7 PLATING [3.7]

Plating is building of conductive materials by an electrical process, in which ions of the material in a solution (electrolyte) are deposited and give off their ionic charge when they hit the object that is to be plated. There are two main types: Electrolytic and chemical ("electrolyses").

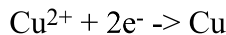
3.7.1 Electrolytic plating

By electrolytic plating the current passes through the object, the electrolyte and an external circuit. The deposition only takes place on conductive surfaces that are connected to the external circuit. By chemical plating it is the electrochemical conditions in the electrolyte and in the surface of the object that cause the ions to deposit on the surface. Chemical plating may be done both on conducting and insulating surfaces.

As an example of the electrolytic plating we will describe the deposition of copper: The object is immersed into an electrolyte that contains Cu^{2+} ions, for example $CuSO_4$ dissolved in H_2SO_4. The object forms the negative electrode (cathode), and a metallic copper plate forms the positive electrode (anode) in an electrolytic cell. Copper is dissolved on the anode:

$Cu \rightarrow Cu^{2+} + 2e^-$.

The reaction at the cathode is the reverse:


$Cu^{2+} + 2e^- \rightarrow Cu$

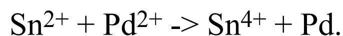
Thus, metal is removed from the anode and deposited on the object. (The cathode)

Electrolytic plating normally is a simple process. It can give a high rate of deposition (tens of µm per hour). The structure in the deposited material depends of the speed of deposition (current density), temperature and type of plating bath.

3.7.2 Chemical plating

To make the chemical plating process act on an insulating surface or parts of an insulating surface, they must be "sensitised" and "activated". We will describe the main steps in standard chemical plating of copper as an example. The whole process is relatively complicated [3.7, page 262].

The sensitising consists in dipping the object in a solution containing Sn^{2+} ions, to increase the sensitivity of the surface. Sn^{2+} ions are adsorbed on the surface. The activation takes place in an acidic solution of palladium chloride, which is transformed to metallic Pd. The reaction is the following:


$Sn^{2+} + Pd^{2+} \rightarrow Sn^{4+} + Pd$.

In the plating process (see below) Pd is a catalyst for the deposition of copper. (There is still doubt about the details of this process [3.7].)

The plating process continues as follows: The object is immersed into a reducing bath that contains Cu^{2+} ions, for example in the form of dissolved $CuSO_4$. Formaldehyde, HCHO, is the most common reducing agent. In this bath Cu^{2+} is reduced to Cu, which covers the whole surface, even where the surface is electrically insulating. At the same time formaldehyde is oxidised into acetic acid.

Chemical plating is a critical process, if we are to achieve good adhesion and controlled deposition. The composition of the solutions is complex, and if the composition, temperature, "bath loading" (the ratio between plated area and the volume of the bath) drifts outside the acceptable values, Cu^{2+} may be reduced to metallic Cu in the bath itself, which is thereby destroyed.

3.8 VACUUM DEPOSITION AND SPUTTERING [3.8]

3.8.1 Vacuum deposition

Thin metal films on hybrid substrates and semiconductor wafers are normally deposited by vacuum evaporation or by sputtering. Vacuum evaporation takes place in a chamber, Figure 3.12, which is evacuated to a vacuum of typically 10^{-6} Torr. The metal that is to be deposited is placed in a recess in a plate of high temperature melting metal, e.g. W, the "boat". The boat is heated by passing a high current through it (resistance heating), until the metal evaporates and its molecules spread out upwards in all directions in the vacuum chamber. The molecules hit the substrate that is located on the substrate holder above. A different way to heat the metal is to bombard it with an electron beam that is accelerated in an electric field with the boat as anode.

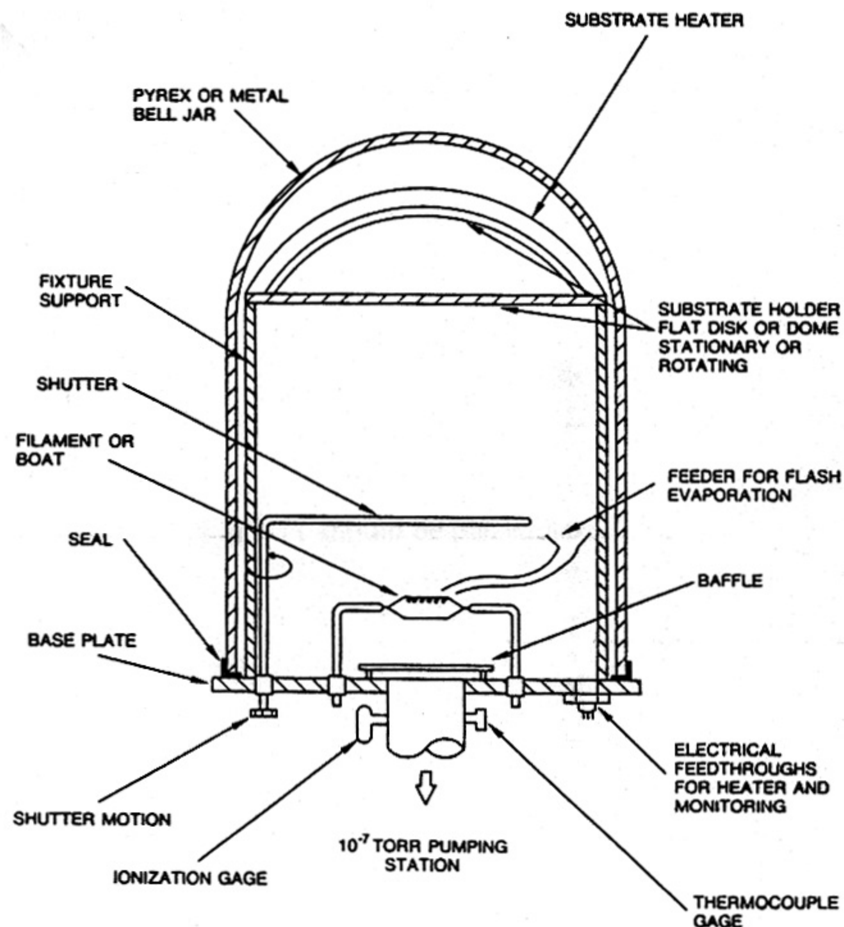


Fig. 3.12: Vacuum evaporation.

3.8.2 Sputtering

Sputtering is a process under low pressure where a "target" is bombarded by energetic positive ions. When the ions hit and give off their energy, particles are ejected from the target. These "sputtered" particles hit the substrate that is to be covered. The simplest version is DC sputtering, Figure 3.13. The plasma may be a noble gas, for example argon, at pressure 10^{-3} - 10^{-1} Torr. The gas is ionised in the strong electrical field, obtained by having 1000 - 2000 V between the target and the anode. A glow discharge is created in the argon gas, which is

decomposed into positive ions and free electrons. The ions are accelerated toward the cathode (target), they give off their charge by receiving electrons and are again neutral. Target material is torn off by the energy released. Energetic secondary electrons interact with neutral Ar atoms that are again ionised. Typical deposition rates are 100 - 1000 Å per min. Film thickness by sputtering, as well as by vacuum deposition, is limited to a few µm.

Electrically insulating target materials are not suitable for DC-sputtering, because they will be electrically charged and then disturb the glow discharge. Then AC radio frequency is used on the target holder electrode. Other types of sputtering are reactive sputtering and magnetron sputtering, which have other advantages.

Metals as well as alloys, oxides, glass and organic materials can be deposited by sputtering, by choosing a target made of the desired material. By placing the substrate as a cathode and masking selected areas, we may sputter etch, when the positive ions bombard the substrate surface and tear loose particles from the uncovered areas.

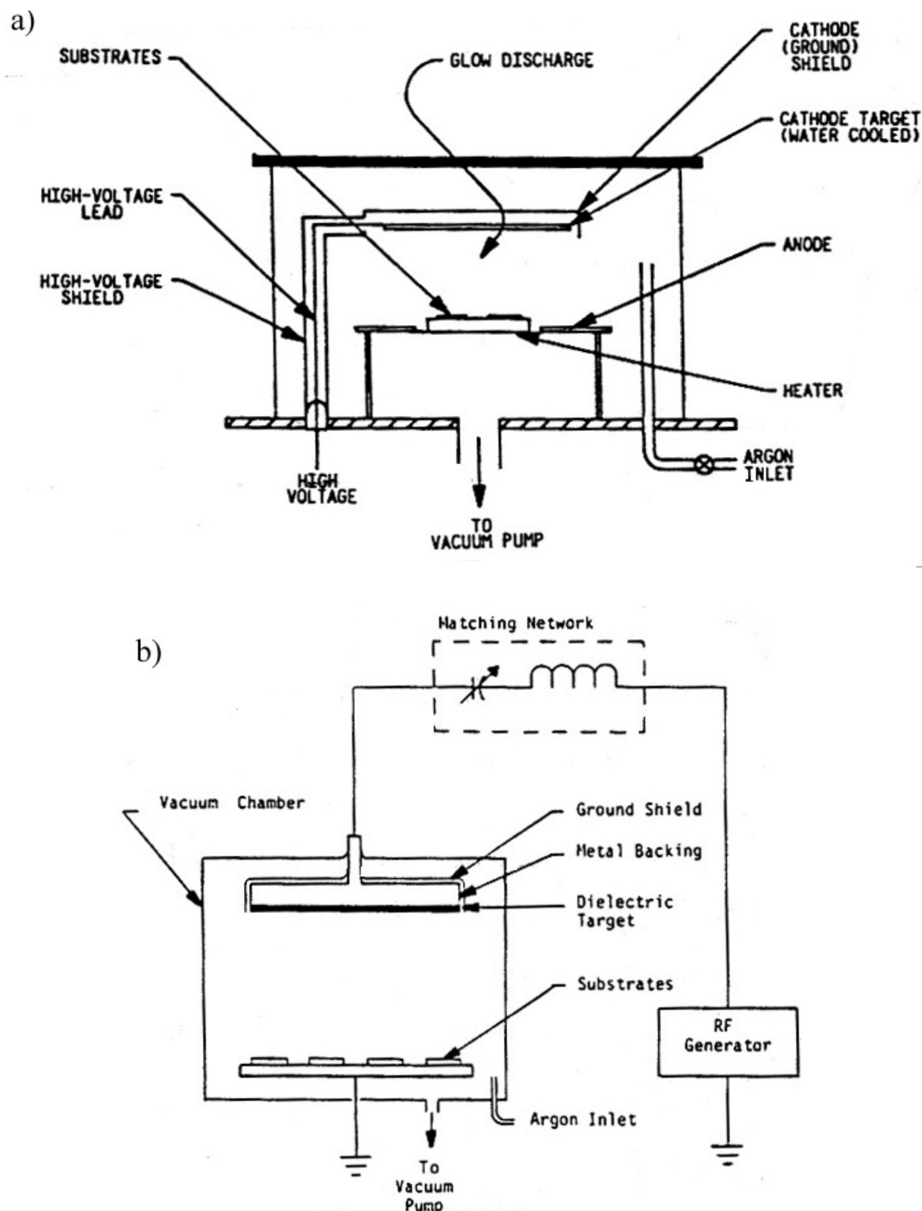


Fig. 3.13: Sputtering: a): DC sputtering, b): Radio frequency AC sputtering [3.8].

METHODS FOR ELECTRICAL AND MECHANICAL CONTACT

3.9 GENERAL

In this section we describe basic methods and processes for providing mechanical and electrical contact in electronics.

Soldering and gluing are used to hold parts together as well as to give electrical contact, whereas bonding only serves for electrical contact (except for die bonding).

3.10 SOLDERING [3.7, 3.13]

Soldering is the dominating method for electrical connection of electronic components. It is also important for mechanically assembling and to establish good thermal contact. It may be defined as "establishment of a metallic bond between two metallic surfaces by use of a different liquid (solder-) metal".

Soldering consists in wetting the surfaces that are to be joined by the molten solder metal and cooling until it solidifies. Soldering with high melting alloys is called hard soldering or brazing, and it is used mainly for connecting structural mechanical parts. In electronics, soft soldering with tin/lead alloys, with melting point around 180 °C, dominates. The materials are cheap, the process can easily be automated, and the parts may easily be taken apart for repair.

Yet soldering is the source of a large fraction of the faults in the electronics, during production as well as during the field life of the product afterwards.

Some factors that determine solder quality:
- Metallurgical and mechanical properties of the solder metal and compatibility with the metal on the surfaces to be joined
- Wetting
- Surface properties
- Grain structure in the solder metal.

3.10.1 Wetting

With poor wetting the solder metal will tend to contract into a spherical shape, seeking the minimum surface area because of surface tension in the solder metal, γ_l, Figure 3.14. If we have good wetting the surface tension between the liquid and the base material, γ_{ls}, dominates and stretches the drop out. The drop and the base material will minimise the free energy that also includes the surface tension in the base material, g_s. This can be described by Young's equation [3.13]:

$$\gamma_{ls} + \gamma_l \cos \Theta = \gamma_s$$

The surface properties that determine the wetting depend on many parameters. The combination of materials is of great importance. Purity is important, an oxide layer on top of copper or solder metal for example, may ruin the wetting. The surface structure and the roughness, are also important. In a good solder

joint the atoms diffuse from the solder metal into the surface of the base material down to 0.1 - 1 µm. In order to improve the wetting fluxes are used, as described in section 3.10.3 in this chapter.

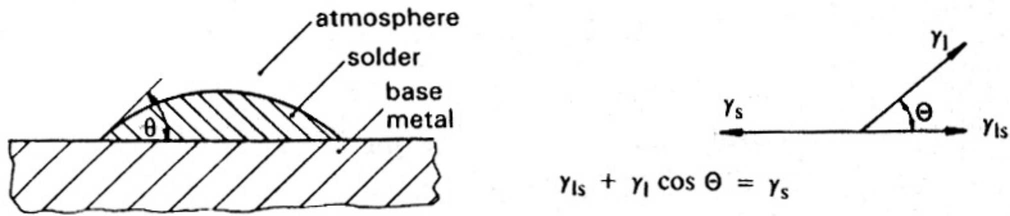


Fig. 3.14: Wetting in soldering.

3.10.2 Solder metal

It is most common to have a eutectic mixture of Sn/Pb: around 63 % Sn/37 % Pb (weight %). The melting point is 183 °C, see Figure 3.1. Some properties of solder metal are given in Table 3.6. Due to high price of tin a higher percentage of lead is often used. That will raise the melting temperature and it makes the wetting properties inferior. Even small concentrations of other elements change the properties.

Table 3.6: Properties of solder alloys 63 Sn:37 Pb or 60 Sn:40 Pb (weight %) [3.13, page 162].

	Temp. [°C]	Value	Unit
Electrical resistivity, ρ	25 100	0.17 0.32	µOhm•m "
Thermal conductivity, °K	25 100	51 49	W/m°K "
Thermal coeff. of expansion, α		24.5	ppm/°C
Specific heat		46 000	J/kg°K
Modulus of elasticity, E	25	32 000	N/mm^2
Density, ρ		8.5	g/cm^3

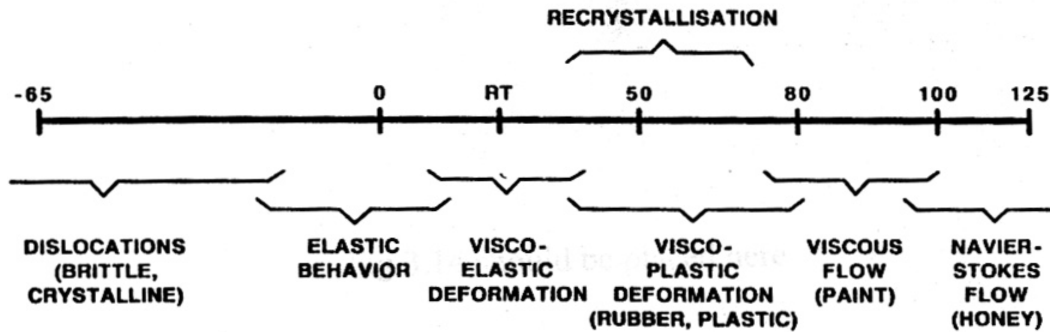
The mechanical properties of solder metal change strongly over the normal temperature range of operation of electronics, see Figure 3.15. This is because the highest temperatures approach the melting point. Below 0 °C the solder metal behaves elastic, whereas at the temperatures above room temperature it is plastic. That means that the mechanical built-in stresses, due to thermal mismatch with the other materials will relax and vanish over time. However, cyclical plastic deformations change the grain structure, weaken the solder fillet and can lead to fatigue. Such deformations occur e.g. in SMT (Surface Mount Technology) assemblies, please refer to Figure 3.16. The time until the solder fractures, depends on relative deformation (strain), temperature, frequency of deformation, etc., see Figures 3.17 a) and b). A simplified relationship is given by the Coffin-Manson´s formula [3.13]:

$N^{0.5} \times g_p = \text{constant},$

Where N is the number of cycles until fracture, and g_p is the relative deformation amplitude. In practice the relations are more complex. This can be explained by

the temperature changes that give rise to the deformations, and the material is plastic part of the time and elastic part of the time.

RESPONSE OF SOLDER TO STRAINS IN THE -65°C TO +125°C TEMPERATURE RANGE



- **FURTHER THE α- AND β- PHASES OF TIN-LEAD SOLDER HAVE DIFFERENT PROPERTIES, INCLUDING DIFFERENT EXPANSION COEFFICIENTS**

Fig. 3.15: Behaviour of solder metal at different temperatures, schematically. [W. Engelmaier].

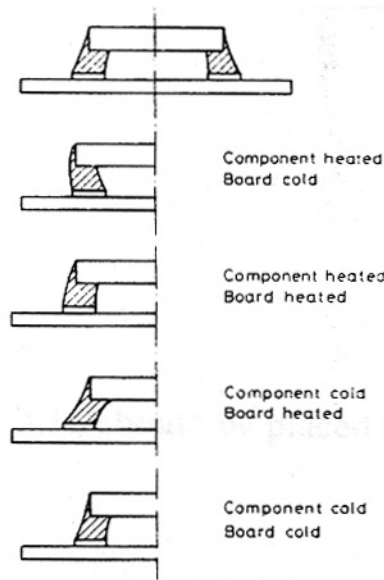


Fig. 3.16: Solder joint fatigue in surface mounted assemblies is often caused by power cycling.

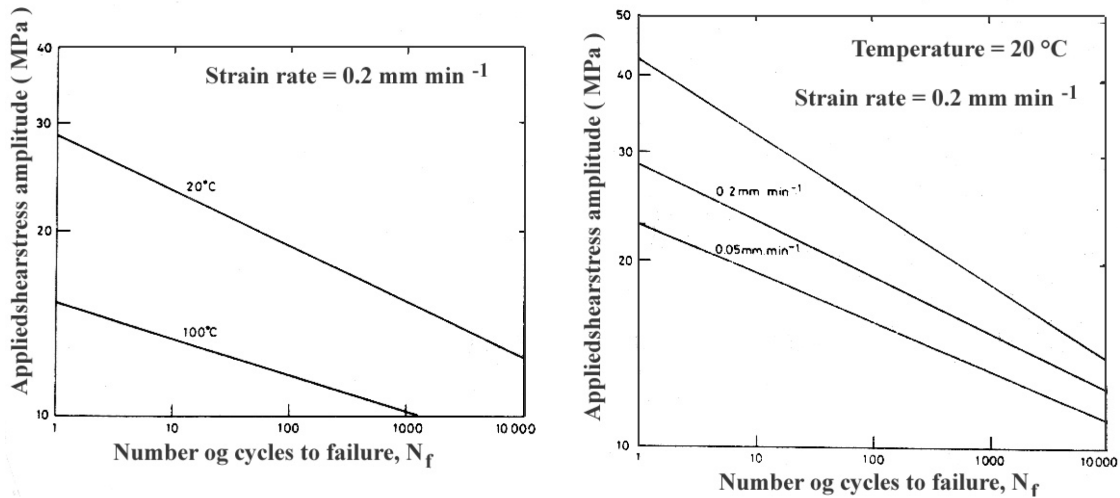


Fig. 3.17: Experimental data for fatigue in Sn/Pb solder fillet by cyclical mechanical stress. High temperature and low cycling frequency gives the fastest failure, because the grain structure relaxes most and is damaged [3.11].

SMD (Surface Mount Devices) resistors and capacitors often have silver in their terminals (please refer to Chapter 4), and the dissolution of the termination metal ruins the metallurgical and the electrical properties ("leaching" [3.11, p. 165]). For surface mounting it is therefore common to add 2 % Ag in the solder metal to impede the dissolution of silver into the solder metal, Figure 3.18. Another way to reduce the solubility is to alloy Pd or Pt into the silver in the component terminals.

Au in the solder metal may arise from Au component termination in certain component packages, please refer to Chapter 4. Gold dissolves very rapidly, as shown in Figure 3.18. It gives brittle, inter metallic $AuSn_4$ in the form of needles which weaken the mechanical strength in the solder fillet when the concentration is above 4 %.

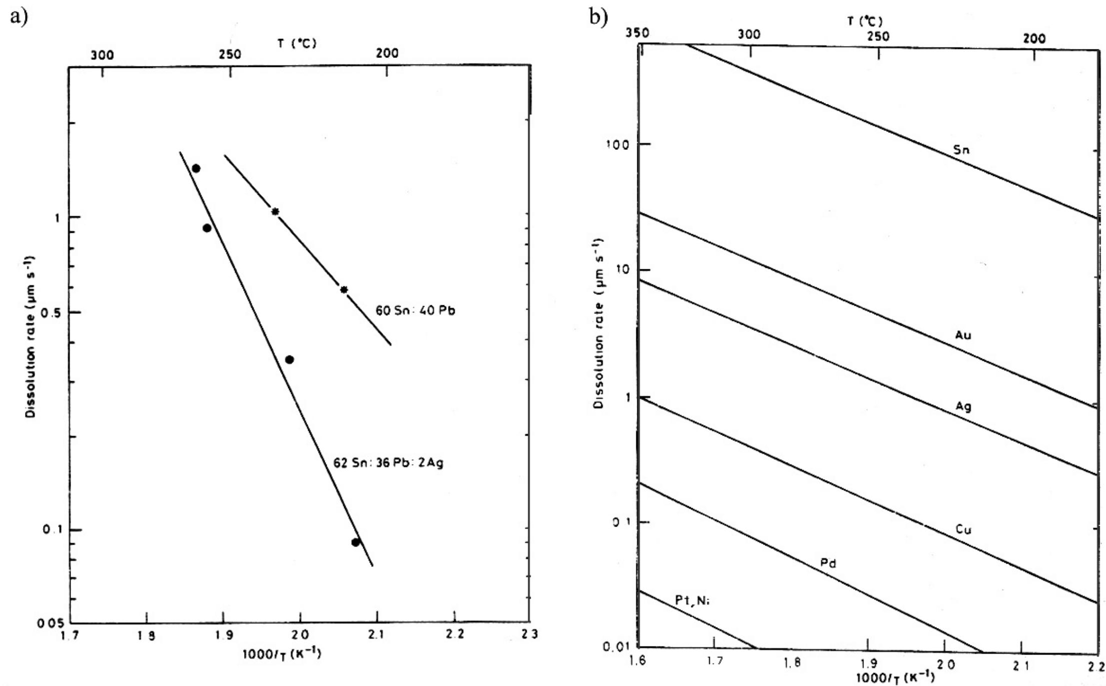


Fig. 3.18 a) Left: Dissolution rate of Ag in solder metal, and in solder metal with 2 % Ag, as function of temperature; b) Right: Dissolution rate of various metals in solder alloy [3.11].

Solder baths for mass soldering must be analysed periodically. Impurities such as Al, Zn, Cd change the properties of the solder metal and are not permitted above approximately 0.005 %. As, S, P are also harmful. Polluted solder metal is re-refined and used again.

For surface mounting solder metal in paste form is used for reflow soldering. This is described in Chapter 7.

Solder metal with a higher melting point may be useful for example for soldering of Si-chips (see below), when other components are to be soldered afterwards without melting the chip attached. 96.5 Sn:3.5 Ag, with a melting point of 221 °C is much used, and 5 Sn:95 Pb.

Solder metals with a low melting point can be obtained by adding In. They are also softer than normal Sn/Pb alloy, and they have better mechanical properties during thermal cycling. Properties of some important solder alloys are given Tables 3.6 and 3.7.

Table 3.7: Alloys for soft soldering [3.11]

Alloy System [mass%]						Code	Melting Temperature [°C]		Shear Strength at 1 mm min^{-1} [Nmm^{-2}]	
Sn	Pb	Ag	Sb	In	Bi		Solid	Liquid	20°C	100°C
100						Sn	232		22,1	19,0
63	37					Sn63	183	183	-	-
60	40					Sn60	183	188	33,6	21,6
50	50					Sn50	183	216	30,0	24,0
40	60					Sn40	183	234	34,3	13,7
10	90						275	302	28,9	14,7
5	95						310	314		
62	36	2				Sn62	179	179	43,0	18,6
10	88	2					268	299	-	-
5	93,5	1,5					296	301	23,8	15,7
96,5		3,5				Ag3,5	221	221	37,7	22,5
95			5			Sb5	236	243	37,2	21,1
	40			60		In60	174	185	-	-
	50			50		In50	180	209	-	-
37	37			25		In25	138	138	-	-
42					58	Bi58	139	139	50,0	19,5
15	33				52	Bi52	96	96	-	-
34	42				24	Bi24	100	146	34,3	17,5
43	43				14	Bi14	143	163	-	-

3.10.3 Flux and cleaning [3.11, 3.13, 3.14, 3.15]

Fluxes are used to improve the soldering and have several functions:
- Dissolve and remove harmful surface layers (oxide, etc.)
- Protect the surface against new oxidation
- Improve the wetting

Many types of flux are used. They consist of active ingredients dissolved in a liquid. They are of two main categories:
- Soluble in organic liquids
- Water soluble

The category determines how one will be able to clean the flux residues.

The common fluxes are also characterised as:
- Organic resin fluxes ("rosin")
- Organic non resin based fluxes
- Inorganic fluxes

Resin fluxes are most used and they contain natural resin from (pine-) trees, dissolved in alcohol, etc. It has a certain effect without additives, but it is normally "activated" by adding an organic chlorine compound: Dimethyl-ammonium chloride (DMA-HCl) or diethyl-ammonium chloride (DEA-HCl). The effect of the chlorine added is shown in Figure 3.19, while wetting of pure copper takes 6 seconds without activation, the time is below 1 sec. with 1 % Cl^- - content.

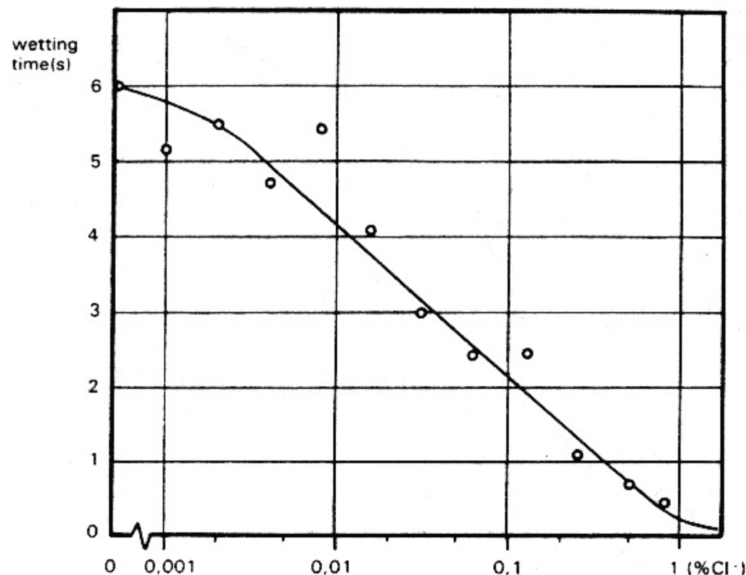


Fig. 3.19: Time for solder alloy to wet a pure Cu surface, depending on the activation of the solder flux. The degree of activation is given by the concentration of Cl^- ions in the flux (temperature: 230 °C) [3.13, page 232].

The following symbols/designations characterise the fluxes:

- R (Rosin, non-activated): Resin flux without chlorine added. It acts because of weak acids in the resin
- RMA (Rosin mildly activated): Up to 0.5 % Cl content
- RA (Rosin, activated): Higher content of chlorine

Chlorine is strongly corrosive, and if it remains on the surface after the solder process is completed it may give reliability problems later. A suitable cleaning process after soldering removes the residues. In many types of products it is accepted to use R and RMA flux without washing, but RA flux must be removed. All inorganic flux residues must also be removed.

Popular organic cleaning agents have been trichloro-trifluoro-ethane (Cl_3CCF_3 also designated TCTFE) mixed with an alcohol. One type is made by DuPont under the name Freon [3.13, page 45]. TCTFE has many good properties: It is efficient, does not burn, it is not poisonous and is chemically inert to most materials in electronics.

Like many other chlorine-fluorine-carbon combinations (CFC) TCTFE is very stable. Due to its low boiling point the vapour will spread in the atmosphere and the chlorine combinations will over long time break down the ozone layer [3.13, 3.14, 3.15].

TCTFE and similar combinations are now prohibited from use in most countries (the Montreal accord). Cleaning agents based on alcohol, cleaning with soap, etc. are replacements, and an extensive development work is taking place in fluxes that do not need to be removed. For certain purposes the soldering is performed in an inert or reducing atmosphere, without use of flux that has to be removed.

3.11 GLUING [3.11]

Gluing is used in electronics to:

- Assemble mechanical parts and keep electronic components in place
- Give electrical connection, as a replacement for soldering
- Give good thermal contact

The types of adhesives used are polymers, that generally are electrically and thermally insulating, often epoxy (or acrylic, phenolic, polyimide, etc.). Electrical conductivity and better thermal conductivity is achieved by adding conductive particles to the epoxy, most often silver (typically 85 weight %). It gives electrical resistivity in the region 1 - 10 x 10^{-6} Ohm•m, compared to 0.17 x 10^{-6} Ohm•m for the Sn/Pb solder alloy (room temperature). Improved thermal contact may also be achieved by mixing ceramic particles (Al_2O_3, AlN) into the adhesive. Thermal conductivity for epoxy without additives typically is 0.2 W/°C • m, and silver filled epoxy has up to 10 x higher value, see Tables 3.1, 3.4, Figure 3.20, and [3.16].

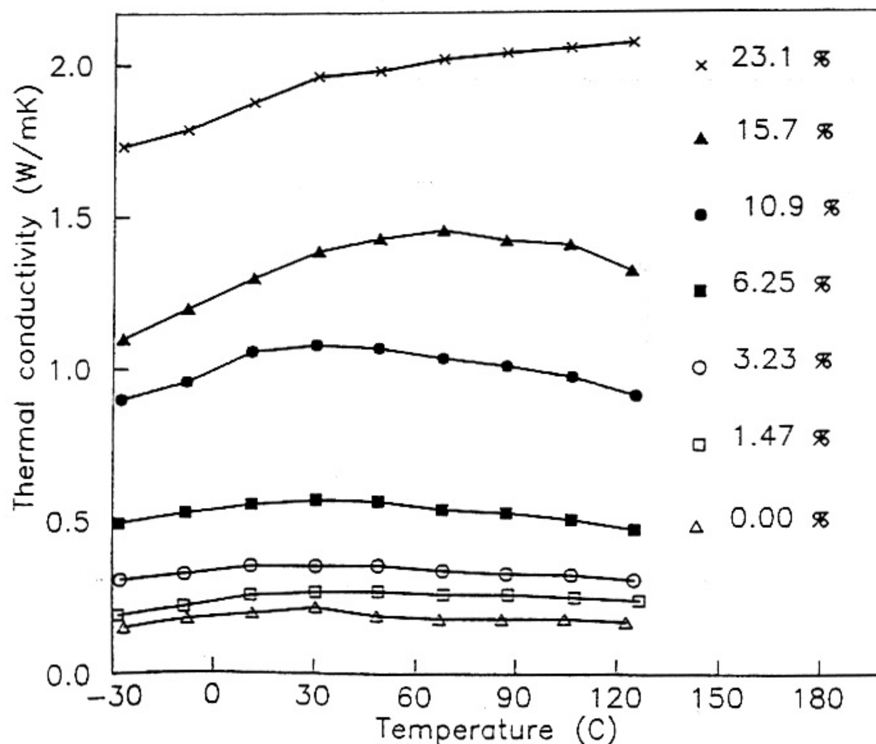


Fig. 3.20: Thermal conductivity of epoxy adhesive with various amounts of Ag [3.16 a)]. The concentration is in volume % Ag. (23 vol. % corresponds to approximately 80 weight %).

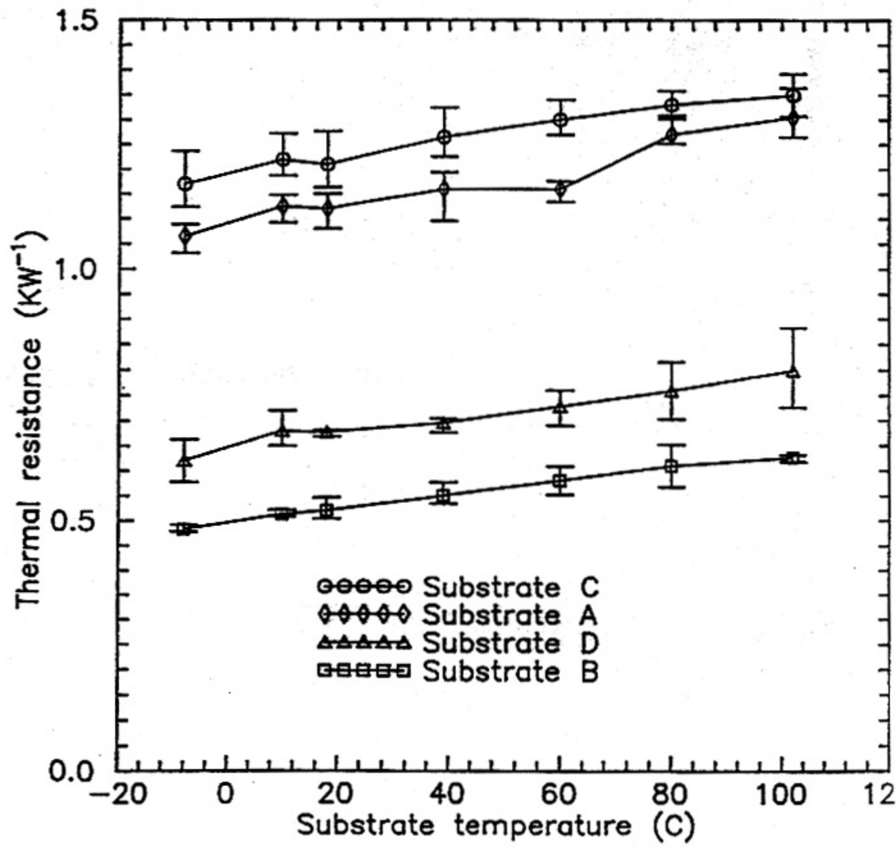


Fig. 3.21: The thermal resistance from the electronically active part, on top of the Si chip (¨junction¨) through a bonding layer of glue or soft solder and a thin alumina ceramic layer covered with Cu (¨direct copper bonding¨, please refer to Chapter 8) to heat sink. The samples with chips bonded by gluing, C and A, have approximately twice as high total thermal resistance as those which are soft soldered, D and B. Details are described in [3.16 c]

The adhesive is deposited by screen printing, dispensing, or in the form of a partly cured dry film cut to the right size, "preform". The curing takes place with heat, or by UV-radiation for certain types.

Replacement of component soldering by use of electrically conductive adhesives is an active topic of research. Gluing requires lower process temperature with less stress on the components and substrate, and we avoid the use of flux, cleaning and poisonous lead. Many researchers believe that better long term reliability can be achieved, because the adhesive is more elastic and deforms less than the solder metal. This work os not yet conclusive and gluing is not yet extensively used.

On the other hand the absorption of moisture in the adhesive polymer may reduce its strength as well as cause migration of the silver. Fine silver threads "grow" out from the silver particles in the presence of an electric field, and they can short circuit conductors in the neighbourhood.

For components with many closely spaced terminals the gluing may give lower failure rate than soldering during the mounting. "Anisotropically conductive adhesive" is used, screen printed over the whole area under the component. The adhesive has a low concentration of conductive particles, Figure 3.24, so that the probability of a short circuit horizontally between two terminals is negligible, but vertical contact between terminal and the substrate, through at least one particle, is virtually certain to occur. An interesting alternative method of contacting is to use insulating instead of conductive adhesive, please refer to Figure 3.24. By use of mechanical pressure during the curing, the adhesive is pushed away, and we get direct physical contact between terminal and substrate at points on the slightly non-uniform surfaces. The polymer shrinks during the curing and causes a permanent force that holds the materials together with good reliability [3.17]. These methods are particularly suitable for components with low current (such as LCD-displays).

3.12 MOUNTING OF THE SEMICONDUCTOR CHIPS: DIE BONDING

Before electrical connections are made to the chip, the chip must be mounted on the base by "die bonding". That takes place by a eutectic bonding, soft soldering or gluing. Important points with the die bonding are: High electrical conductivity if current runs from the chip to the substrate, good thermal conductivity if the chip dissipates much heat, mechanical strength and reliability. Die bonding may be a critical point in demanding applications.

3.12.1 Eutectic die bonding

Eutectic bonding takes place when an eutectic alloy is created between silicon and a metal system deposited underneath (or with a preform placed between the chip and the substrate). The melting point for the eutectic composition is much below that of the pure elements. Au/Si alloy is often used (melting point 363 °C at 96.7 Au:3.3 Si, while Au melts at 1063 °C, Si at 1412 °C) or 80 Au:20 Sn (melting point 280 °C).The process takes place in an inert atmosphere. Eutectic bonding gives very good electrical and thermal contact and high mechanical strength. However, it is very brittle and when the chips are large the thermal mismatch may cause the chip to crack during the bonding process or during thermal cycling later. Use of gold-rich alloys also makes it costly.

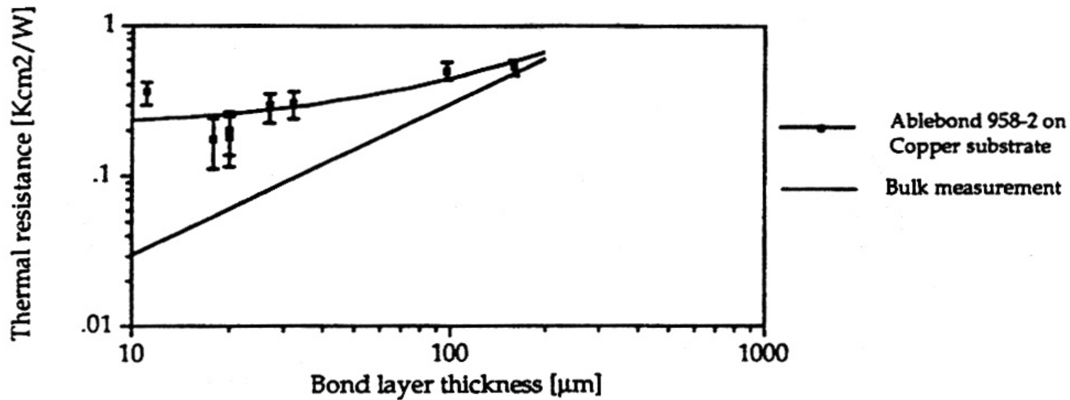


Fig. 3.22: Thermal resistance from junction to heat sink through adhesive of various thicknesses. For thick layers the resistance approaches the value calculated, based on the bulk thermal conductivity of the adhesive. For thin layers the resistance is higher, approaching a constant value, which indicates an "interface thermal resistance" caused by defects in the adhesive layer. For details, please refer to [3.16 b)].

3.12.2 Soft soldering

Soft soldering is used for large chips, particularly in power electronics, where good thermal and electrical conductivity is important. PbSn, AgPb, SnAgIn and other alloys are used. They are softer than the SiAu eutectic, the temperature in the process is lower and they can take up thermal mismatch by plastic deformation. They are more robust against fatigue than the common SnPb eutectic, but after many thermal cycles the soldering still may fracture due to fatigue.

The soldering of chips is made by screen printing of solder paste or by use of a solder preform. It takes place in inert or reducing atmospheres, without flux, to avoid gas pockets or flux residues that may corrode during long term use or which may cause hot spots in high power chips.

3.12.3 Gluing

Gluing is the dominating method of mounting. It is normally made with electrically and thermally conductive epoxy, see above. Cracks and damage due to thermal mismatch may be a problem with epoxy, but one can obtain soft types that are suited for large chips. One limiting factor for high power chips may be the poor thermal conductivity of the glue, see Figures 3.20 and 3.21, from [3.16 a) and c)]. Even when the adhesive thickness is made very thin there is evidence for an interface thermal resistance due to damage caused by the thermal mismatch between substrate and the Si chip, please refer to Figure 3.23 [3.16 b)]. During thermal cycling the adhesive will crack or lose its adhesion to the substrate and the Si chip, please refer to Figure 3.24 [3.16 d)], and the thermal resistance will increase further. The severity depends on chip size, temperature excursion and thermal mismatch between chip and substrate material, as well as the elastic modules and other properties of the adhesive. A different kind of chip gluing is done with silver filled low melting glass.

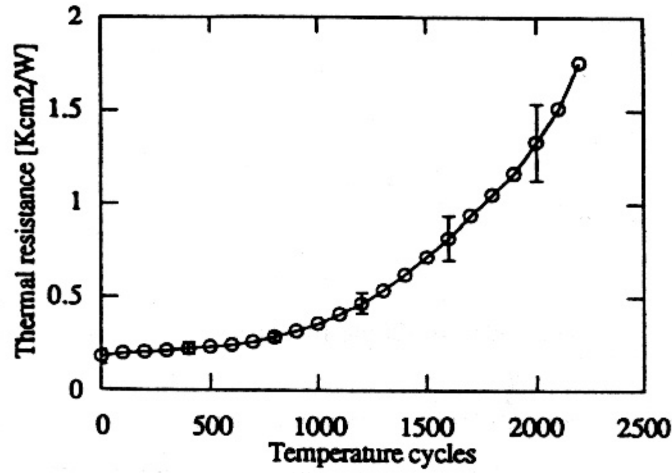


Fig. 3.23: Thermal resistance through an adhesive die bond between an Si chip and a Cu substrate, as a function of the number of thermal cycles between 10 °C and 150 °C. The increasing resistance is evidence of defects developing in the adhesive due to cyclic stress [3.16 d)].

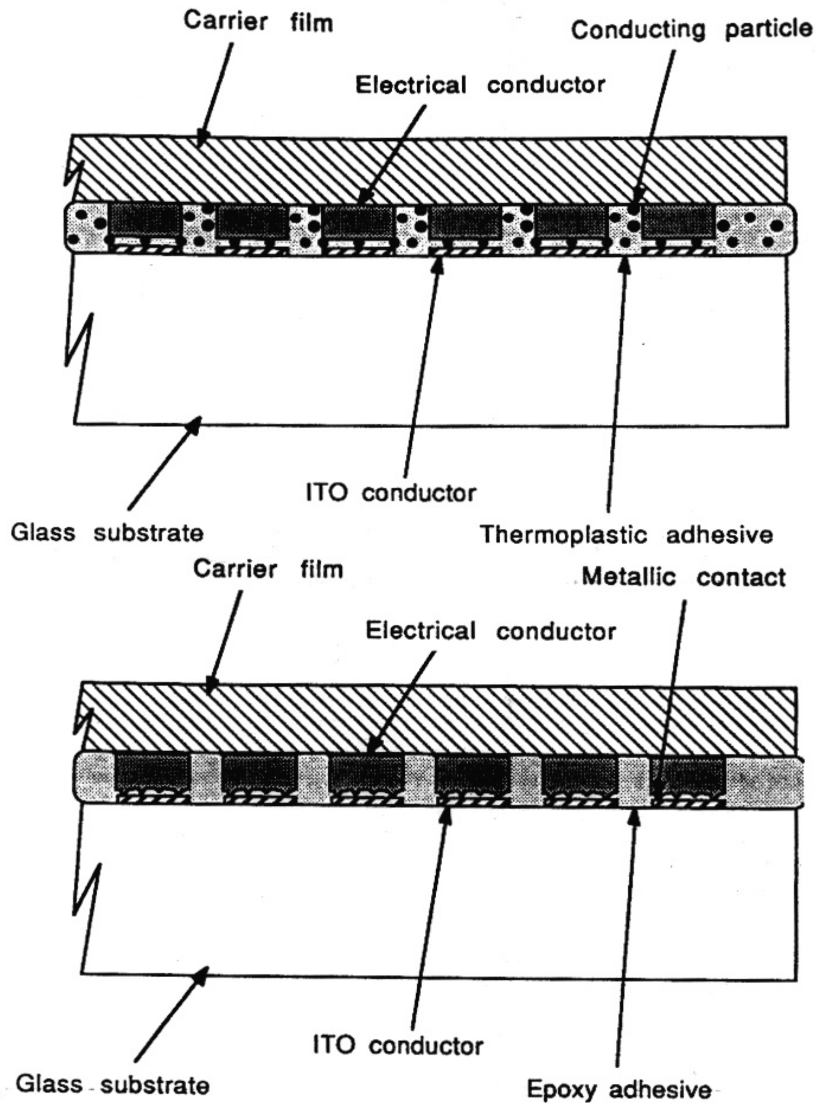


Fig. 3.24: Use of adhesive for contacting IC-chips with small pitch, schematically [3.17]: a): Anisotropic conductive adhesive, the conduction is through the metal particles in the adhesive; b): Electrically insulating adhesive, the conduction is through point contacts where the adhesive has been squeezed out.

3.13 WIRE BONDING

The most common methods for electrical connections to the semiconductor chip are mentioned in section 2.6: Wire bonding, tape automated bonding (TAB) and flip chip, see Figure 2.8. (In addition beam lead has been used for special purposes for many years [3.2].) Wire bonding is the dominating, well-established method and we will start describing this method.

Thin metal wires are connected one by one between the contact points on the semiconductor chip and the corresponding contact point on the substrate outside the chip. The wires normally are made of gold or aluminium, 0.025 - 0.5 mm in diameter. Al bond wire with rectangular cross section is also used. The substrate surface is normally covered on the bonding pads by soft (high purity) gold, deposited by plating or screen printing. The bonding wire is stretched out through the hole in a capillary tube. The connection to the chip is made by pressing the wire down onto the Al metallisation on the bonding area of the chip, against the edge of the capillary. There are several processes:

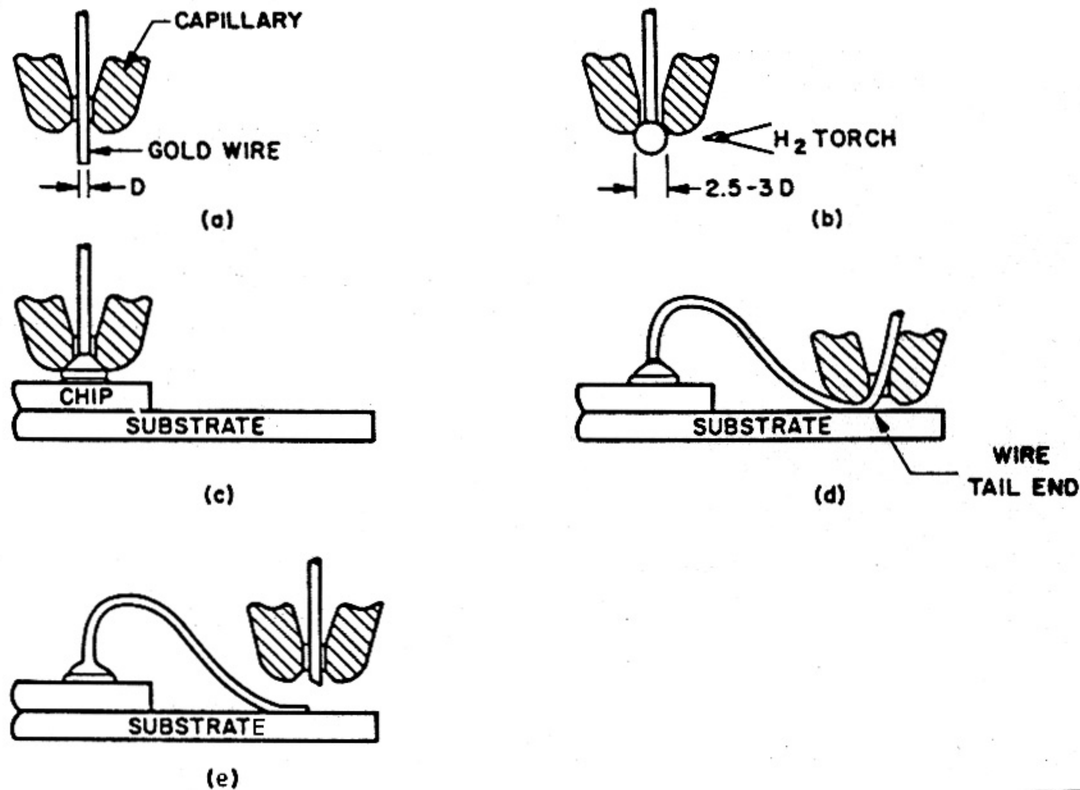


Fig. 3.25: The steps in wire bonding. a): The gold wire comes out of the capillary. b) A ball is created by melting the tip of the gold wire with a hydrogen flame. c) The ball is bonded to the Si chip with heat, pressure and possibly ultrasound vibration. d) The conductor is stretched and bonded to the substrate. e) The wire is torn off when the capillary is pulled up while the wire is held firmly inside the capillary.

- Ultrasonic bonding: Here the capillary vibrates with high frequency during the bonding, and the wire is cold-welded to the base by a combination of pressure and vibration. In addition to the softening of the gold, the vibrations also break up surface oxide layers. The technique is

used most for aluminium wire with flat ends on both sides ("wedge - wedge" bonding).

- Thermocompression bonding: The substrate and chip are heated to about 150 °C during the bonding process. This process is mainly used for gold wire, forming a gold ball at one side and a flat compressed wire end at the other side ("ball - wedge" bonding).

- Thermosonic bonding is a combination of the two previous methods.

The process steps in ball - wedge bonding are shown in Figure 3.25. The end of the gold wire that sticks out of the capillary is brought to melting with a hydrogen flame and it creates a small spherical ball. The capillary is moved down onto the aluminium bonding area on the Si chip, and it is pressed down, making the soft gold flat and sticking to the Al surface. The capillary is pulled up and it is moved over to the substrate bonding area, where it is pressed down and the bonding wire is squeezed flat. Then the capillary is pulled up, while the wire is held firmly inside the capillary and is torn off. The capillary is moved to the next terminal and the cycle is repeated.

Bonding machines are available as manual, semi-automatic and completely automatic units. The automatic machines have a camera for pattern recognition. Two registration marks on the chip are recognised by the camera and it tells the machine exactly where the chip is located. Two other registration marks on the substrate define exactly the position of the substrate relative to the chip. Teaching of the machine takes place in advance, whereby one programmes the co-ordinates for the registration pattern, and manually bonds one chip. The machine then learns the position of each bonding area relative to the registration patterns on both chip and substrate. The speed of machines used today is up to 10 bonds per sec. The failure rate may be less than 0.1 %.

Normal dimensions of the bonding areas are approx. 100 x 100 µm, and centre to centre distance 200 µm (pitch). It is possible to get down towards 60 µm pitch. Normally the bonding areas are in one row along the edges of the semiconductor chip, but it is possible to have two staggered rows without short circuiting the bonding wires. With a typical maximum chip size of today (over 20 mm side), there is an upper limit of approximately 1000 terminals for wire bonding.

A comparison between the properties for wire bonding, TAB and flip-chip is shown in Table 3.8.

Table 3.8: Comparison of wire bonding, TAB, and flip chip soldering [3.22]

Bonding technology	*Wire Bond*		*TAB*	*Flip-Chip*
Material(s)	Al	Au	Cu	Pb-Sn
Melting temperature [°C]	660	1064	1084	310
Bonding geometry	25 µm diameter x 2,5 mm length		25x100 µm tape x 2,5 mm length	125 µm diameter 100 µm height
Typical pitch [µm]	170 µm perimeter		200µm perimeter	250 µm area
Minimum Pitch [µm]	60 µm perimeter		70 µm perimeter	50 µm area
Strength per bond [gram]	6	10	50	30
Lead resistance [mOhm]	142	122	17	1,2
Interlead capacitance [pF]	0,025	0,025	0,006	<0,001
Lead inductance [nH]	2,6	2,6	2,1	<0,2
Thermal resistance [°C/mW] per bond	80	52	8	0,5
No. of I/Os per chip				
Typical pitch 8 mm chip size	184		160	1024
Minimum pitch 8 mm chip size	266		400	15150

3.14 TAPE AUTOMATED BONDING (TAB) [3.1, 3.2, 3.17]

When tape automated bonding is used a conductor pattern has been made in advance, fitting the semiconductor chip and the substrate bonding pad patterns, as described in Section 2.6, Figure 2.8. The conductor foil is on a carrier of polyimide film, please refer to Figure 3.26. The conductors are bonded to Au bumps on the chip.

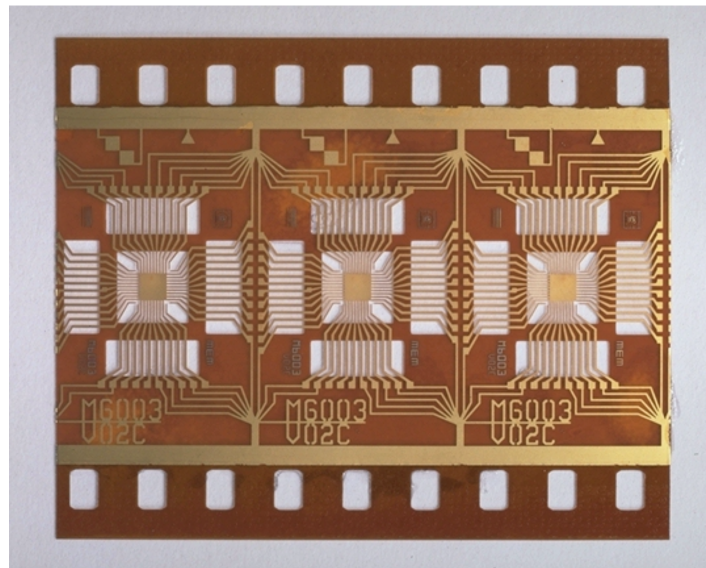


Fig. 3.26: A picture of a TAB film with the Cu pattern, as well as the holes in the film for excising the circuits, and the sprocket holes for moving the film during processing.

3.14.1 Process

There are a number of different varieties of TAB and TAB processes. Below we describe the most common type, please refer to Figure 3.27. Other alternatives will be commented on afterwards.

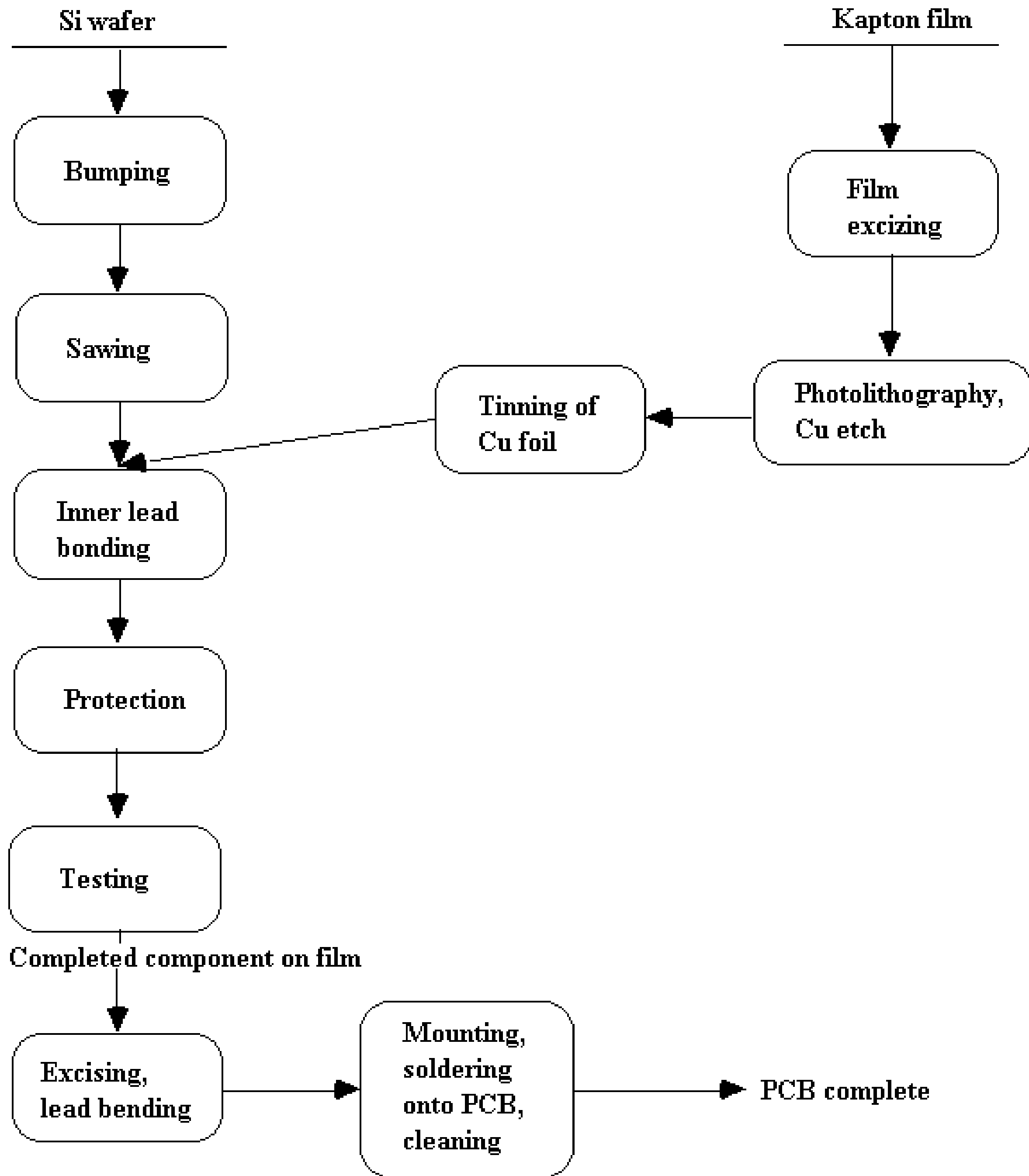


Fig. 3.27: The main steps in TAB processing.

Fabrication of gold bumps

Gold bumps are formed on processed Si wafers, please refer to Figure 3.28. First a metal system is deposited having the following functions:

- Covers the Si surface with a conducting layer, such that electrolytic plating can be used
- Prevents gold from diffusing into Al and Si (diffusion barrier)
- Gives better adhesion for the gold

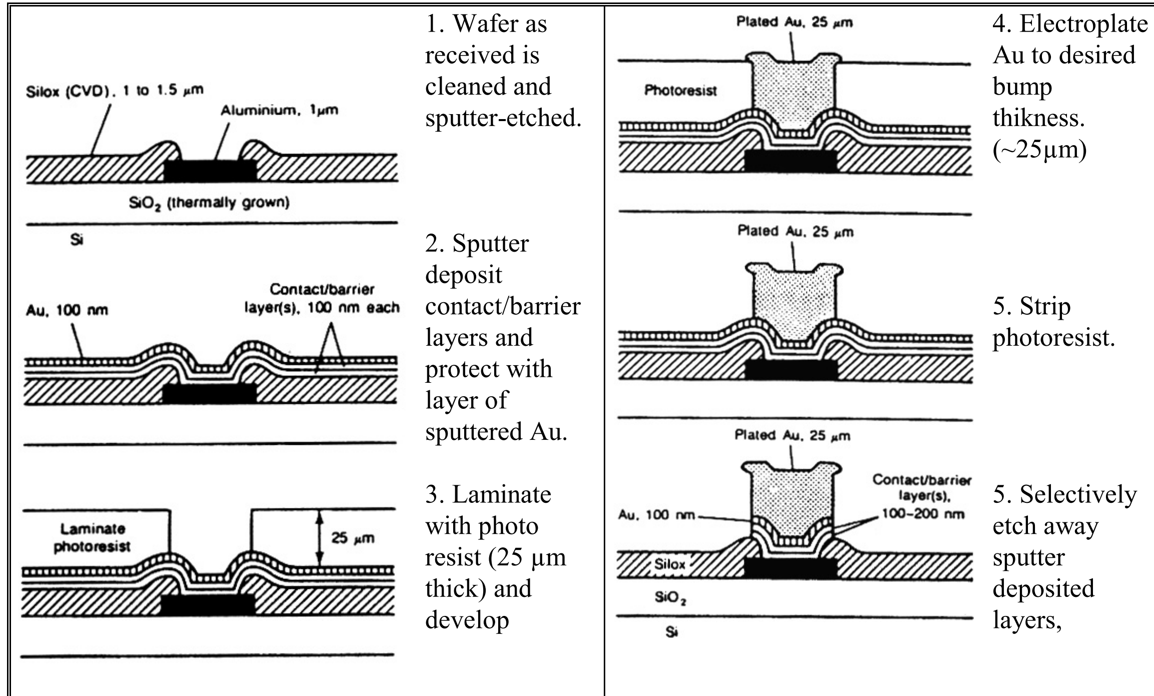


Fig. 3.28: The process for fabricating TAB bumps on the semiconductor chip [3.18].

For this the metal system Ti/Ni/W often is used (Approximately 1000 Å of each metal that is sputtered on).

Afterwards a layer of thick photoresist is deposited, openings at each bonding area are then made by photolithography and approximately 25 μm of high purity (soft) Au is electroplated with the photoresist as plating mask. Often the photoresist is thinner than this, and the gold bumps grow laterally and become greater at the top, in a characteristic mushroom shape. Then the photoresist is stripped, and the barrier metal system is etched off outside the gold bumps.

Then the wafers are cut into individual chips. The chips are now ready for inner lead bonding (ILB) of the TAB film with Cu pattern, which is made by its own process.

Fabrication of TAB film

The starting material for normal 3-layers TAB film is polyimide (often designated Kapton, which is DuPont´s trademark). Sprocket holes for handling, analogous to those on camera film, are punched along the edges of the film, as well as windows for the Si chip. Copper foil is laminated onto the polyimide, with an adhesive layer between. The conductor pattern in the Cu foil is defined by photoresist that is illuminated through a photo mask with the pattern on it.

Then developing follows and etching of the foil. The conductor pattern is tinned or gold plated. An example of such a pattern is shown in Figure 3.26.

35 mm wide film is the most common, with standard dimensions like for camera film. Also 8,16 and even 70 mm wide films are in use.

Inner lead bonding (ILB)

Inner lead bonding is the mounting of the semi-conductor chip onto the TAB film. It is normally performed by thermocompression bonding. The bonding tool, the thermode, see Figure 3.29, is of hard metal or diamond. It is pressing all Cu ends against the soft gold bumps simultaneously, "gang bonding". The process takes approximately 1 sec, at a temperature of 300-400 °C. A drop of epoxy is applied on to the chip for mechanical protection and environmental protection encapsulation. The chips may be tested with probes that contact the test points on the Cu conductor pattern on the TAB film.

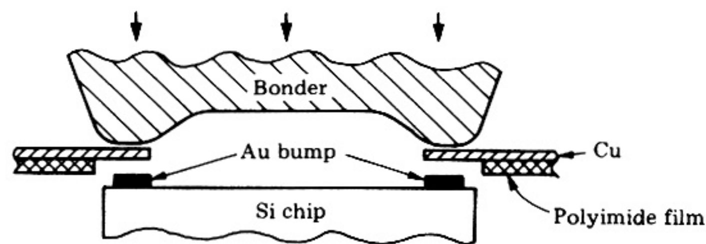


Fig. 3.29: Inner lead bonding.

The film with Si chips is rolled on to a reel. This is the stage where most users of TAB circuits buy them, regardless of whether they are standard or custom designed circuits.

Mounting, outer lead bonding (OLB)

The mounting of the TAB circuit on the printed circuit board consists of three steps:

- Excising of Si chip with short Cu conductors from the TAB film with a cutting tool that is made for the dimensions of that particular circuit.
- Bending of the leads, so that the outer ends are in the plane of the underside of the Si chip ("lead bending"), also with a dedicated bending tool.
- Placement of the chip on the printed circuit board and soldering the outer ends of the Cu leads.

The connections on the printed circuit board are normally made by pressing the copper lead ends down into solder paste or reflowed solder metal on the board. The soldering is most frequently performed with a "solder-iron" in the form of an electrically heated frame, this tool is also called thermode, for outer lead bonding. The frame solders TAB chips individually by pressing the Cu leads down into the solder metal and supplies heat by a pulse that lasts a few seconds. The process is called thermode soldering, impulse soldering or hot bar soldering, see Figure 3.30. The OLB thermode is cooled below the melting point before it is lifted up. The complete cycle takes 10 - 20 seconds.

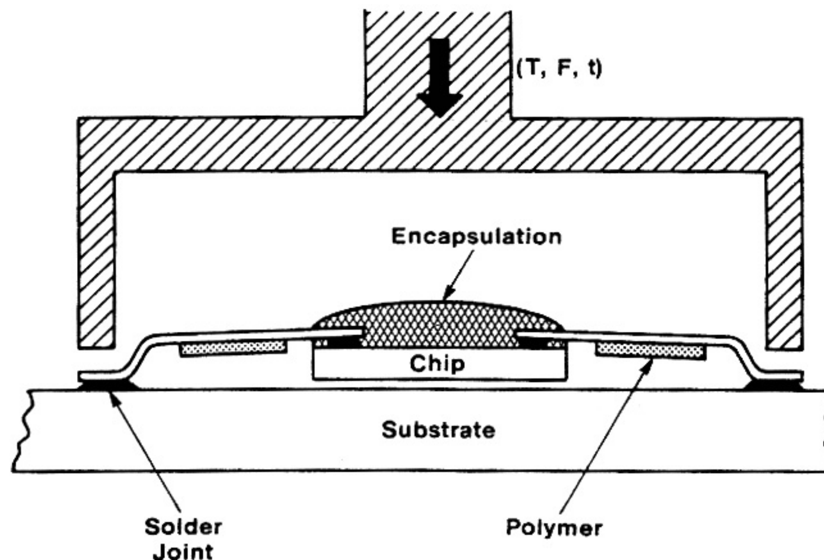


Fig. 3.30: Outer Lead Bonding (OLB) by thermode soldering.

3.14.2 Advantages and disadvantages of TAB technique

Some of the advantages of TAB are the following:

- It requires less bonding area for each contact on the semi-conductor chip, and smaller distances between the terminals than wire bonding. It therefore saves chip area at the same time as it makes it possible to interconnect chips with a larger number of terminals (up to approximately 1000).
- The outer lead bonding requires considerably less space on the printed circuit board than the same chip in a regular package and often less space than the same chip connected with wire bonding. The mounting is simpler and more robust than wire bonding.
- The gold bump on each bonding area gives a hermetic enclosure of the Al metallisation underneath. This reduces the possibility of corrosion, and the reliability is improved. Therefore TAB is suitable for use without additional encapsulation. (The epoxy drop mentioned above is still the most common.)
- The gang bonding operation is a more efficient process than wire bonding that is made one bond at a time, and has a higher production yield.
- TAB film can also be used as a separate, flexible little printed circuit board, on which it is possible to mount other components as well. (This is made e.g. in the Swiss Swatch watches, where all the electronics is on one TAB film.)

TAB is not yet extensively used, for the following reasons:

- It requires non-standard process of the Si chips (deposition of the gold bumps).
- It requires special fabrication of carrier film and conductor pattern that is costly and takes time.
- The mounting on the PCB requires special mounting equipment, and a separate tool for each individual component geometry. Individual mounting/soldering of each component is time consuming and costly.
- Repair (replacement of a defect component) on the PCB is demanding.

- Few standard circuits are available in TAB form. Few firms supply production on a subcontractor basis.
- There is little standardisation of dimensions and tooling, which increases the costs.

3.14.3 Alternative processes

Among the many alternative forms of TAB we may mention:

- The bumps can be made on the TAB film by plating ("bumped tape"), instead of on the Si chips ("bumped chip"). This simplifies the wafer processing, but the bumps of hard copper gives a more demanding inner lead bonding process and is a non-hermetic enclosure of the bonding area. It is also possible to make the Au bumps separately and transfer them to the wafer ("transfer TAB")
- One or two layer films: One layer film is only an etched Cu foil. It is not possible to test on the film, because all conductors must necessarily be interconnected and short circuited. One layer film has been in use for simple low price circuits for many years by National Semiconductor. Two layer film does not have a layer of adhesive. The Cu foil is plated on to the polyimide film instead of being laminated on.
- "Single-point bonding": For chips with a large area and many inputs and outputs a non uniform pressure on the contact points during gang bonding is a problem. This can lead to damage of the chip during inner lead bonding, or unreliable soldering for some of the terminals during outer lead bonding. Single-point bonding may be of help. The equipment for such bonding has a thermode that only touches and bonds one terminal at a time, then it moves to the neighbouring terminal. That also gives more process flexibility, because it can be programmed to bond accordingto the geometry of a new chip, without fabrication of a new thermode. However, the bonding requires long time and is very time consuming in large volume production.
- Area-TAB: Normally all contact points are along the periphery of the chip. For chips with many in-/outputs it may be very space saving to have contacts also at the inner parts of the chip area. This has been demonstrated for TAB, but it has not come into much practical use, because of process difficulties with the Inner Lead Bonding.
- Alternatives for Outer Lead Bonding: In addition to thermode soldering, IR soldering, vapour phase soldering, laser soldering and welding are used. Gluing is also used, please refer to Section 3.11.

Using the tape automated bonding technique one can easily process chips with less than 100 x 100 µm Al bonding areas, and 100 µm separation. With vertical walls on the Au bumps and advanced processing TAB technology has been demonstrated for a pitch between bonding areas of 50 µm, and more than 1000 terminals on the chip.

3.15 FLIP CHIP SOLDERING [3.1]

Direct soldering between the electrical contact points on the semi-conductor chip and points on the component substrate is designated "flip chip" because the chip is turned upside down, please refer to Section 2.4. "Solder bump" or C4 for "Controlled Collapse Chip Connection" (IBM's terminology) are other designations.

With this technology a bump of solder metal is formed on each bonding area on the silicon chip, please refer to Figure 3.31. The wafer is heated to reflow the solder metal and the chips are separated. Each chip is turned upside down and placed very accurately in position on the corresponding solder areas on the substrate. Then one heats up until reflow of the solder metal takes place again.

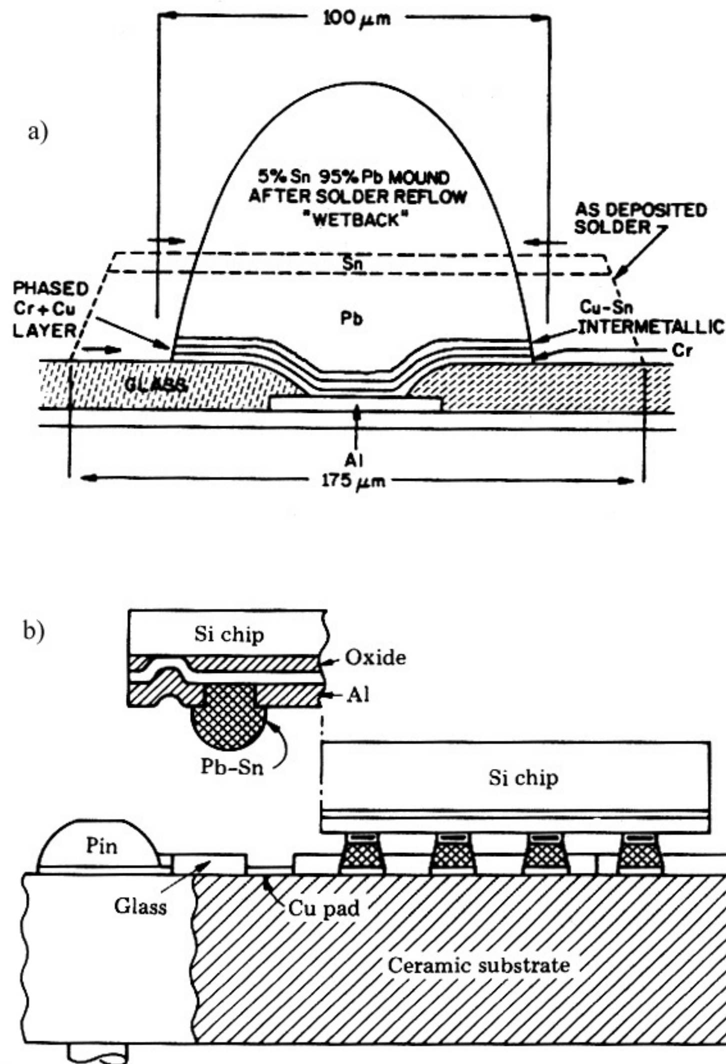


Fig. 3.31: Flip chip soldering: a): The metals for the solder bump before reflow (dashed lines) and after reflow; b): Bump before the soldering of the chip onto the substrate and after soldering.

A great advantage of flip chip is that one gets a placement on the substrate that does not require more space than the chip itself. In addition one can have terminals everywhere on the chip area, not only along the periphery. Flip chip soldering of chips with 10 000 terminals has been demonstrated. The electrical

properties are better than for other mounting methods, with low electrical resistance and low inductance, see Table 3.8.

The fabrication of the bumps takes place before the silicon wafer is cut. First a metal barrier layer is deposited, for example thin films of Cr/Cu/Au. Cr gives adhesion to the passivation on the Si chip around the Al metallisation. Cu gives a solderable surface, and a thin layer of Au prevents oxidation of the Cu. The solder metal may be 95 % Pb/5 % Sn (melting point approximately 305 °C), or an In alloy. It is deposited on the chip by sputtering or vacuum deposition through a metal mask with an opening for each bump, or by photolithography and electroplating, analogous to Au bump forming in TAB. For prototypes it is possible to place spheres of solder metal on to each terminal manually.

After deposition the solder metal is reflowed in a hydrogen atmosphere. This is done to homogenise the composition of the alloy, and to let the surface tension generate a spherical shape of the bumps. The reducing atmosphere removes oxides, which will otherwise ruin the solder ability. The bumps typically have diameter 100 µm.

The Si wafer is cut, and the chips are ready for mounting. That is done by turning them upside down as mentioned, and placing them accurately on the substrate, which is heated to reflow again. Water- or resin-based flux is used, but the subsequent cleaning is very critical. A certain amount of self-alignment is achieved because of the surface forces in the molten solder metal, which try to move it to the location where the total surface in all solder joints is a minimum. That is where the position is perfect.

A problem with flip chip soldering is the lack of thermal flexibility, because of the short "conductors" between chip and substrate. Therefore it is best suited for silicon substrate or for small chips on Al_2O_3 or AlN substrate. The heat conduction is not so good, unless one also has a thermal contact to the back side of the Si chip, please refer to Chapters 4 and 8.

IBM has used flip chip soldering since 1964, but few other companies have used the method in volume production until the last years. Areas of application today are mostly for multichip modules in computer- and telecommunication applications where extreme performance and minimum space are required.

3.16 PLANAR BONDING WITH ADAPTIVE ROUTING [3.2, 3.21]

For future complex semiconductor circuits there is a need for several thousand in- and outputs with a higher density than even flip chip can provide. An interesting method that is under development is called "planar bonding". In one version [3.2, page 308] a silicon wafer with crystallographic orientation (100) is used as substrate, see Figure 3.32. Holes are made in the wafer by anisotropic etching for all the ICs that are to be mounted. The chips are glued in from the back side, such that the surface with the conductor pattern is planar with the substrate surface. (Alternatively a ceramic substrate may be used with holes or cavities.) Thereafter a polyimide film is deposited all over the surface, via holes to the chip pads are laser "burned", and thereafter a conductive layer of titanium or chromium is deposited by sputtering.

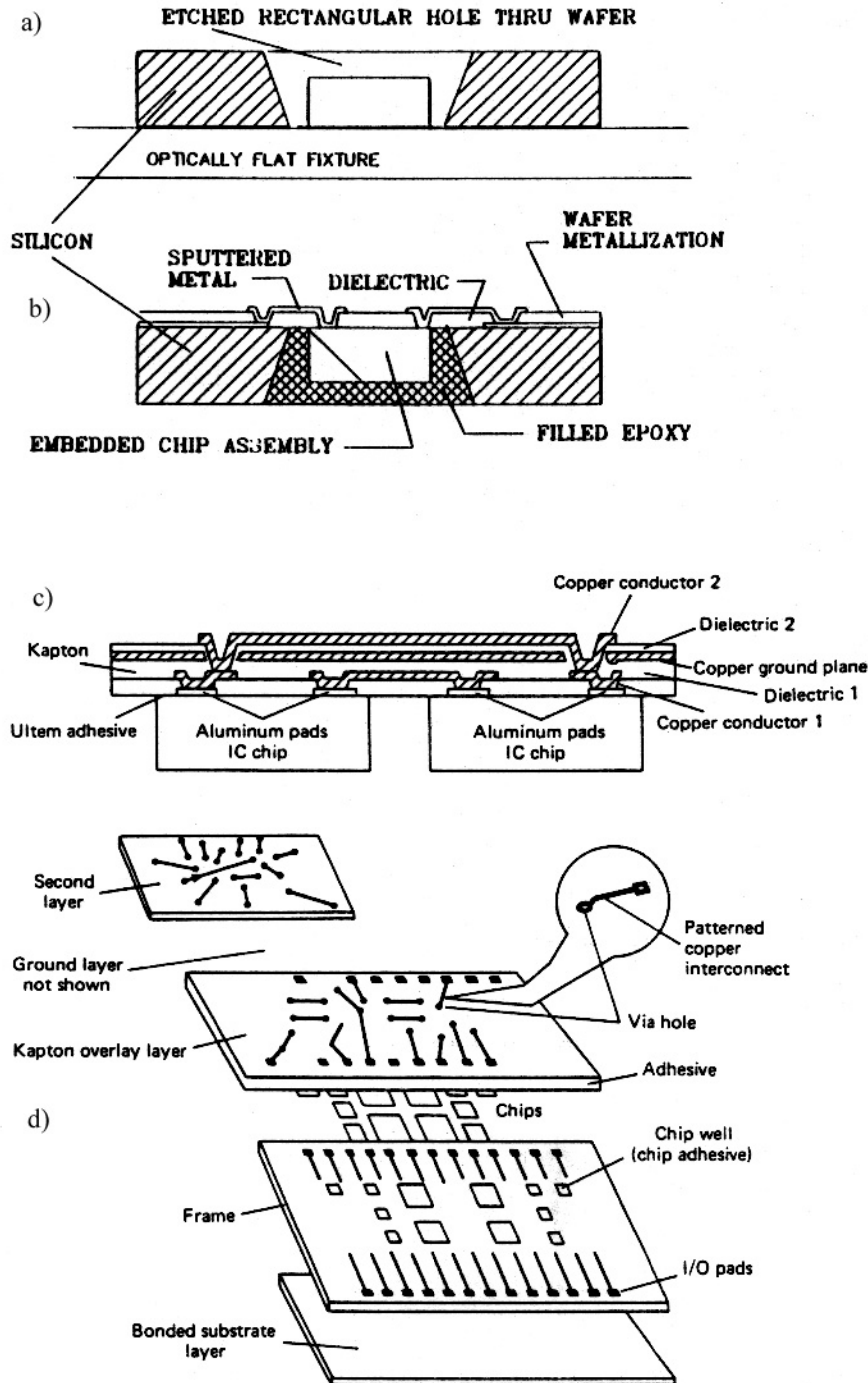


Fig. 3.32: Planar bonding with laser-assisted adaptive conductor routing. The top two figures a) and b) show a substrate cross section with details of the mounting of the chip in an etched through-hole. Figure c) shows the conductor layers and polyimide insulation on top of the substrate. The bottom figures show an exploded view of all the layers [3.20, 3.21].

Electroplating of copper is then performed to increase the thickness of the conductive layer, and the conductive paths are patterned by photolithography by direct laser writing. Photolithography and etching of the conductor pattern must be adjusted to each chip and each substrate because of the deviation in the IC chip placement. That is done as follows: The wafer is covered with positive

photo resist. An electronic vision system recognises the substrate interconnection points and the IC interconnection points, and gives information to a laser that illuminates selectively the path from each substrate interconnection point to the corresponding chip interconnection point. The photo resist is cured where the laser has illuminated it, and removed by the development process elsewhere. In the subsequent etching process the metallisation is removed on the rest of area. This is called "adaptive routing".

A second layer of conductive paths can be implemented by spin coating of polyimide with laser burning of vias and deposition of a new conductive layer, which is then patterned. This can be repeated for new layers until the required interconnect routing is achieved.

This method is under development at Auburn University, General Electric and other places and may be capable of giving interconnections with a pitch of a few tens of µm. It has the potential to be both flexible in production, give excellent electrical characteristics and give high packaging density.

REFERENCES

[3.1] R.R. Tummala and E.J. Rymaszewski: "Microelectronics Packaging Handbook". (van Nostrand Reinhold, 1988.)

[3.2] ASM International: "Electronic Materials Handbook, Vol. 1, Packaging". (1989.)

[3.3] S.M. Sze:
a): " Technology". (McGraw Hill, 2nd Ed.1988.)
b): "Physics of Semiconductor Devices". (Wiley, 2nd Ed. 1981.)

[3.4] R.C. Buchanan: "Ceramic Materials for Electronics". (Marcel Dekker, 1986.)

[3.5] L.M. Levinson: "Electronic Ceramics". (Marcel Dekker, 1988.)

[3.6] M.T. Goosey: "Plastics for Electronics". (Elsevier, 1985.)

[3.7] G. Leonida: "Handbook of Printed Circuit Design Manufacture, Components and Assembly" (Electrochemical Publications, 1981.)

[3.8] J.J. Licari and L.R. Enlow: "Hybrid Microcircuit Technology Handbook". (Noyes Publications, 1988.)

[3.9] D.P. Seraphim et at.: "Principles of Electronic packaging". (McGraw-Hill, 1989.)

[3.10] See e.g.: D.E. Riemer: "Analytical engineering model of the screen printing process", parts I and II. Solid State Technology Aug. and Sept. 1988.

[3.11] C. Lea: "A Scientific Guide to Surface Mount Technology". (Electrochemical Publications, 1988.)

[3.12] C.I. Wall: "Screen printing in the Printed Circuit Board Industry". Circuit World vol. 12, No. 3, 1986, page 36.

[3.13] R.J. Klein Wassink: "Soldering in Electronics". (Electrochemical Publications, 2nd Ed., 1989.)

[3.14] B.N. Ellis: "Cleaning and Contamination of Electronics Components and Assemblies". (Electrochemical Publications 1986.)

[3.15] a): Truls Koch et al.: "Methods for Clean Electronics". EPF report R-45 (Feb. 1991, in Norwegian.)
b): C. Lea: "After CFCs - Options for cleaning electronic assemblies". (Electrochemical Publications 1991.)

[3.16] A. Bjørneklett, L. Halbo and H. Kristiansen:
a): "Thermal conductivity of epoxy adhesives filled with silver particles". Int. J. of Adhesion, vol. 12, no. 2, April 1992, p. 99.
b): "Investigation of the Thermal and Mechanical Properties of Die Bonding Adhesives". Proceedings IEPS 1992, p. 509.
c): "Hybrid Substrates for Power Electronic Applications: An Investigation of Thermal Resistance and Mechanical Stress". Hybrid Circuits, vol. 30, Jan. 1993.
d): "Thermal Resistance, Thermomechanical Stress and Thermal Cycling Endurance of Silicon Chips Bonded with Adhesives". Proceedings Semitherm 1993.

[3.17] H. Kristiansen and A. Bjørneklett: "Fine pitch connection of flexible circuits to rigid substrates using non-conductive adhesives". Proceedings IEPS 1991, p. 795.

[3.18] J.H. Lau et al.: "Overview of Tape Automated Bonding Technology". Circuit World, vol. 16, no. 2, 1990, p. 5.

[3.19] L. Halbo:
a): "Tape Automated Bonding", EKF report R 44 (1986, in Norwegian).
b): "Tape Automated Bonding - Analyses and Case Studies", Nordic Industry Fund report (March 1987, in Norwegian).

[3.20] R.C. Landis: "Electronic packaging for the year 2000". Proceedings IEPS 1990.

[3.21] See e.g.:
a): R. Hartley et al.: "Rapid prototyping using high density interconnect". European Design Automation Conference, Glasgow, March 1990.
b): R.O. Carlson & al.: "A High Density Copper/Polyimide Overlay Interconnection". Proceedings IEPS 1988, p. 793.

[3.22] S. T. Riches: "Packaging Options for High Lead Count ASIC Devices". Hybrid Circuits, vol. 23, Sept. 1990, p. 14.

[3.23] F.N. Sinnadurai: "Handbook of Microelectronics Packaging and Interconnection Technologies". (Electrochemical Publications, 1985.)

[3.24] C. P. Wong et al.: "Understanding the Use of Silicone Gels for Nonhermetic Plastic Packaging". IEEE Trans. CHMT, vol. 12, no. 4, Dec. 1989, p.421, and IEEE Gel Task Force Reports in IEEE Trans. CHMT.