CHAPTER 4

COMPONENTS FOR ELECTRONIC SYSTEMS

4.1 INTRODUCTION

The components and the component technology are of great importance for performance, reliability, space needed, and cost of electronic systems. They also are important in determining the production process for modules and PCBs(Printed Circuit Boards). In this chapter we shall describe the properties of the most important passive components and IC packages. The electronic functions of ICs, however, are outside our scope.

The American organisation JEDEC (Joint Electronic Device Engineering Council) has recommended standard dimensions for many components. Standardisation is extremely important.

4.2 RESISTORS

4.2.1 Hole mounted resistors

Hole mounted resistors generally have cylindrical body, with axial leads, Fig. 4.1. There are three main types:

- Carbon composite, with a massive body of conductive carbon in a matrix of insulating material. Resistor values are between 1 ohm and 100 Mohm, maximum power dissipation 1/8 - 2 Watt, depending on the physical size. The temperature coefficient of resistance is high (~500 ppm/°C), the stability is low, and the resistance tolerance is 5, 10 or 20%.
- Wire wound, with insulating body. Metal wire, e.g. NiCr, is wound on the body and covered by insulation. Range: 1 - 100 Kohm, low temperature coefficient (~70 ppm/°C), tolerance 0.1 - 0.5 %, high stability.
- Film layer resistors have a thin film of metal, tin oxide or carbon, possibly with a spiral cut to increase the resistance. Resistance values ≤ 1 ohm to ≥ 1 Mohm, temperature coefficient 20 - 250 ppm/°C. Low tolerance can be obtained by trimming.

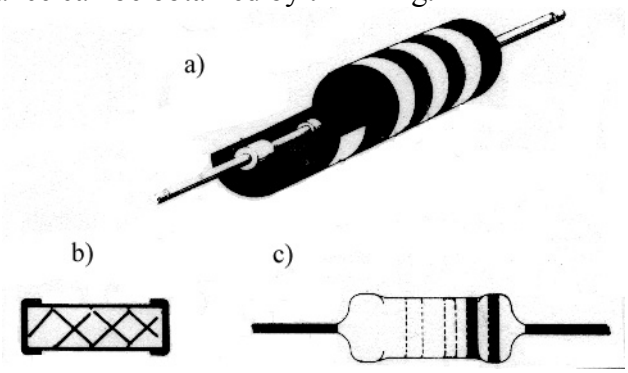


Fig. 4.1: Hole mounted resistors: Carbon composite, wire wound and metal film types.

4.2.2 Surface mounted resistors

SMD resistors normally have a rectangular body made of ceramic, Fig. 4.2 a). The resistor material may be ruthenium oxide. It is printed on in paste form and cured at high temperature by thick film methods (Chapter 8), and laser trimmed to correct value. On top is a protective layer of insulating glass. The component has no leads but electrical terminals at the ends. The inner electrode material is Ag or Au. The outside electrode material is AgPd or a diffusion barrier of Ni with SnPb solder on top, Fig. 4.2 b). The manufacturing process is described in [4.3, 4.4]. The purpose of the Ni layer is to prevent Ag from being dissolved in the outer metal, as Ag dissolves fast in Sn and Sn/Pb solder, please refer to Chapter 3.

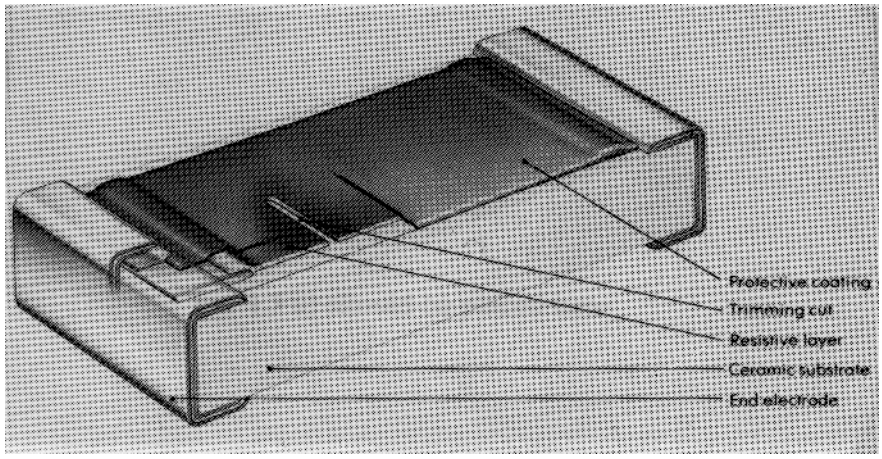


Fig. 4.2 a): Surface mounted resistor, rectangular shape.

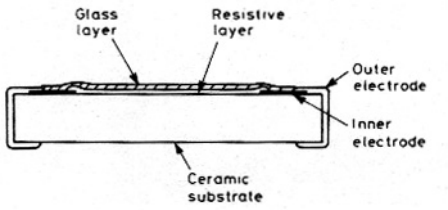


Fig. 4.2 b): Metal system for termination on SMD resistors.

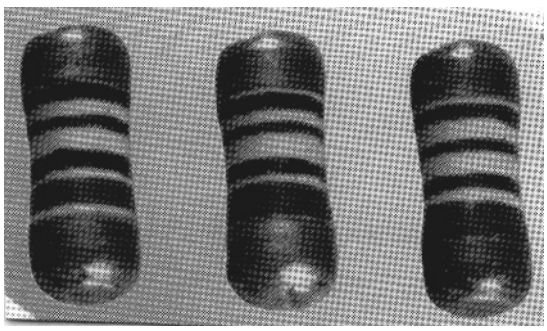


Fig. 4.2 c): MELF-resistors have cylindrical body.

SMD resistors are also made in cylindrical form, called MELF (metal electrode face bonding), see Figure 4.2 c). This component has metal plates at the ends, coated with solder.

The temperature coefficient of resistance is typically below +/- 200 ppm per °C, tolerance +/- 1 - 20 %. The most common rectangular sizes are denoted 1206 (0.12" x 0.06 ", or 3.2 x 1.6 mm) and 0805. There are smaller sizes: 0603 is extensively used, and 0402 is emerging. Maximum power dissipation for 1206 is 1/8 or 1/4 Watt. Higher power resistors have larger bodies. Resistor values range from < 1 ohm to approximately 10 Mohms. A "zero ohm" component has resistance around 50 Mohms and is used as a "jumper" to contact two conductors on the PCB with other conductors between.

Typical properties of SMD resistors are shown in Table 4.1.

Table 4.1. Properties of SMD resistors (Philips).

Resistance range and tolerance	10 ohm to 1 Mohm (E24* series) ± 2% 1 ohm to 10 Mohm (E24 series) ± 5% 1 ohm to 10 Mohm (E12 series) ±10%
Dimensions	3,2 x 1,6 x 0,6 mm
Operating temperature range	-55°C to + 155°C
Temperature coefficient (-40°C to 125°C)	$<+200 \times 10^{-6}/K$
Absolute max. dissipation at T_{amb}= 70°C	0,25 W
Maximum permissible voltage	200 V (r.m.s.)
Climatic category (IEC68)	55/155/56
Jumper resistance	≤ 50 mohm
Maximum current	2 A

*See Table 4.2

Table. 4.2: The resistance series E24, E12 and E6. The numbers mean that for example in series E6 there are 6 resistance values for each decade: 10, 15, 22, 33, 47 and 68 $x10^n$ ohms.

E24	10	11	12	13	15	16	18	20	22	24	27	30	33	36	39	43	47	51	56	62	68	75	82	91
E12	10		12		15		18		22		27		33		39		47		56		68		82	
E6	10				15				22				33				47				68			

4.3 CAPACITORS

In addition the capacitance, the following properties are important for the area of application of capacitors:

- Maximum voltage rating
- Temperature dependence of the capacitance (temperature coefficient)
- Loss tangent (tan δ), see below
- Equivalent series resistance
- Long term stability and ageing phenomena
- High frequency properties
- Leakage current
- Ability to withstand various production processes (high temperature, etc.)
- Price, physical size, etc.

There are many types of capacitors, and the choice depends on the relative importance of these factors for the given application.

4.3.1 Electrical model

An ideal capacitor consists of two electrodes of area A, with a perfect insulator between them, of thickness d and relative dielectric constant ε_r :

$$C = \varepsilon_o \varepsilon_r \times A / d$$

Practical capacitors can be described by models like the one in Fig. 4.3. Deviations from the ideal are represented by series resistance R_s, parallel resistance R_p, and inductance L. The various parasitics dominate at different frequencies.

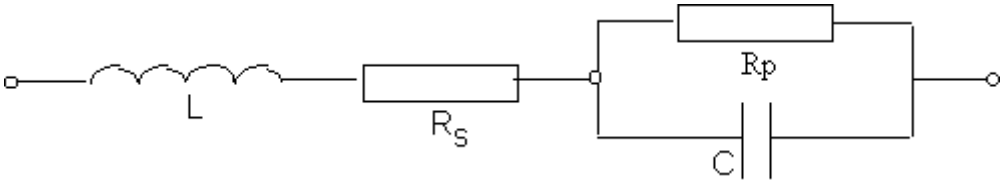


Fig. 4.3: Electrical equivalent model for capacitor.

If R_p can be neglected the impedance is given by:

$$/Z/ = [R_s^2 + (\omega L - 1/\omega C)^2]^{1/2}.$$

Examples of the frequency dependence are shown in Figure 4.4. It shows a resonant behaviour with Z_{min} at the frequency where $\omega L = 1/\omega C$. Above this frequency the capacitor behaves more like an inductor.

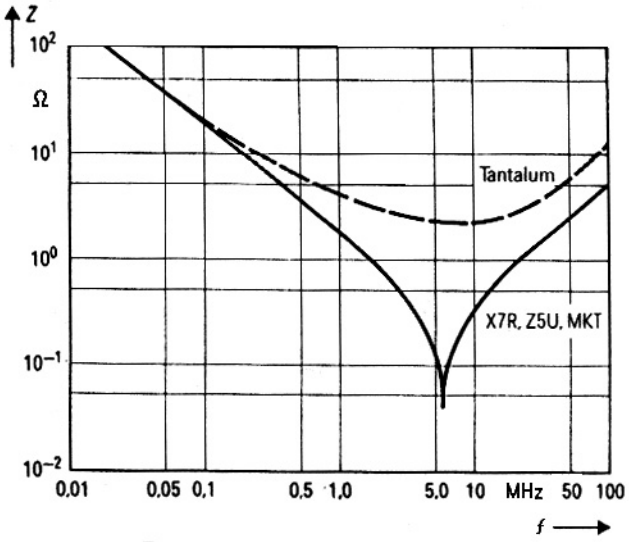


Fig. 4.4: The frequency dependence of impedance for multilayer ceramic capacitors (below) and tantalum electrolytic capacitors (top), all having 100 nF capacitance value [4.5].

The loss tangent is of special importance. It is defined as the ratio between the resistive and reactive parts of the impedance (please refer to Section 3.2.3):

$$\tan \delta = R \,/\, /\mathrm{Im}\, Z/ = [R_p + R_s\,(\,1+(\,\omega C R_p)^2)\,] \,/\, (\,\omega C R_p^2 - \omega L\,(1+(\,\omega C R_p)^2)\,].$$

Schematically tan δ will depend on the frequency as shown in Figure 4.5. Most capacitors have a constant loss tangent over a large frequency interval, where they are normally used.

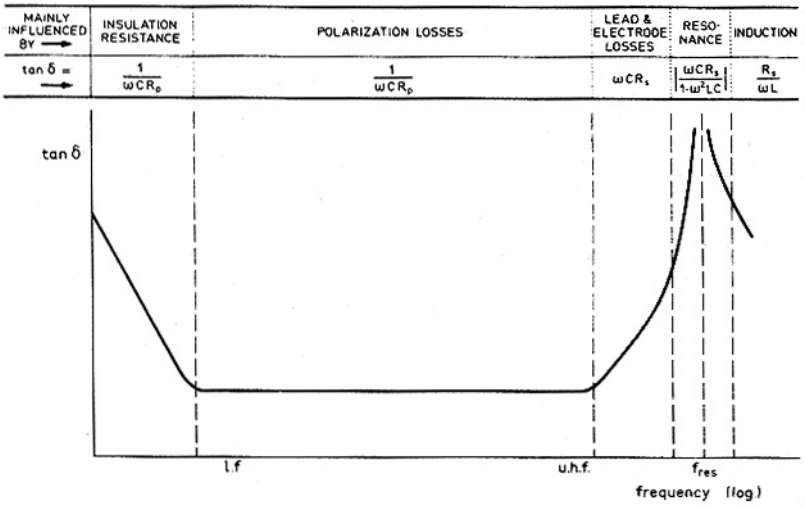


Fig. 4.5: Frequency dependence of the loss tangent tan δ schematically (Philips data book).

4.3.2 The main types of capacitors

Capacitors are of the following types:

- Ceramic multilayer
- Electrolytic, dry and wet
- Metallised plastic film dielectric (polyester, polystyrene, etc.)
- Mica.

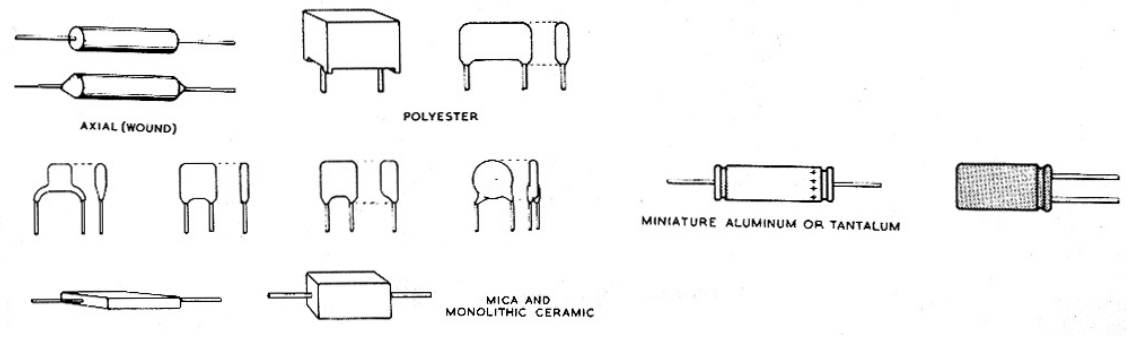


Fig. 4.6: There is a large spectrum of hole mounted capacitors. To the left some types of dry capacitors: axial metal/plastic film, ceramic, mica, and to the right aluminium and tantalum electrolytic capacitors.

All types are made in hole mounted as well as surface mounted (SMD) versions. The main difference is the body shape and the electrode form. We shall focus on the SMD versions. However, Figure 4.6 shows some examples of the shapes of hole mounted capacitors.

4.3.3 Multilayer ceramic capacitors

Ceramic multilayer capacitors, see Figure 4.7, are the dominating type for SMD. They are composed of a number of metal electrodes, isolated from each other by thin layers of a ceramic dielectric. Every other electrode is connected to the end termination on the left and the right side. The dielectric layers are only of the order 20 μm thick, and the dielectric may have a very high relative dielectric constant. Thus, one achieves very high capacitance to volume ratio. The capacitors are manufactured by processes similar to those used for making multilayer ceramic packages and multichip modules, please refer to Chapters 3 and 8 and [4.2, 4.3, 4.6, 4.8]. Due to the high temperatures used during sintering the inner electrodes are normally made of the noble metals Pt or Pd, which have a high melting point. The end electrodes are AgPd or Ag, see Figure 4.7, and a diffusion barrier of Ni outside it, and on top of that, a eutectic composition of SnPb solder. See also Section 4.7.

The ceramic dielectrics are of different types. Designations and compositions vary between manufacturers, but properties are similar. The dielectrics are divided into classes according to relative dielectric constant and other properties. The ceramic is often based on barium- or strontium titanate with additives. These materials are ferroelectric, therefore the high dielectric constant, please refer to Figure 4.8. Near the Curie temperature ε_r is strongly temperature dependent, and the purpose of the additives is to move the Curie point or in other ways reduce the temperature dependence in the temperature region of use.

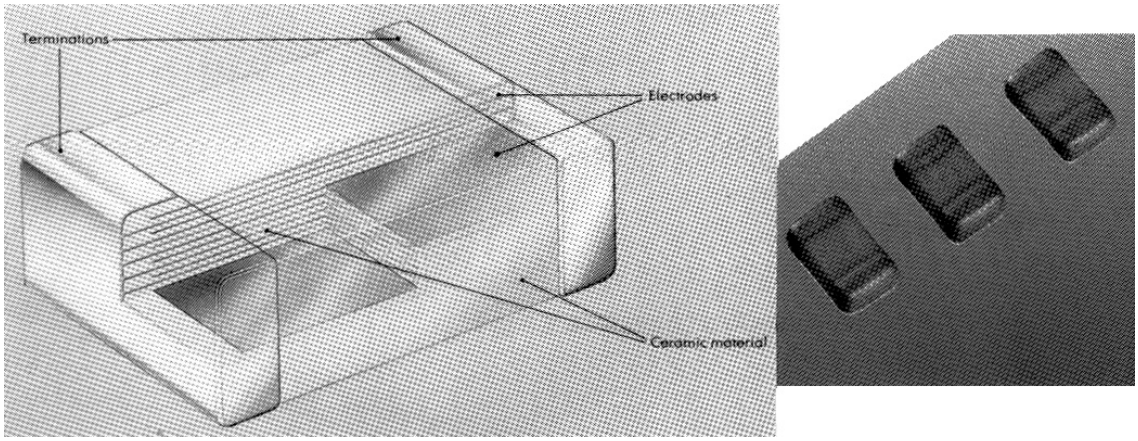


Fig. 4.7 a): SMD multilayer ceramic capacitor.

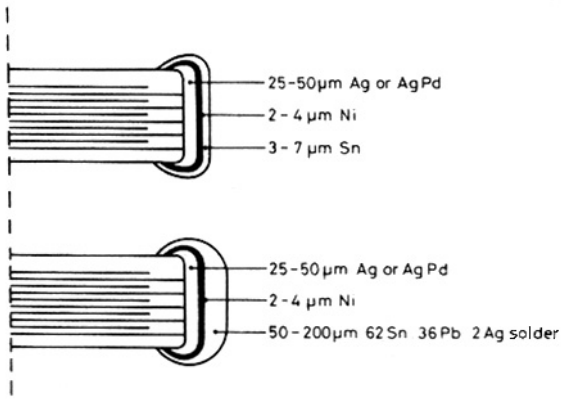


Fig. 4.7 b): Metal system for the end termination of multilayer ceramic capacitors.

There are two main classes of ceramic capacitors [4.8]:

Class 1: Capacitors with low capacitance values, dielectric with $\varepsilon_r < 100$, low dielectric losses, low temperature coefficient. Ceramics composed of $MgTiO_3$, Mg_2SiO_4, $BaTiO_3$ and various other materials are used for Class 1 capacitors, which are designated NP0, N220, N750, COG, etc.

Class 2: Capacitors of higher capacitance values, based on ceramics with ε_r up to about 15 000. The capacitance varies strongly as a function of temperature and voltage. Tan δ is higher than for Class 1, and the properties change in time. Dielectric designations are X7R, Z5U, etc.

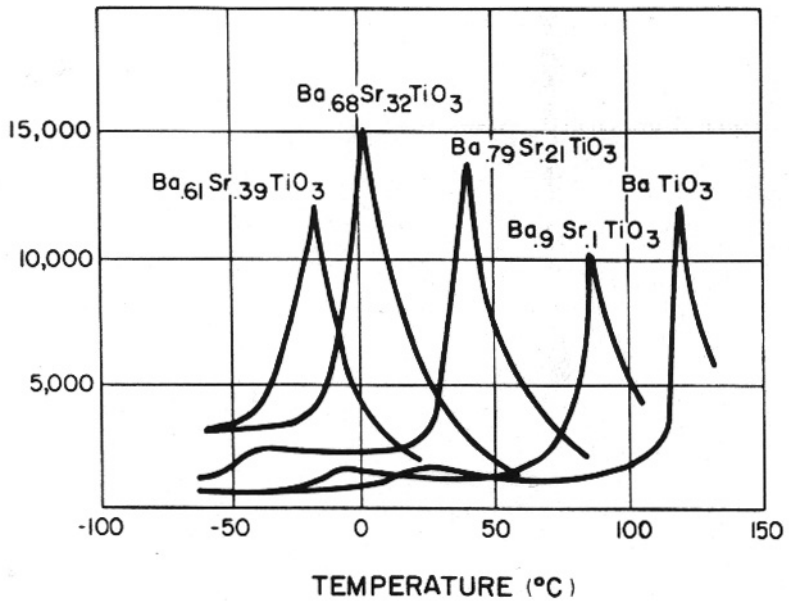


Fig. 4.8: Relative dielectric constant for ferroelectric ceramic compositions, as a function of temperature, near the Curie point [4.10].

Ceramic multilayer capacitors are available in the range between 1pF and several µF, maximum voltage 50 to over 500 V (power capacitors up to several kV), tolerance ±5 - 20 %. The sizes are standardised, the dominating ones being 0805

and 1206. 1210, 1808, 1812, 2220 are also common. The thickness of the chip varies depending on the number of layers, i.e. the capacitance value. The development moves toward smaller sizes; 0603 is in use and 0402 in development. They will require significant changes in mounting and soldering/gluing technology and equipment.

Some characteristic properties of capacitors of Classes 1 and 2 are shown in Figure 4.9. The voltage dependence as well as temperature coefficient and loss tangent are most favourable for NP0, least for Z5U. However, Z5U is a good choice for decoupling and other less critical applications that require high capacitance-to-volume ratio.

Ceramic capacitors - particularly Class 2 - have some inherent failure mechanisms that must be kept in mind: Low voltage failures, dielectric absorption [4.10], crack formation [4.11], and silver electromigration. The failures often occur gradually and may lead to high leakage current and change in capacitance value after some time.

Crack formation is the most troublesome failure type. It is caused by rapid temperature changes combined with thermal mismatch between the materials: The ceramic (thermal coefficient of expansion (TCE): α= 9.5 - 11.5 ppm/^{o}C for barium titanate), the terminal metals (15 ppm/^{o}C for nickel, 27 for solder), and the substrate (12 - 16 for fibre glass epoxy, and 5 - 7 for alumina ceramic). Figure 4.10 illustrates the most sensitive regions for crack formation. The cracks may start during the rapid temperature changes of the solder processes: The stress depends on the shape of the solder fillet and the capacitor, and the materials combination. The shape of the solder fillet again depends on the solder process, and the shape and location of the solder land. Thus, the reliability is determined by the design rules and technology choices made by the designer. It is characteristic for a ceramic that it can withstand more compression than tension. When the heating is uniform there is more tendency towards cracking when the substrate TCE is greater than that of the capacitor (e.g. organic substrates), than the opposite (e.g. alumina substrate). When self-heating of the capacitor is dominant the opposite is the case: The crack formation is more pronounced when the substrate TCE is smaller than that of the capacitor.

The crack formation is normally not visible or measurable at once. However, humidity and impurities will enter the crack and cause deterioration over time. The electrode materials will migrate into the crack, particularly when there is an electric field present. Furthermore, the component is mechanically weakened, and thermal cycling during the field life of the product will make the crack grow. Then tan δ and C will also change.

Class 2 capacitors change their capacitance over time by "ageing", according to a logarithmic time dependence.

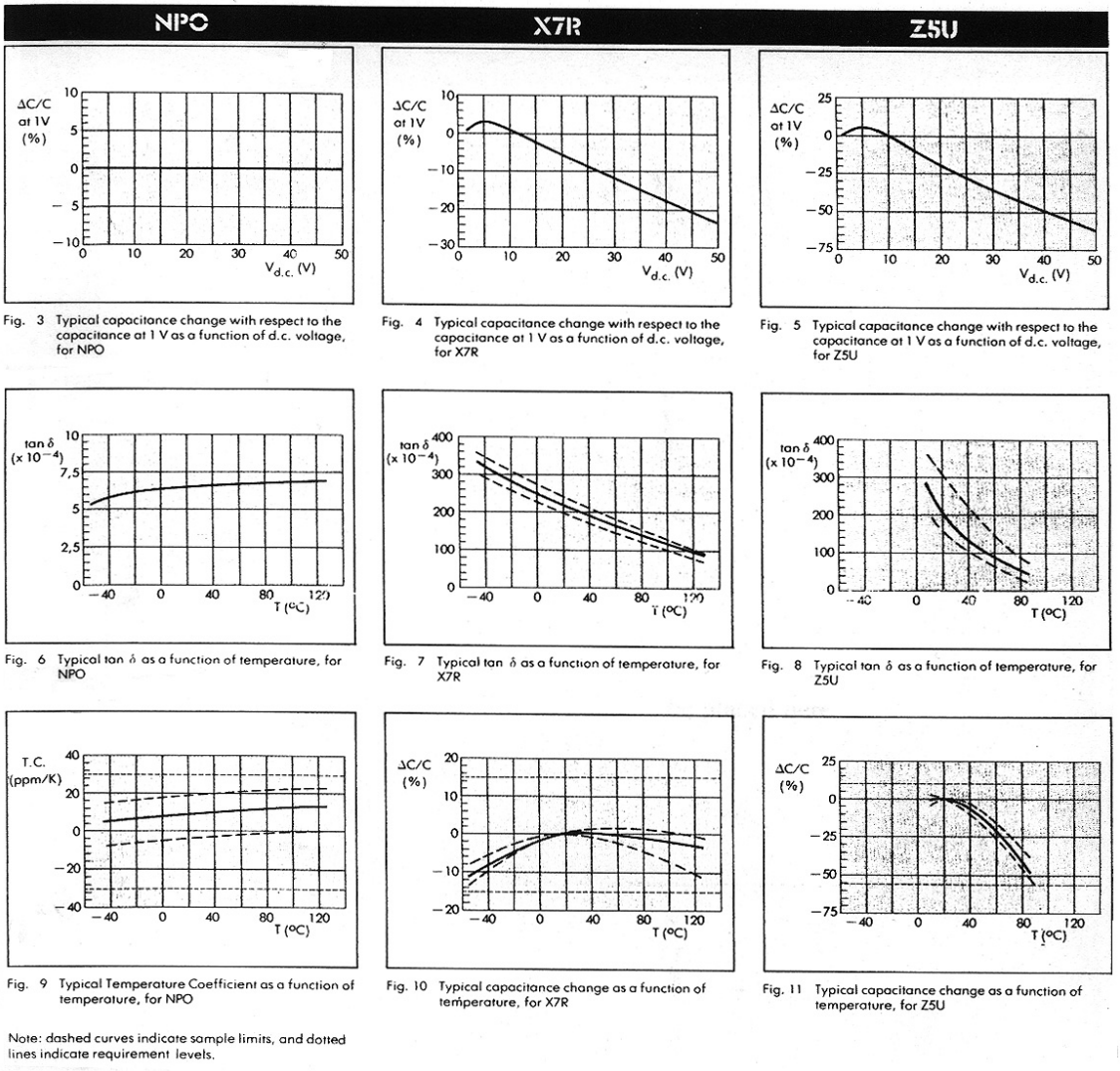


Fig. 3 Typical capacitance change with respect to the capacitance at 1 V as a function of d.c. voltage, for NPO

Fig. 4 Typical capacitance change with respect to the capacitance at 1 V as a function of d.c. voltage, for X7R

Fig. 5 Typical capacitance change with respect to the capacitance at 1 V as a function of d.c. voltage, for Z5U

Fig. 6 Typical tan δ as a function of temperature, for NPO

Fig. 7 Typical tan δ as a function of temperature, for X7R

Fig. 8 Typical tan δ as a function of temperature, for Z5U

Fig. 9 Typical Temperature Coefficient as a function of temperature, for NPO

Fig. 10 Typical capacitance change as a function of temperature, for X7R

Fig. 11 Typical capacitance change as a function of temperature, for Z5U

Note: dashed curves indicate sample limits, and dotted lines indicate requirement levels.

Fig. 4.9: Properties of dielectrics of the types NP0, X7R and Z5U in SMD ceramic multilayer capacitors. Top: The voltage dependence of capacitance; in the middle loss tangent as function of temperature; and at the bottom the temperature coefficient of the capacitance (Philips).

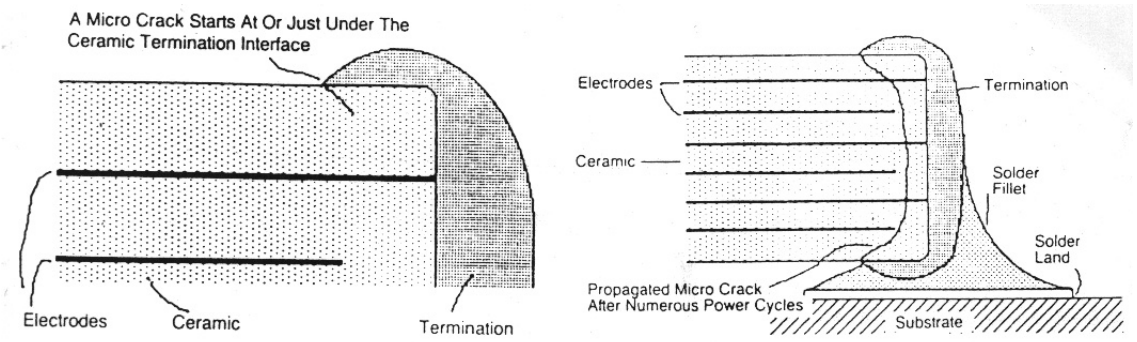


Fig. 4.10: Crack formation because of thermal stress in ceramic capacitors [4.11].

4.3.4 Electrolytic capacitors

Dry and wet electrolytic capacitors have a very high capacitance to volume ratio, due to a high effective area and a very thin dielectric. For this reason, they can withstand only low voltages. Due to their structure they can operate with voltages of only one polarity and are damaged by voltages of the other polarity, through destruction of the dielectric.

The most common dry type is the tantalum capacitor, Figure 4.11 a). It has tantalum as one electrode (anode), a thin layer of tantalum oxide as dielectric, and manganese dioxide as the other electrode (cathode). Its manufacturing process is described in [4.2, 4.6].

Tantalum electrolytic capacitors have good electrical properties, but so far, a high price and they lack standardisation between manufacturers. Available capacitance values are typically between 0.1 and 100 μF, maximum voltage 2 - 50 V, please refer to Fig. 4.11 b). A common fault is short circuit due to changes in the crystal structure of the dielectric for very high AC currents [4.14].

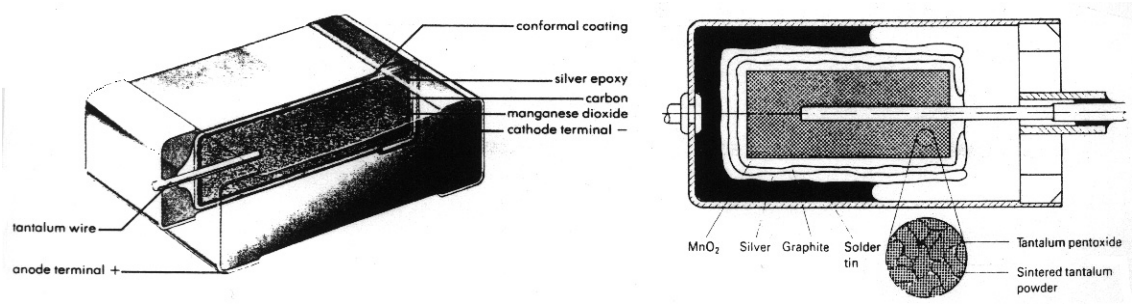


Fig. 4.11 a): Tantalum SMD electrolytic capacitor (Philips), hole mounted tantalum capacitors (Siemens [4.14]).

Dissipation factors vary with temperature: Maximum values which are not exceeded by any capacitor ar as follows.

Temperature	-55°C	25°C	85°C	125°C
Rated Voltage 4 to 10 V d.c.	10%	12%	12%	12%
Rated Voltage 15 to 50 V d.c.	8%	6%	6%	6%

The d.c. leakage current (at rated voltage) is within the limit set below

25°C <	0,01 µA/µFV	or	<	1 µA	whichever is greater
85°C <	0,10 µA/µFV	or	<	10 µA	whichever is greater
125°C <	0,125 µA/µFV	or	<	12,5 µA	whichever is greater

Fig. 4.11 b): Electrical properties of tantalum electrolytic capacitors (Philips).

Wet aluminium electrolytic capacitors are manufactured by anodic oxidation of Al [4.2]. The Al foil has been etched to give a rough surface with very high effective area. The wet electrolyte forms one electrode, the cathode, and Al the other electrode, the anode. Fig. 4.12 shows geometry and some electrical data. Wrong polarity of the voltage will ruin the dielectric and short-circuit the capacitor. Positive hydrogen ions will drift through the dielectric, become neutralised at the Al electrode and form hydrogen gas that breaks the dielectric and gives shortages.

When the temperature changes the wet electrolyte must "breathe", and the component cannot be sealed. This means that wet electrolytic capacitors cannot withstand long time in wave- or reflow solder processes. In these processes the component life will be reduced - in the worst case high pressure will build up in the electrolyte, which "boils" and may leak out, ruining the component.

Some aluminium electrolytic capacitors are made with a solid electrolyte, very often MnO_2 is used.

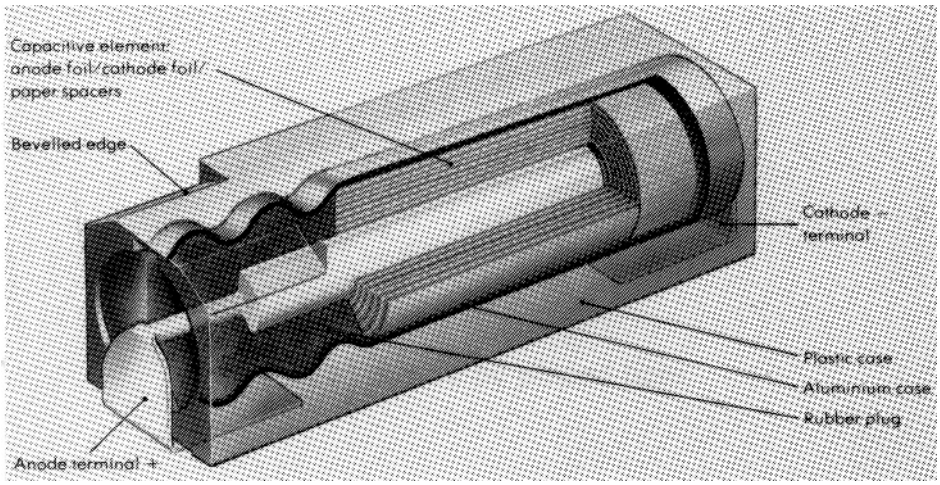


Fig. 4.12 a): Aluminium electrolytic capacitor for SMD mounting (Philips).

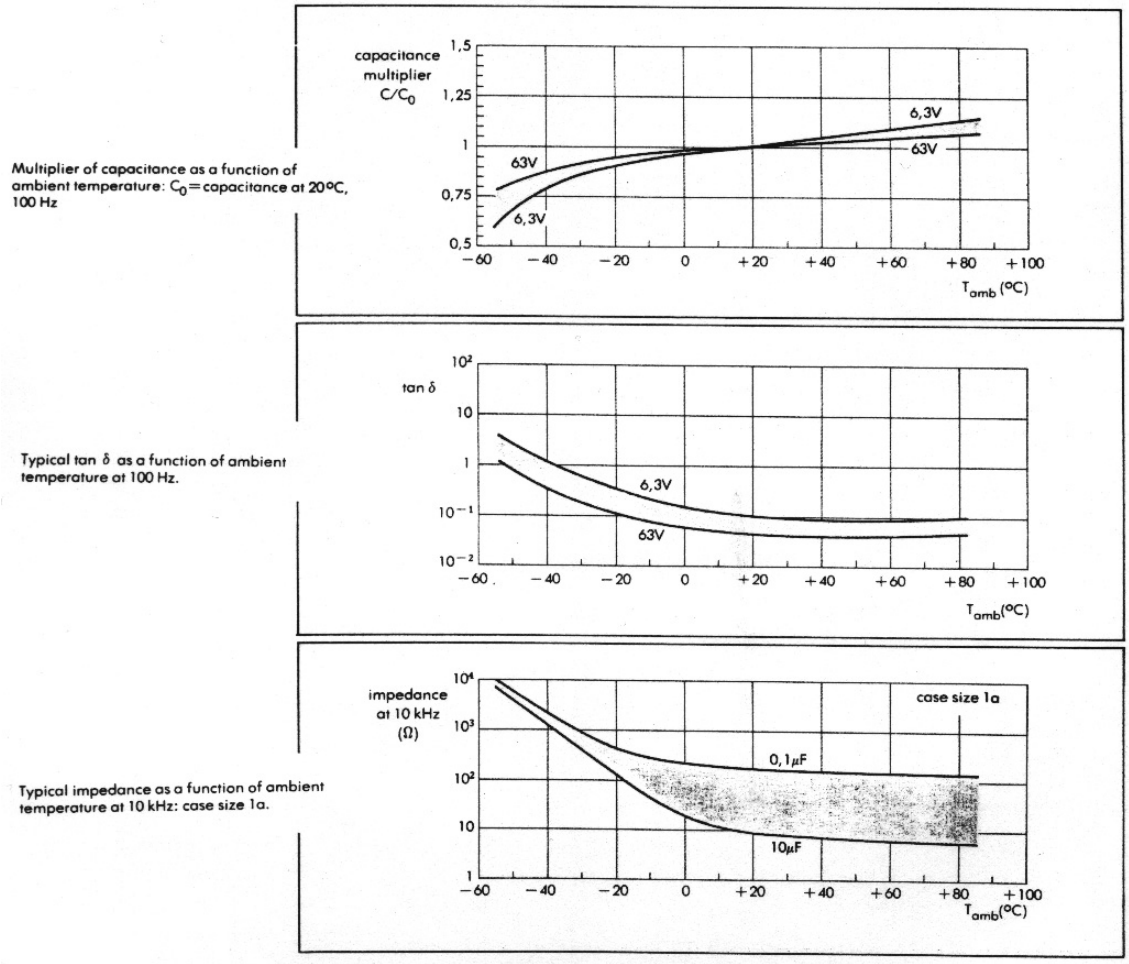


Fig. 4.12 b): Aluminium electrolytic capacitor properties (Philips). The top figure shows temperature dependence of the capacitance, relative to the value at 20 °C, the middle figure shows temperature dependence of tan δ, and the bottom figure shows temperature dependence of impedance at a frequency of 10 kHz.

4.4 DIODES AND TRANSISTORS

The packages for diodes and transistors depend on the component power, frequency of operation, reliability required, etc. For hole mounted diodes axial packages are most common, the semiconductor chip being mounted in a body of glass or ceramic, please refer to Figure 4.13. Power diodes have metal housing and screw mounting for better thermal coupling. The cathode of the diode is grounded to the can.

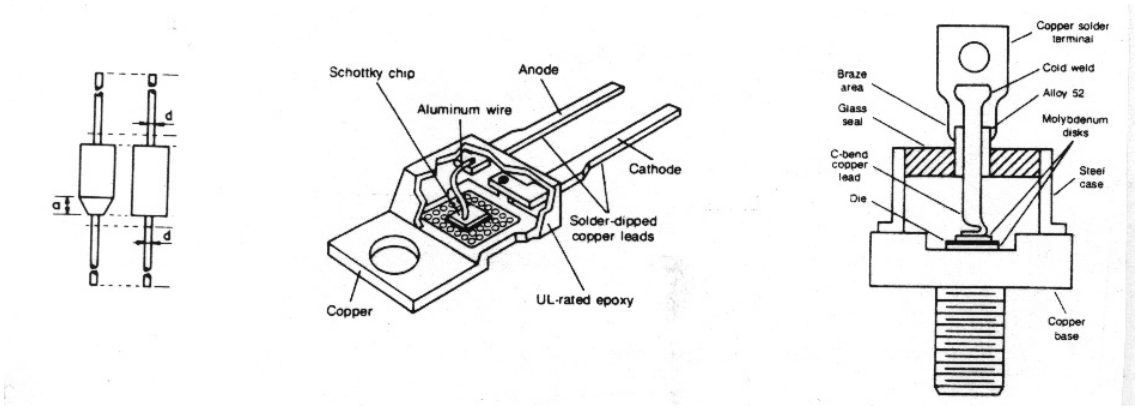


Fig. 4.13: Axial, plastic encapsulated, hole mounted diodes to the left. In the centre, a plastic can with metal base for power diodes. It can be hole mounted or surface mounted, depending on how the leads are bent. The base is screwed to the substrate. To the right, a higher power diode in a metal can, which is also screw mounted to the substrate for efficient thermal contact.

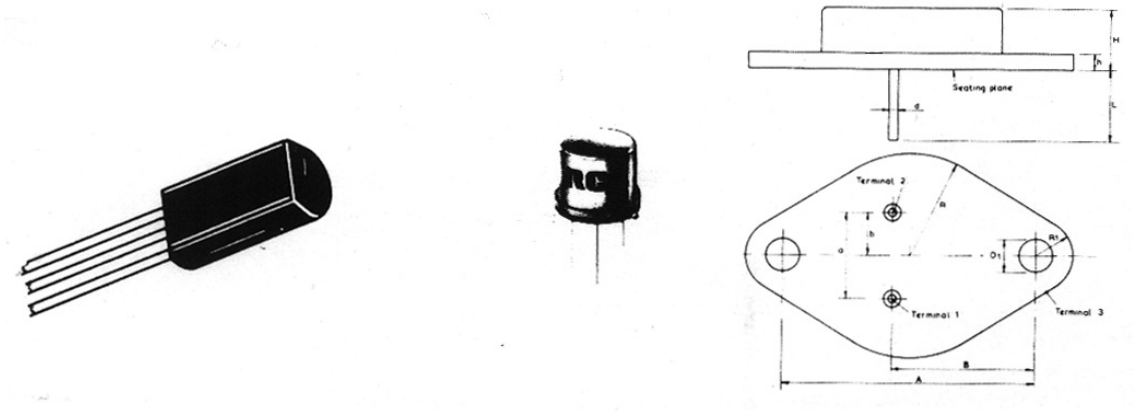


Fig. 4.14: Various types of hole mounted transistor packages: a) Plastic packages, b) Low power metal packages, c) Metal package for high power transistors. For the high power package, the collector is connected to the metal body.

Hole mounted transistors have a number of package forms, see Figure 4.14. Most are plastic. Metal housing is used to get hermeticity and the highest reliability. Power transistors have metal housings that are screw mounted on to the substrate for good thermal contact. The electrodes run through the metal base in a glass seal, with TCE matched to the metal.

For active SMD components, the semiconductor chip is normally the same as in the hole mounted equivalent, but the package is different. SMD diodes use two main package forms: MELF and SOT (Small Outline Transistor). For the MELF (Metal Electrode Face Bonding) version SOD-80 is the normal size, Figure 4.15. (SOD stands for Small Outline Diode.)

The more common type is SOT packages. They have rectangular plastic bodies and 3 or 4 leads, see Figure 4.16. In an SOT-23 package, there may be one diode with the third lead floating, or two diodes with one common terminal. The SOT-143 will contain two independent diodes. These packages have a maximum power rating of 0.1 - 0.3 W. SOT-89 has very good thermal contact to the substrate and can dissipate up to 1 W.

Hermetic SMD transistor packages made of ceramic exist, see Figure 4.16, but are not much used.

A transistor package with dimensions even smaller than those of the SOT-23, the SOT-323 has also been introduced: "Mini SOT" or SOT-323, with over-all dimensions 2.0 x 1.25 x 0.9 mm.

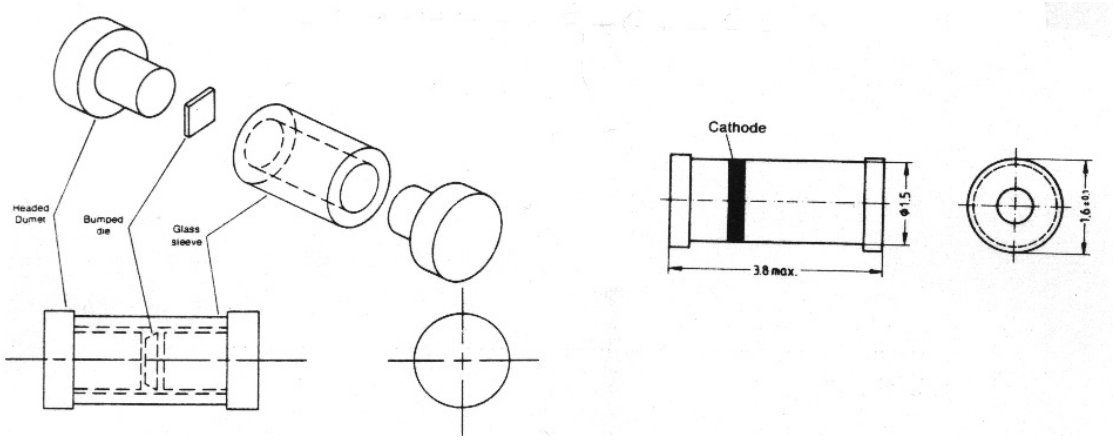


Fig. 4.15: MELF-package for SMD diodes. The standard size is designated SOD-80, with dimensions shown to the right.

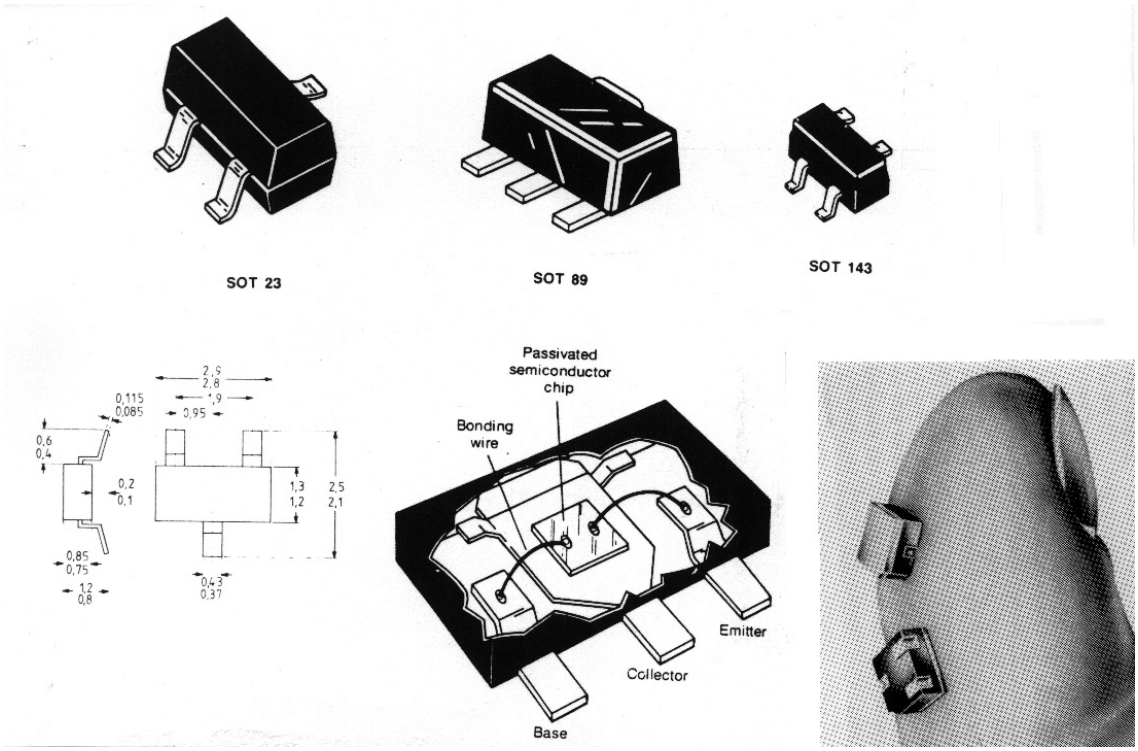


Fig. 4.16: SOT-packages for SMD diodes and transistors: The most common, SOT-23 top left, SOT-89 for power transistors in the middle, and SOT-143 with four terminals to the right. The dimensions for SOT-23 are shown bottom left, and a cut-through SOT-89 in the middle. Ceramic SMD transistor packages with terminal placement like for SOT-23 are shown bottom right.

4.5 MONOLITHIC INTEGRATED CIRCUITS

4.5.1 Plastic or ceramic packages: Advantages and disadvantages

Plastic and ceramic IC packages are both used. Each type has advantages and disadvantages, and the application determines the choice. We list some characteristics of both types.

Plastic:

- Not hermetic.
- Low price in large component quantities.
- High initial cost for tooling etc., not suitable for prototypes of custom circuits.

- Poor thermal conductivity of the plastic (0.2 W/°C·m, somewhat higher with special additives).
- Tolerate only limited time at high temperature (SMD soldering processes).
- High thermal expansion coefficient (25 - 50 ppm/°C) and thermal mismatch to Si chip and to metals. This is important for large Si chips and large packages.
- High demands on plastic quality and moulding process. If not satisfied, the long-term reliability will suffer.
- Not suitable for high frequency circuits which require controlled characteristic impedance.
- Special failure mechanisms (please refer to Section 3.3 and Chapter 9).

Ceramic:

- Hermetic, give good reliability.
- Costly, even in large volume, but Si chips can easily be mounted into pre-made packages, important for prototyping.
- Good thermal conductivity (15 - 30 W/°C·m for alumina).
- Low thermal coefficient of expansion (5 - 7 ppm/°C for alumina), gives thermal mismatch to organic substrates. This can be serious for leadless packages.
- Leadless packages have gold metallisation, which must be removed before soldering (see Section 4.7).
- Can be manufactured with well-defined high frequency properties.

Plastic packages dominate for ordinary uses. Ceramic is used for critical military and telecommunication systems, where hermeticity is required to get supreme long term reliability. They are also used for electrically and thermally demanding systems, see later (and in Chapter 6).

During the last years the reliability of good plastic packaging has improved much and is used increasingly even in the most demanding telecom- and military equipment.

4.5.2 Standard packages for hole mounted ICs

The DIP package

"Dual-in-line" packages (DIP), as seen in Figure 4.17, dominate for hole mounted ICs. For plastic DIPs the silicon chip is alloyed, soldered or glued to a metal plate, the leadframe, which is often an alloy of Fe/Ni 42/58 ("alloy 42") with low TCE to reduce the mismatch to Si. Components with high heat dissipation have Cu leadframe. Thin gold or aluminium bonding wires provide electric contact between chip and leads.

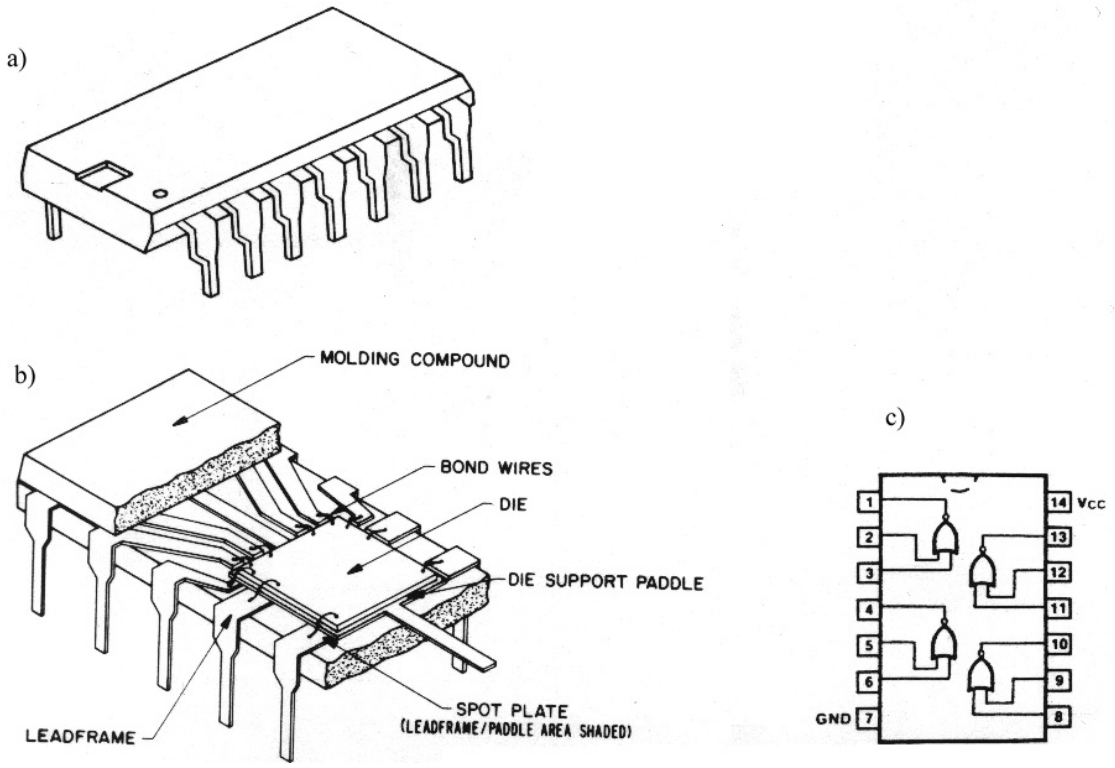


Fig. 4.17: a) DIP IC package. b) Partly cross-sectioned DIP package which shows the silicon chip, bonding wires, lead frame and plastic body. c) The terminal organisation for 4 two-input NOR gates in a 14 pins package.

The leads are in two rows. The dimensions are standardised on a grid of 0.1 " (100 mils) distances. The lead separation is 100 mils and the distance between the lead rows is 300 - 600 mils.

DIP packages are made with 8 - 64 leads. For small circuits with few I/Os several circuits are often made on the same piece of silicon and packaged in the same package, see Figure 4.17 c).

Ceramic DIP packages with a cavity for the chip are also common. The simplest is called CERDIP, and has two ceramic parts with glass sealing between them. The more advanced 3-layer ceramic package is made by multilayer ceramic technology, with metallisation between the layers (see Chapters 3 and 8). It normally has a metal lid that is soldered on after the component has been evacuated and filled with inert gas.

DIP packages can be surface mounted if necessary, by butt soldering the leads, or by bending them out in "gull wing" shape like for the SO package (see below).

Cylindrical metal cans with axial lead terminals are still used for some hole mounted ICs. They are not suitable for automatic mounting and high volumes.

The Pin Grid Package

Large VLSI circuits often have more than the maximum 64 I/Os available as a DIP. The largest hole mounted IC package is the pin grid, with leads on a grid of 100 mils lead separation, please refer to Figure 4.18. The pin grid is most frequently made of alumina ceramic, with up to 400 - 500 leads. There may be up to 6 - 10 layers of ceramic. Pin grid packages are made "cavity down" or "cavity up", depending on whether the heat should be removed down into the substrate or up, into a cooling fin (see Chapter 6). They use the board area better than the DIP and have very good thermal performance, but they are expensive. Once they are soldered onto the board, it is difficult to de-solder and remove them (repair). Therefore, they are often mounted in a socket. Routing the wiring to a pin grid package normally requires more than two layer boards.

Some standard products are supplied in plastic pin grid packages.

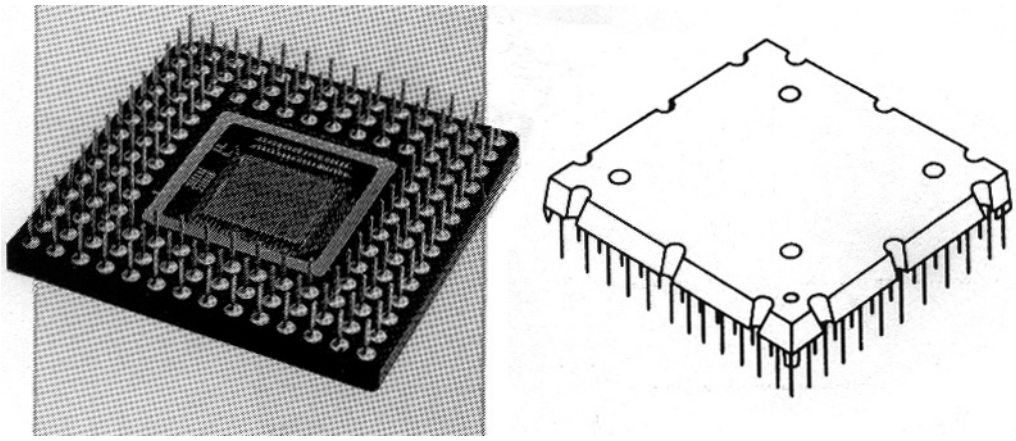


Fig. 4.18: Pin grid packages: To the left a cavity up ceramic package, and to the right a plastic moulded package.

4.5.3 Standard packages for SMD

SO and VSO

Between 8 and 28 terminals the Small Outline (SO) package, please refer to Figure 4.19, is the most common SMD package for ICs. They are similar to a small version of the DIP, thus the name. The lead separation is 50 mils, and the leads are bent out in "gull wing" form. Philips introduced the SO package, as well as the "Very Small Outline" (VSO) package with 40 and 56 leads, with separation 30 mils and 0.75 mm respectively. The VSO has not become widely used.

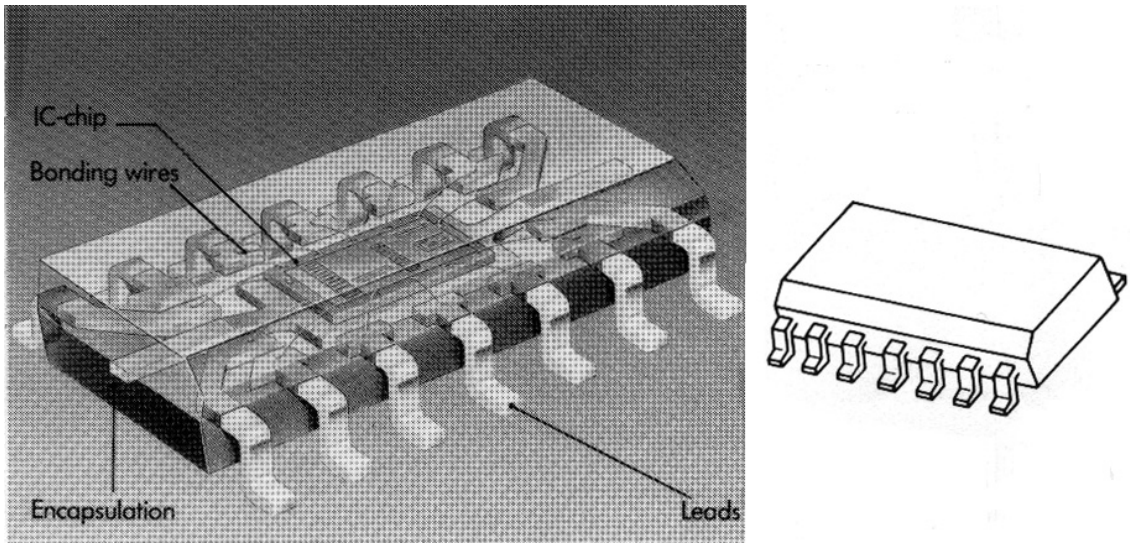


Fig. 4.19: Surface mounted SO (Small Outline) IC package (Philips).

Table 4.3: Dimensions for SO- and VSO packages. Centre-to-centre lead distance is normally 50 mils, except for VSO-40 with 30 mils and VSO-56 with 0.75 mm.

Outline	Encapsulation		Maximum width
SO	Maximum width	Maximum length	Lead end to lead end
	[mm]	[mm]	[mm]
SO-8	4,0	5,00	6,2
SO-8	7,6	7,6	12,4
SO-14	4,0	8,75	6,2
SO-16	4,0	10,00	6,2
SO-16L	7,6	10,5	10,65
SO-20	7,6	13,0	10,65
SO-24	7,6	15,6	10,65
SO-28	7,6	18,1	10,65
VLO-40	7,6	15,5	12,8
VSO-56	11,1	21,6	15,8

Normally the SO packages are plastic, but ceramic versions exist.

A similar package, much used for memory circuits, is the "SOJ", which has its leads bent underneath the body, similarly to the PLCC, see below and Figure 4.20a).

PLCC and LLCC

Two dissimilar packages are called "chip carriers". One of them is the Plastic Leaded Chip Carrier, (PLCC), Figure 4.20 a), with leads on all four sides. The leads are folded under the body in J-shape to conserve board area. They have 50 mils pitch and are used for 18 - 84 terminals. The largest type is less used, because of reduced reliability due to thermal mismatch problems. The PLCC was introduced by Texas Instruments and is the most common SMD package for 28 - 68 terminals.

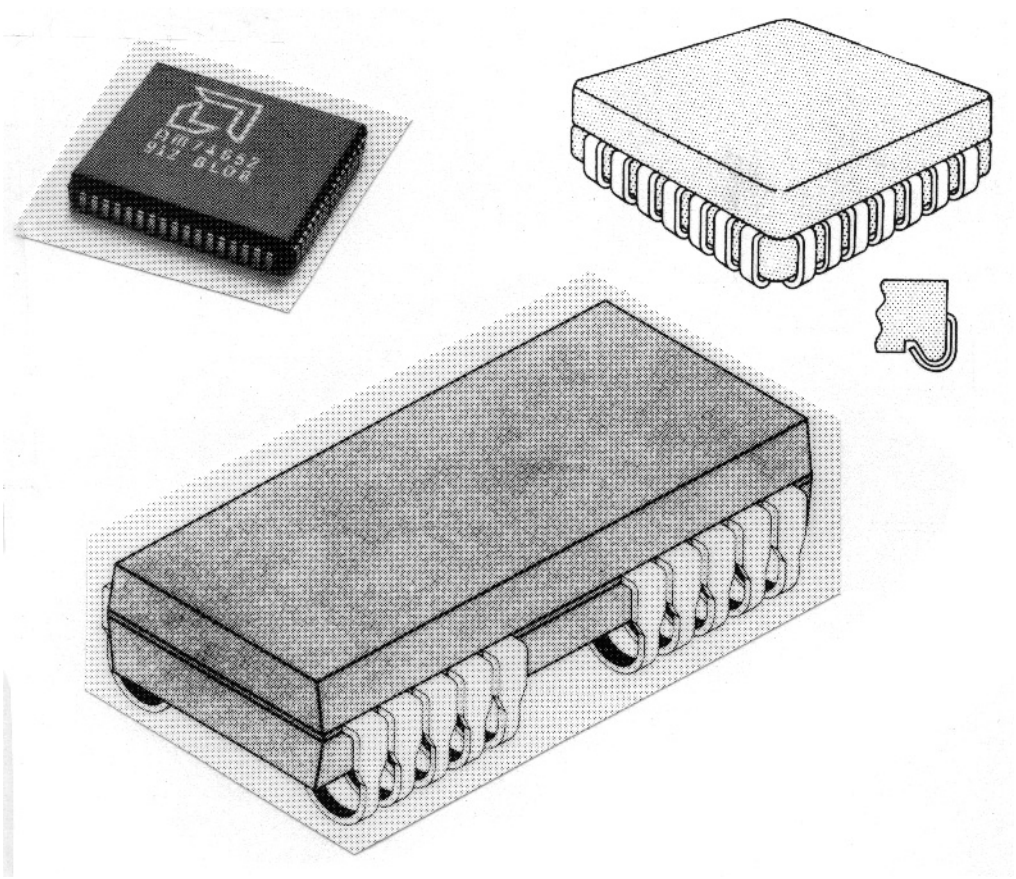


Fig. 4.20: Plastic chip carrier with leads (PLCC). They are normally square with an equal number of terminals on all four sides (top). For large DRAMs, the package has terminals on only two sides, also being called SOJ. The bottom figure shows a 1 or 4 Mbit DRAM package.

Table 4.4 Dimensions for PLCC packages. Format means the number of terminals on two neighbouring sides.

Leads	Format	Lead pitch [mm]	Maximum body dimensions [AxB] [mm]	Maximum Device Dimensions (LxW) [mm]	Typical Height (C) [mm]
20	5x5	1,27	9,1x9,1	10,1x10,1	3,5-4,7
28	7x7	1,27	11,6x11,6	12,6x12,6	3,5-4,7
44	11x11	1,27	16,8x16,8	17,8x17,8	3,5-4,7
52	13x13	1,27	19,3x19,3	20,3x20,3	3,5-4,7
68	17x17	1,27	24,4x24,4	25,4x25,4	3,5-4,7
18	5x4	1,27	10,9x7,5	11,9x8,5	3,5-4,7
28	9x5	1,27	14,1x9,0	15,1x10,0	3,5-4,7
32	9x7	1,27	14,1x11,6	15,1x12,6	3,5-4,7

The other type of chip carrier is ceramic and has no leads, thus the name Leadless Chip Carrier (LLCC), Figure 4.21 and Table 4.5. The terminals are metallised areas on the ceramic body. The ceramic makes the package hermetic, and it has thermal properties much superior to the plastic IC packages (Chapter 6) when they are soldered to the substrate.

However, the missing flexible leads give a disadvantage: Thermal mismatch to organic PCBs. The TCE for glass epoxy laminates is 12 - 16 ppm/°C, whereas the alumina ceramic has 6 ppm/°C. When the temperature changes during soldering processes and operation, this mismatch will give mechanical stress and in time possibly broken solder fillets. This is particularly a problem for the larger LLCCs and has reduced the usage of LLCC. Some types are made for socket mounting, or a set of leads can be soldered onto the LLCC. For leaded packages, stress due to the thermal mismatch normally is negligible.

Fig. 4.21 shows all the standard forms of chip carriers. A - D are LLCCs, type C is the most common for direct soldering on a substrate. It is made with three layers of ceramic. The other types are primarily for socket mounting or soldered-on leads. The components normally have metal lids that are soldered on with a solder alloy of high melting temperature, so it does not fall off during the component soldering. Alternatively, the lid may be ceramic too.

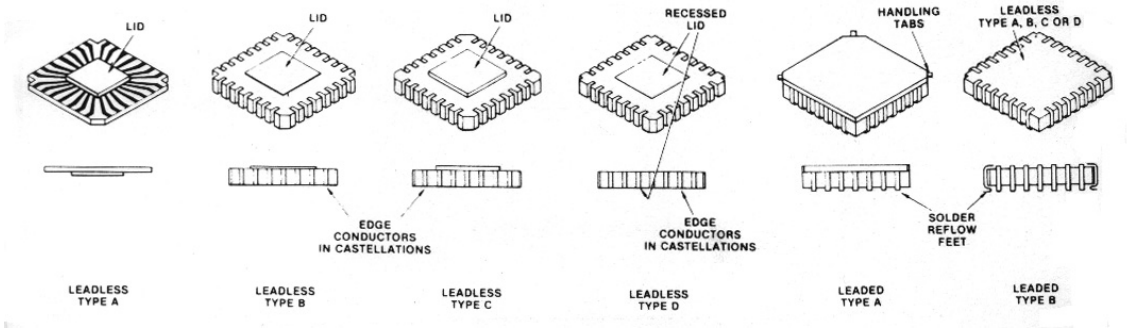


Fig. 4.21 a): The various types of ceramic chip carriers [4.15]. Types A -D to the left are leadless (LLCC), whereas types A and B to the right are meant for mounting leads (LDCC).

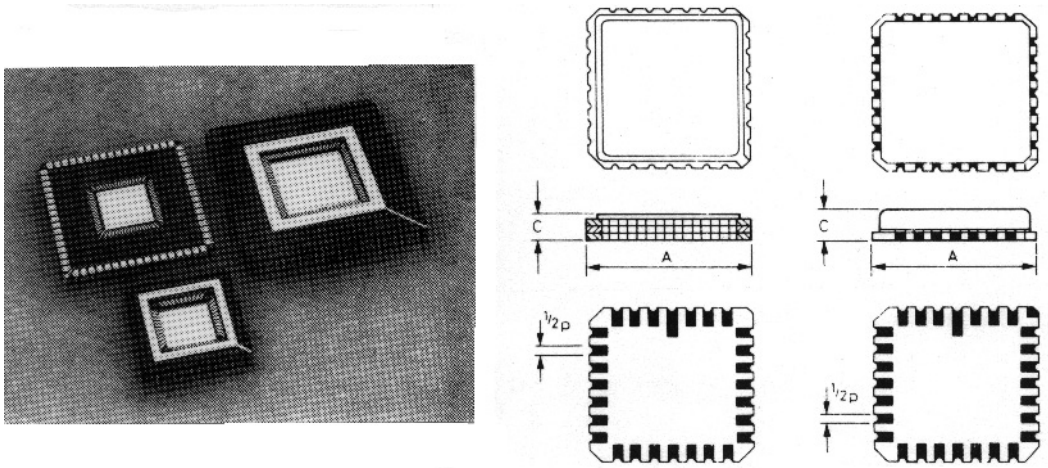


Fig. 4.21 b): LLCC packages, additional details. The longest terminal is to designate electrical terminal number 1 in the circuit.

Table 4.5. LLCCs, dimensions.

Leads	Format	Pad Pitch (p) [mm]	Maximum Dimension (AxB) [mm]
20	5x5	1,27	9,1x9,1
28	7x7	1,27	11,6x11,6
44	11x11	1,27	16,8x16,8
52	13x13	1,27	19,3x19,3
68	17x17	1,27	24,4x24,4
84	21x21	1,27	29,6x29,6
18	5x4	1,27	10,9x7,5
28	9x5	1,27	14,1x9,0
32	9x7	1,27	14,1x11,6

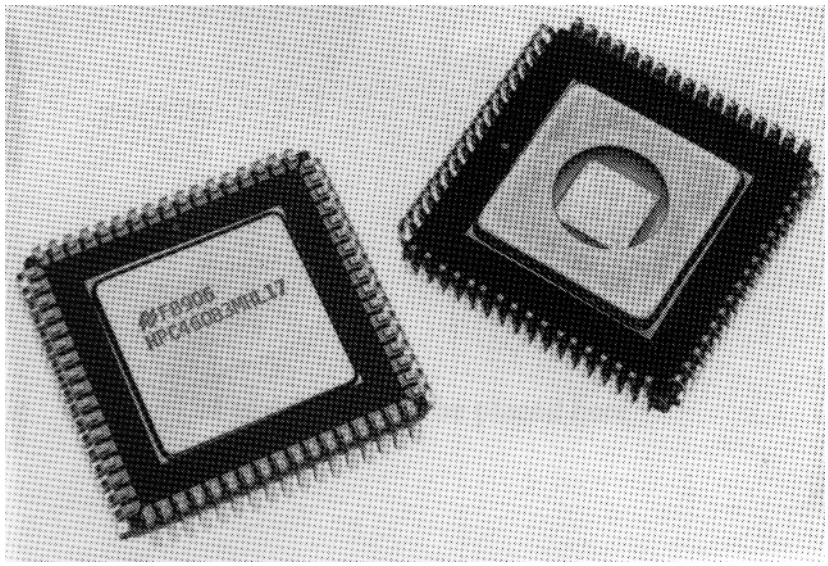


Fig. 4.22: Leaded ceramic chip carriers.

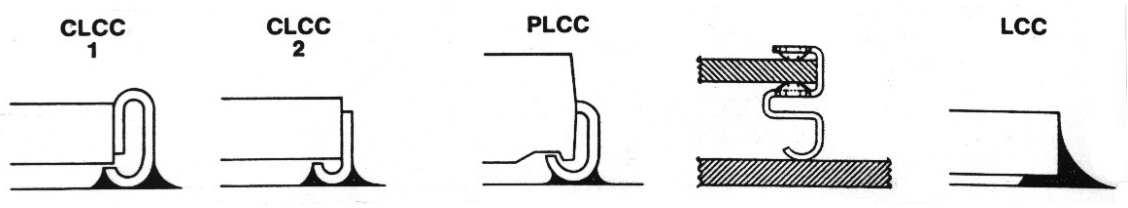


Fig. 4.23: Various shapes of the leads, and leadless termination for comparison.

Leaded ceramic chip carriers (LDCC), see Figure 4.22, with gull wing or J-shape leads are in limited use. The leads have various shapes, giving high or low flexibility, see Figure 4.23.

A plastic type of leadless chip carrier has been developed in the United Kingdom under the name EPIC [4.16]. The body is machined from glass/epoxy, giving perfect thermal match to glass/epoxy PCBs. The idea seems good, but the package is not much in use.

Flatpacks and mini-flatpacks

Flatpacks have been used in hybrid technology for many years, also for packages for a complete hybrid circuit (See Chapter 8). They are made out of plastic or ceramic (and metal for hybrid circuit packages). Some have leads on two sides and some on four (Quad flatpacks), see Figure 4.24. Often the leads come out from the central plane of the body, and end in a shorting frame or ring that protects the leads from being bent, as well as protecting the IC (see Section 4.8). When they are mounted the ring must be cut off, and the leads bent to a gull wing shape if the component is mounted on a flat surface.

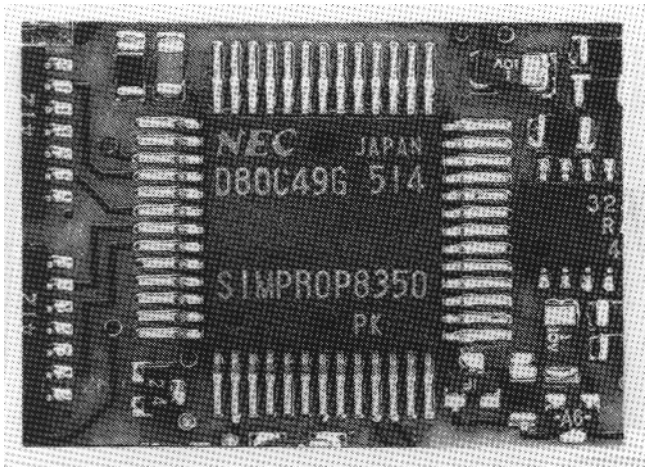


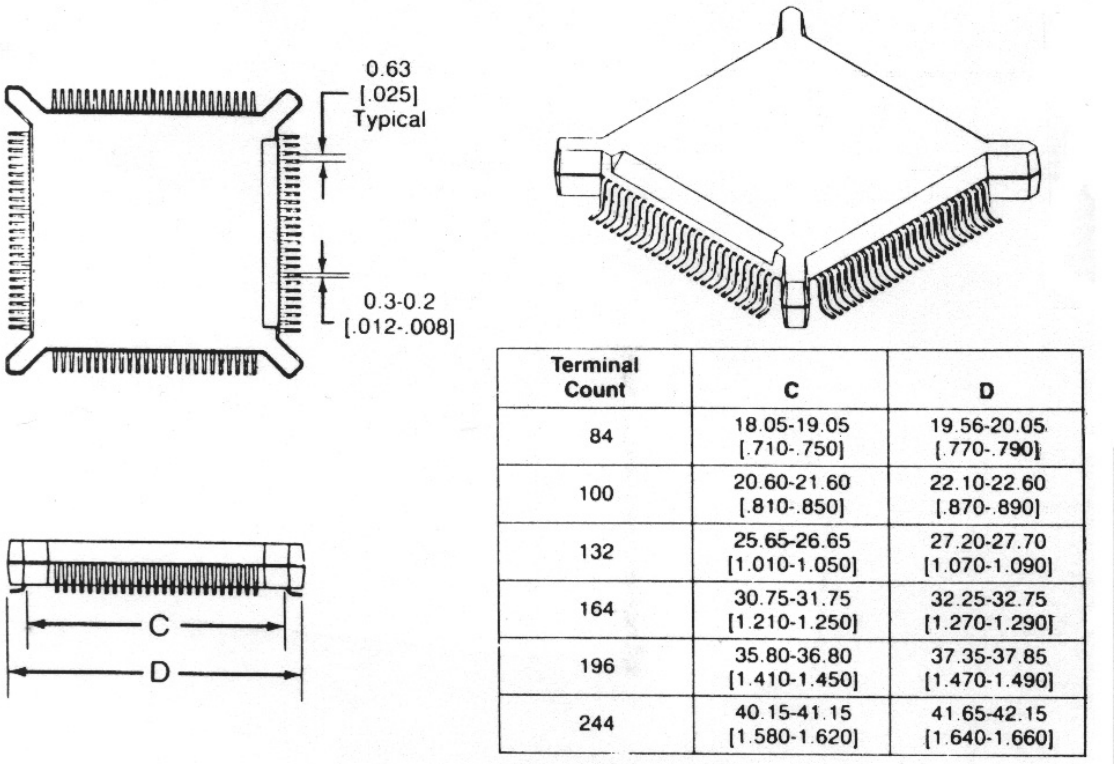
Fig. 4.24: Quad flatpack with leads on all four sides.

Many sizes and lead pitches are used for flatpacks. In the USA 50 mils, 25 and 20 mils dominate, in Japan 1.25, 1.0, 0.8, 0.65 mm. Up to 300 terminals are available for plastic or ceramic flatpacks.

One type of plastic package is called Fine Pitch Quad Flatpack or Mini-flatpack.This package has been accepted by JEDEC as a new industry standard for 84 - 244 terminals and a pitch of 25 mils, see Figure 4.25. It has a gull wing lead shape. Because they are thin, the leads are very vulnerable to deformation during transport and handling. As protection, the package has a characteristic protuberance at each corner. The transport tube is formed such that the protuberances touch the walls, but not the leads.

4.5.4 TapePak and moulded carrier ring packages

National Semiconductor has developed a compact and elegant plastic package "TapePak", that is on its way to become another industry standard for demanding applications [4.17]. The IC is moulded into the central plastic body, see Figure 4.26. The connections to the chip are made by Tape Automated Bonding (TAB) using one-layer tape (Chapter 3), that serves as leadframe. The TAB leads stick out of the central body, at a pitch of 20 mils or less. Further out there is a plastic ring for protection, and the leads go through it too, ending in test points for component testing. The test points have a pitch of 50 mils, making it possible to have a simple and rugged test fixture. During mounting, the leads are cut inside the outer ring in an excising operation, and they are bent to gull wing form, in a combined cut-and-form tool. Then the mounting is done, all in the same automatic machine.



Terminal Count	C	D
84	18.05-19.05 [.710-.750]	19.56-20.05 [.770-.790]
100	20.60-21.60 [.810-.850]	22.10-22.60 [.870-.890]
132	25.65-26.65 [1.010-1.050]	27.20-27.70 [1.070-1.090]
164	30.75-31.75 [1.210-1.250]	32.25-32.75 [1.270-1.290]
196	35.80-36.80 [1.410-1.450]	37.35-37.85 [1.470-1.490]
244	40.15-41.15 [1.580-1.620]	41.65-42.15 [1.640-1.660]

Fig. 4.25: Mini flatpack.

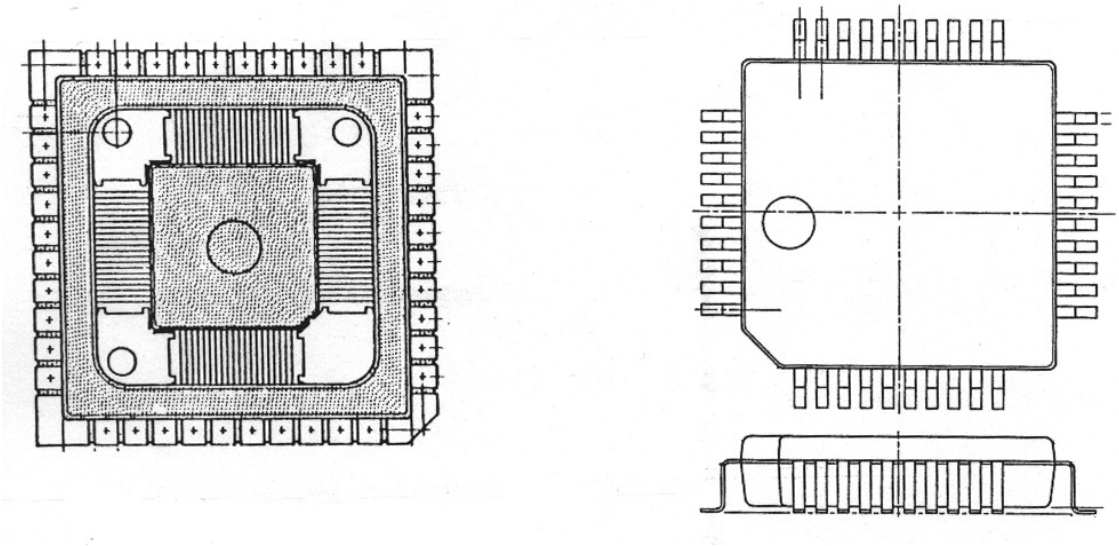


Fig. 4.26: National Semiconductor´s TapePak component packages are specified with terminal numbers between 40 and close to 600. To the left we see a 40 leads TapePak in the form it is received by the user with a protective ring around it, and test points outside the ring. To the right is TapePak 40 after excising and lead bending, seen from above and from the side.

TapePak has standardised dimensions for components with between 40 and about 600 leads. Pitch for the smaller packages is 20 and 15 mils. For the larger packages it is metric, down to 0.25 mm.

The concept has many advantages for compact packaging of complex circuits: They take up very little board space (similar to TAB circuits), They are rugged during transport and testing, and the testing is easy. Finally, TapePak has the possibility of a larger number of I/Os than any other standard package.

A major problem is that expensive equipment is needed for the mounting, including the cut-and-form tool that is specific for each size. Mounting and soldering are challenges requiring refined processes. The mounting equipment needs electronic vision to achieve the necessary accuracy.

Around one dozen companies use TapePak today, for special high volume circuits. Some component manufacturers make a modified version of TapePak, called "Moulded carrier ring". It looks similar to TapePak but uses a regular leadframe and wire bonding for electrical contacts to the chip.

4.5.5 High performance packages

The most demanding electronic systems have components that operate at clock frequencies 100 MHz – 1 GHz, (higher in the future) dissipating a power of 2 - 10 Watts and more, some have several hundred in- and outputs. Standard component packages cannot satisfy such demands.

To improve the ability to remove the heat, one can mount cooling towers on both plastic and ceramic packages and cool with fans (please refer to also Chapter 6, thermal design). Some plastic and ceramic packages are made with a metal plate or metallised via holes underneath the semiconductor chip, through the bottom, and the package can be soldered to the component substrate at these points, to use the good thermal conduction of the metals. This is designated "thermal vias", see Figure 4.27.

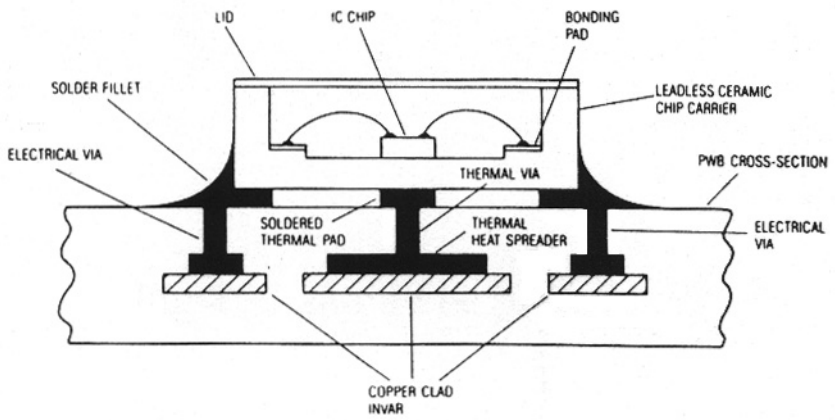


Fig. 4.27: Thermal via-holes in the printed circuit board, for better heat conduction.

Packages for power electronics, demanding computer circuits, etc., are in some cases made with AlN ceramic, which has thermal conductivity one order of magnitude better than Al_2O_3. Another advantage with AlN is low thermal coefficient of expansion. However, until now the material has been very costly, and special processing is required to get the conductor materials to give good adhesion, please refer to Section 8.6.

Special high frequency packages must have a controlled characteristic impedance for all critical signal paths, and it is important to have decoupling capacitors close to the power terminal for the Si- or GaAs chip (please refer to Chapter 6). Such packages are often designed especially for the circuit. They are built from many layers of ceramic, with separate metal layers for ground and power plane, and signal layers between, with transmission line geometry (Chapter 6). Figure 4.28 shows such a component, made by Triquint Semiconductor. On top of the package there are soldering terminals for mounting of decoupling capacitors/termination resistors.

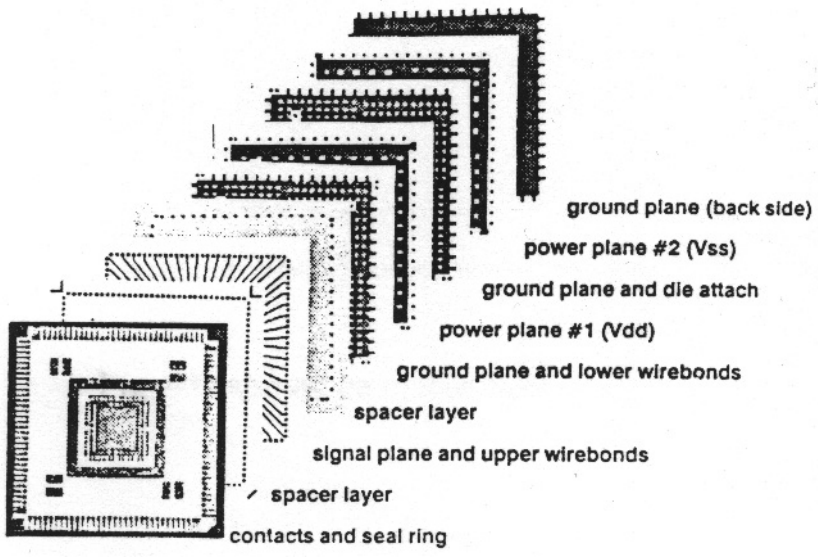


Fig. 4.28: Multilayer package for high frequency GaAs circuits with 3 ground planes, 2 voltage planes, 1 signal layer and a top conductor layer for contacts and sealing (Triquint).

The company Gigabit Logic has chosen a different solution for their GaAs circuits. Here the chip is mounted on a Si substrate, where the decoupling capacitors and termination resistors are made by monolithic technology in the substrate.

Figure 4.29 shows a module with several ECL chips for Hitachi computers. Here the Si chips are mounted with flip chip on Si substrate. The package has a bottom of SiC for good heat conduction to a cooling fin.

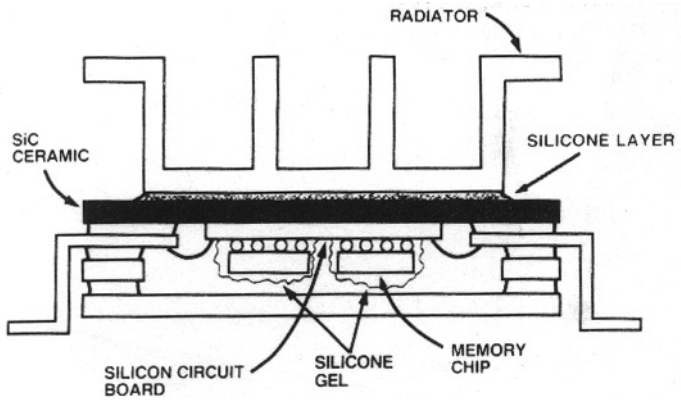


Fig. 4.29: Multichip package for memory module in a Hitachi high-performance computer [4.18]. The module contains 6 ECL chips, mounted by flip chip.

The last examples show packaging of several chips in the same package, and use of Si as substrate for IC circuits. Such multichip modules will be discussed in more detail in Chapter 8.

4.5.6 Future trends

The development of electronic systems tends toward denser packaging, higher working frequency, and higher power generated per unit volume, as mentioned earlier (Chapter 2). This gives constantly increasing demands on the component technology and packaging. The use of compact forms of packages is increasing. Figure 4.30 shows the area required for an IC with approximately 64 terminals, in different forms of encapsulation.

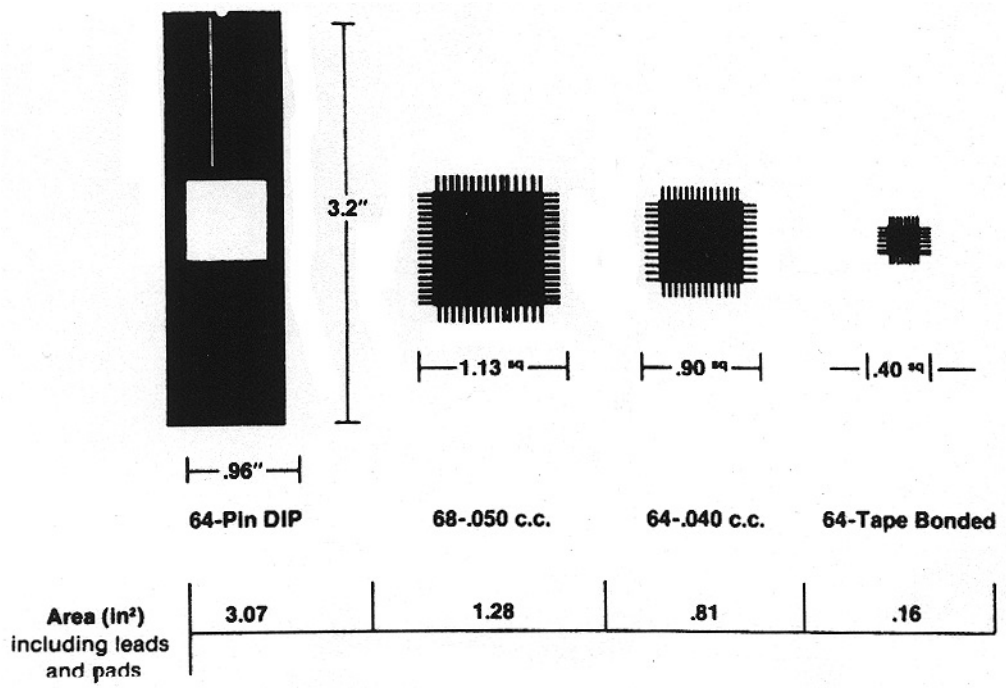


Fig. 4.30: Comparison between the size of various package forms for an integrated circuit with approximately 64 terminals.

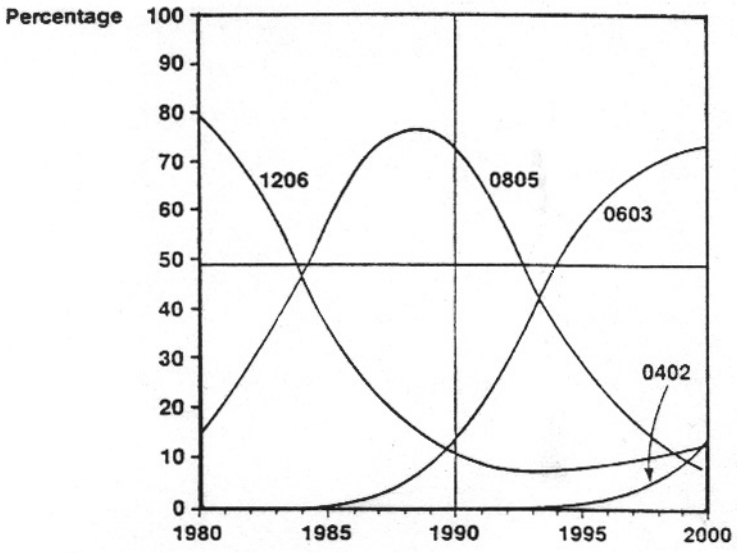


Fig. 4.31: History and prognosis for the use of various sizes of passive SMD components, in percentage of the total number (K. Wassink, ISHM Nordic).

A prognosis for the use of DIP, SMD and TAB packaging was shown in Figure 2.3, indicating an increasing use of more compact packages or chip on board. Fig. 4.31 shows a prognosis for the use of passive components in different sizes, also demonstrating a trend toward more miniaturisation. The development toward smaller packages will give major challenges to the component producers and to the electronic systems producers.

4.6 VARIOUS COMPONENTS

The components discussed until now are the most common categories, both for digital and analogue circuits. However, for the complete system special components are often required, such as:

- Connectors
- Potentiometers
- Inductors
- Transformers
- Crystals
- Switches
- Sockets
- Displays, etc.

They are often termed "odd" components. There are so many types of them and there is so little standardisation, that it is outside the scope of this course to treat them all. They often complicate the mounting and soldering processes. They may give high cost, because they must be mounted and soldered manually in many cases. They require special consideration in the development and design phase of the electronic product.

Mechanical components that provide the mechanical support of the electronics are also important, and they also require special consideration in the design phase. These components are made of metal, plastic and other materials. They may represent a major part of the system cost.

4.7 TERMINAL METALLISATION, SOLDERABILITY AND RELIABILITY

The metal layer on the leads/terminals areas where the components need to be soldered or glued is important for the solderability and for long term reliability of the soldering.

The components may be stored several months. Spare parts are often stored many years before they are mounted and soldered into the system. Also then, the solderability must be good. The metallurgy is particularly important for SMD components because the solder joints serve as electrical connections as well as mechanical support to the component. In addition, the dimensions of the solder joints are small. The components experience great thermal stress during the solder processes, when the whole component gets a thermal shock.

4.7.1 Passive components

For SMD resistors and multilayer ceramic capacitors, silver or a silver alloy is used closest to the ceramic, because it gives good adhesion. However, silver has very high solubility and high speed of solution in solder metal, as pointed out in

Section 3.10. Thus, we risk that the silver is dissolved during the solder process ("leaching") or diffuses in the solid phase during the normal operation of the equipment. This may give electrical discontinuity, or the component may even fall off. Several alternatives are used to avoid this [4.3, 4.4, 4.7]. One alternative is to alloy the silver with up to 20 - 35 % palladium or possibly platinum, that reduces the solubility. By using a small percentage of silver in the solder metal, the solubility is further reduced, see Figure 3.17.

Alternatively, a layer of nickel is deposited outside the silver (the silver alloy), as a diffusion barrier.In addition, it is common to use tin or a eutectic mixture of tin/lead, to avoid oxidation of the nickel during soldering. This is done to ensure a good solderability.

If the components are to be glued (e.g. in thin film hybrid circuits), there must be no Sn/Pb in the outer layer. The electrically conductive adhesives contain silver, which will in that case be dissolved.

Nickel is harder than the other metals, and it gives mechanical stress during quick changes of temperature because of this. The noble metals used on the terminations are quite costly. What type of termination is most suitable depends on environmental requirements, area of application and the sensitivity to price for the components and for the system.

4.7.2 Integrated circuits

During their processing ceramic DIP packages or LLCC packages get a thin layer of high purity, soft gold on the metallised areas, both inside, where the bonding wires from the silicon chip are connected, and outside, where the package is to be soldered to the substrate. The gold is good for bonding and also has the advantage that it does not corrode during long time storage. However, gold in mixture with solder metal gives poor strength in the solder fillet, and it gets brittle, see Figure 4.32. That is because of the generation of inter-metallic mixtures of gold and tin/lead: $AuSn_2$, $AuSn_4$, and others |4.21]. For demanding applications it is required that the gold on the component soldering areas is removed by dipping the component in a molten solder alloy. The gold is rapidly dissolved in the solder alloy, and instead the component gets a layer of solder alloy. (There is a debate about how much gold is needed to harm the solder fillet [4.4, 4.19, 4.20]. A standard requirement is that there should be less than 0.5 % gold in the solder bath and less than 1 % in the solder fillet.)

For integrated circuit packages with leads, the lead frame metal - "alloy 42" or pure copper - is coated with solder alloy by plating or dipping into a solder bath.

Control of the termination metallisation and solderability is an important part of quality control (see Chapter 9).

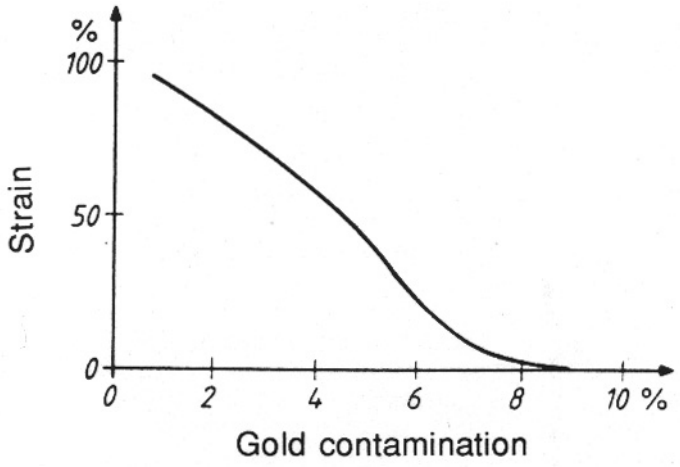


Fig. 4.32: Strain at fracture of solder fillet as function of gold concentration in the solder metal, relative to value without gold [4.20].

4.8 ELECTROSTATIC DISCHARGES - COMPONENT DAMAGE AND PRECAUTIONS

Electrostatic discharge (ESD) is today assumed to be the most important single source of damage of active electronic components, which costs billions of dollars annually. A part of the problem is that ESD is so difficult to document, and it is very difficult to show that a demonstrated damage is caused by ESD. We shall briefly describe how ESD arises, its effect on semiconductor circuits, and how one can take precautions to protect the circuits and avoid damage. Details are given in [4.21].

Tribo-electricity is electric charging by friction. Humans who walk on carpets made of synthetic materials, or who pat a cat, can be charged up to 10 - 20 000 V. The charge is in the range of a few tenths of microJoule, but it can give instantaneous power dissipation of kW during a fraction of a microsecond. Most people have experienced this by the shock they can get by touching a grounded doorknob afterwards. The electronic components may be charged up analogously, either because people handle them, or because of friction against unsuitable plastic packaging, containers, etc. A component that has been exposed to voltages on some of its terminals, while other terminals are grounded will be destroyed instantaneously.

Let us take for example an MOS-transistor, see Figure 4.33. The gate oxide typically is between 20 and 1000 Å thick, and it has a break down field strength 800 kV/mm if the oxide is perfect. That means that if the voltage on the gate is made greater than 1,6 - 80 V, the oxide will break down. This happens by impact ionisation or avalanche breakdown and the subsequent melting of Si, see Figure 4.34, or by destruction of the oxide. The damage may be latent, such that the component still works, but it has been weakened against new ESD. Alternatively, cracks can be created where moisture and impurities accumulate, and the component will be harmed by these elements or materials during exposure over longer periods of time.

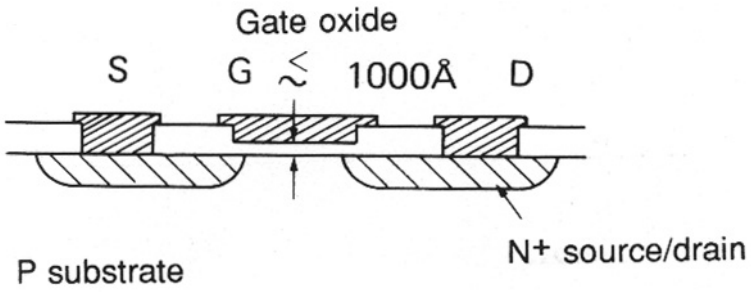


Fig. 4.33: MOS transistor schematically.

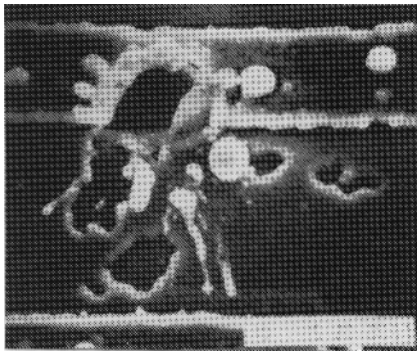


Fig. 4.34: CMOS circuit exposed to electrostatic damage: silicon has molten in a small area (5000 x).

Even bipolar components are sensitive. The P/N junctions in components made by today's technologies are a fraction of a μm deep, with high gradients in the doping concentrations. When voltages of 10 - 50 V are reached the breakdown field strength in Si is exceeded, both for P/N junctions and Schottky barrier junctions.

To increase the tolerance of the components to ESD, modern IC components are made with protection circuits at the in- and outputs, see Figure 4.35. The purpose is to conduct the current from the discharge to the power supply or to ground by diodes that are in the conducting direction for voltages above V_{cc} or below ground level (or below the level of the most negative voltage in the circuit). The protective circuits reduce the performance of the circuit by parasitic capacitances at the inputs, etc., and they require much valuable chip area. It is therefore limited how good the protection is made but with protective circuits components of today typically tolerate 500 - 8000 V discharges.

Additional protection must be made by using suitable component packaging, see below, and by a suitably shaped working area with grounding of operators and equipment, see Chapter 7. Today it is accepted that all components should be treated as if they where electrostatically sensitive to get a total working discipline. Control of the humidity is also of importance since the ESD is worser at very dry conditions.

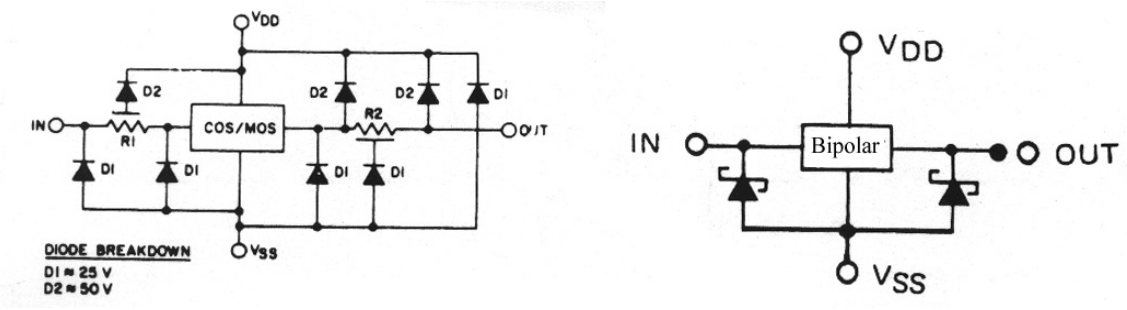


Fig. 4.35: ESD protection circuit at in- and outputs for MOS and for bipolar circuits.

4.9 COMPONENT PACKAGING FOR AUTOMATIC PLACEMENT

It is important for an efficient production process that the components can be bought in a form of packaging which makes handling efficient and that is adapted to automatic placement machines with little or no adjustments.

Hole mounted axial components (resistors, capacitors) are supplied on paper tape. The ends of the components are held between two layers of sticky tape, and the tape is rolled on to a reel. Radial components (capacitors, transistors) are supplied on similar tape. When the components are to be removed from the tape, the leads are cut in the placement machines or in the sequencing machines (see Chapter 7).

The most efficient form of packaging for small surface mounted components (resistors, capacitors, transistors, small integrated circuits, etc.), is the so-called "blister tape", please refer to Figure 4.36. Each component is in a recess in a tape, which is normally made of plastic. A thin protective film is on top, sticking to the tape, so that the components do not fall out.

The blister tape comes in standard formats, of width 8, 12, 16, 24 mm, depending on the component sizes. For the smallest chip components there are 4.000 or 10.000 per reel.

Conductive, metallised plastic tape, or tape made of aluminium, is used for components that are sensitive to electrostatic discharges.

The blister tape is especially well suited for pick-and-place machines mounting SMD components.

For DIP integrated circuits plastic "stick magazines" are the most common form of packaging, see Figure 4.37. Sticks are also much in use for surface mounted integrated circuits. The plastic has an anti static coating to avoid generation of static electricity. Metal sticks are also used to some extent. Even this packaging form is well suited for automatic mounting.

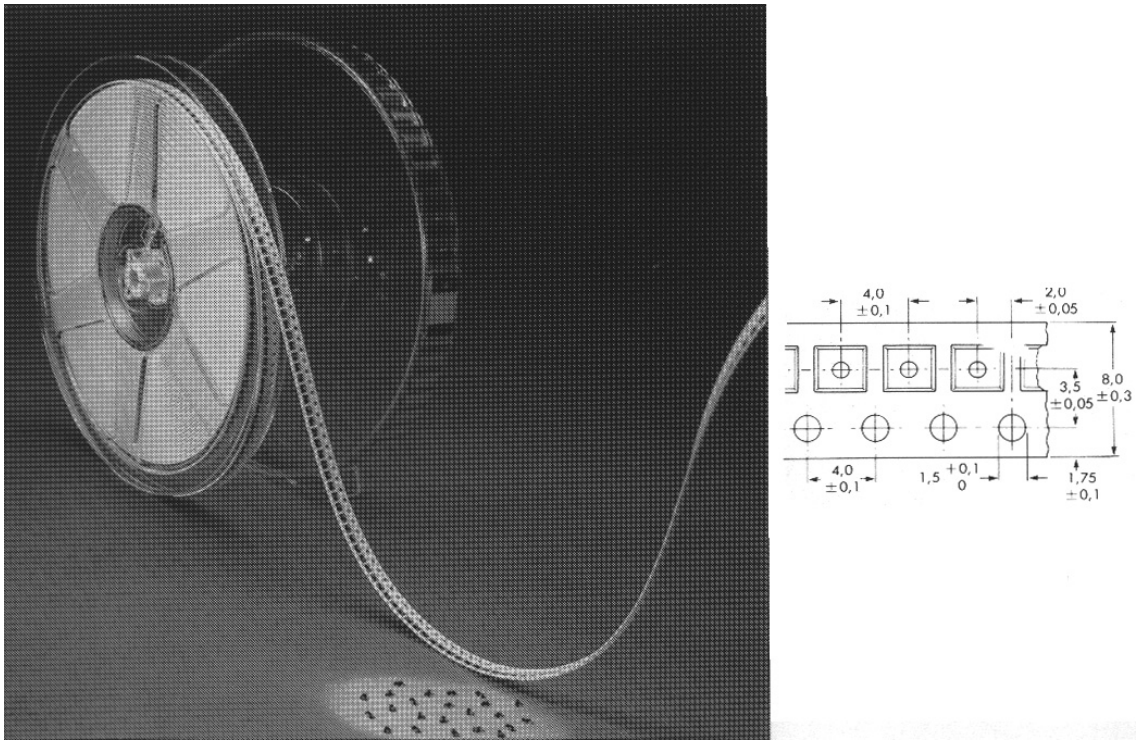


Fig. 4.36: Blister tape for surface mounted components. Standard dimensions for 8 mm wide tape.

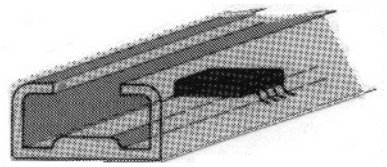


Fig. 4.37: Plastic sticks as packaging for SMD integrated circuits.

For flat packs the so-called "waffle trays" are much used, see Figure 4.38. Here, the components are lying side by side in recesses in a plastic sheet, like chocolate pieces in a box. The sheets are placed layer upon layer on top of each other.

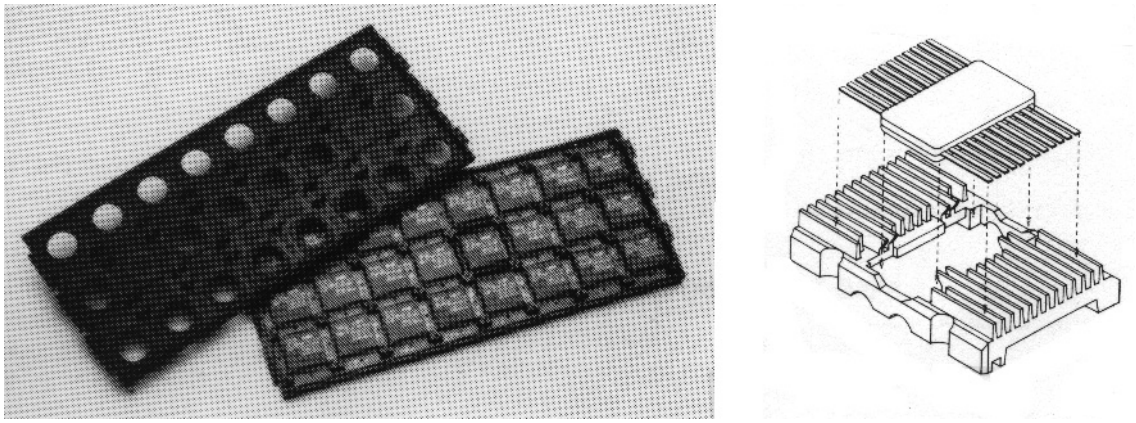


Fig. 4.38: Waffle trays packaging for flatpacks to the left, frame for stacking of single component to the right.

The waffle tray packaging is less suitable for mounting with the ordinary pick-and-place machines (Chapter 7). However, programmable mounting robots can pick components efficiently from such packaging.

Another packaging form for flatpacks is individual plastic frames that can be stacked on top of each other in a magazine, "stack magazines", during transport and mounting.

Components in small quantities are often supplied in bulk, i.e. packed only in a plastic bag. When these components are to be mounted automatically, they have to be oriented in a vibration feeder.

Special components are delivered in many forms of packaging. For nearly all of them, it is a fact that they are poorly adapted to automatic production of the printed circuit boards.

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