CHAPTER 5

PRINTED WIRING BOARDS

5.1 INTRODUCTION

The substrate on which the components are mounted has several purposes:

- Mechanical support for the components.
- Electrical interconnection, "wiring", between components and other parts of the system.
- Conduction of the heat from the components.

The component carrier for printed circuit boards is generally designated printed wiring board. Many people, even with no components mounted often call it printed circuit board. This is confusing and should be avoided. Bare board is also used to some extend. For hybrid circuits and multichip modules it is called substrate (see Chapter 8).

5.2 PRINTED WIRING BOARDS, GENERAL

Strict demands are posed on the properties of the printed wiring board, such as:

- Good electrical properties: High insulation resistance, high break down field strength, low dielectric constant, low dielectric losses.
- Mechanical strength and dimensional stability, under high temperature processing and in field use.
- Chemical resistance against solvents, solder fluxes, and aggressive atmospheres during use.
- Not flammable, even during solder processes at 200 - 260 °C.
- Favourable mechanical processing ability: Easy to drill, mill, and punch.
- Good adhesion between the different materials in the wiring board.
- Low moisture absorption.

The starting material for printed wiring boards is called the laminate, and it consists of many laminated layers of binder and reinforcement. Common binders are epoxy, and for low price consumer products with low requirements on reliability, phenolic. For high performance and demanding applications polyimide and other materials are used, see Sections 5.10 and 5.11. Common forms of reinforcement are woven glass fibres, see Figure 5.1, and paper for low price laminates. Quartz and aramid (Kevlar) are used to a limited extent, they are costly and difficult to process [5.4]. Table 5.1 shows different types of conventional printed wiring board materials. Various other materials are under development for high performance boards, see Sections 5.10 and 5.11.

Today, glass/epoxy laminates are the most common; particularly the type that is designated FR-4. FR means flame retardant, contrary to the earlier materials that might start burning during the wave solder process or during other unfavourable conditions.

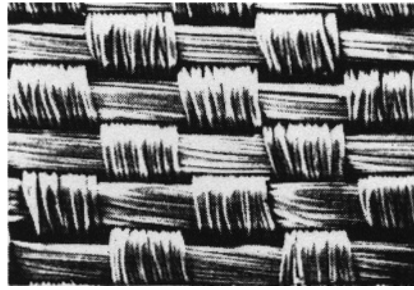


Fig. 5.1: Woven glass fibre for printed wiring board reinforcement.

Table 5.1: Conventional laminates for printed wiring boards. (The designations are according to National Electrical Manufacturers Association, NEMA, USA.)

				Reinforcement				Flame
	Resin			Cotton	Woven	Mat	Glass	retard-
Grade	Epoxy	Polyester	Phenolic	paper	glass	glass	veil	ant
XXXPC			*	*				
FR-2			*	*				*
FR-3	*			*				*
FR-4	*				*			*
FR-5	*				*			*
FR-6		*				*		*
G-10	*				*			
CEM-1	*			*	*			*
CEM-2	*			*	*			
CEM-3	*				*	*		*
CEM-4	*				*	*		
CEM-5		*			*	*		*
CEM-6		*			*	*		
CEM-7		*				*	*	*
CEM-8		*				*	*	

Figure 5.2 shows the composition of printed wiring boards, of various degrees of complexity. The simplest type, see Figure 5.2 a), has only one layer of copper metal foil for conductors, on one side of the board. Surface mounted components are mounted on this side, whereas hole mounted components are mounted on the opposite side, with leads passing through holes in the board. For boards that are more complex, we need wiring on both sides. It is common to have conducting connections between the two sides in plated through via holes, see Figure 5.2 b). The surface of the conductor pattern may be copper or alternatively tin/lead solder metal, which is also plated. Both types have advantages and disadvantages, see Section 5.6.2.

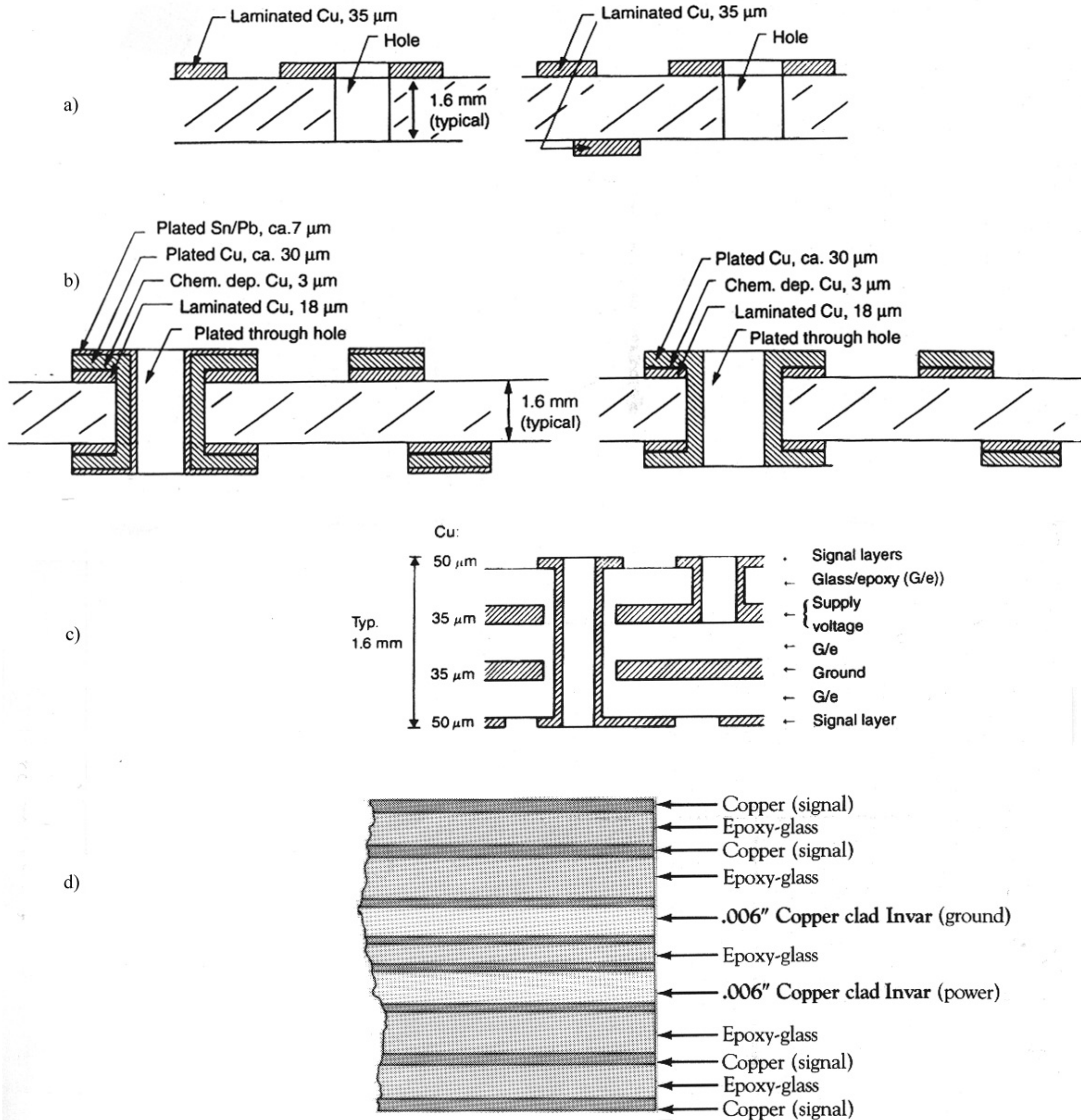


Fig. 5.2: Printed wiring board structures with varying complexity:
a) Single sided and double sided.
b) Double sided through hole plated with bare Cu or Sn/Pb surface.
c) Four layer board.
d) Six layer board with two Cu/Invar/Cu cores.

More complex circuits with a very dense component placement and VLSI components with many inputs and outputs, often require more than two layers of

interconnect wiring, and it is necessary to use multilayer wiring boards, see Figure 5.2 c). They have plated through via holes through the whole board, but they may also have via holes through parts of the board, see Section 5.7. For circuits with high heat dissipation one or more thick metal cores are used, each metal core may be composed of several laminated sheets of metal, see Figure 5.2 d). This composition has several advantages, see Section 5.9.

5.3 GENERATION OF DESIGN DATA, PHOTO- OR LASER PLOTTING

The wiring board design, from net list and schematics to conductor pattern layout is normally made on a computer assisted design system (CAD), where detailed component information is stored, including geometrical information about the solder lands for each type of component (see Chapter 6). The CAD system also has stored information about minimum conductor distances, minimum conductor width and other design rules, and it gives a warning if the designer attempts to break these rules. The designer enters net list and component placement into the CAD system, he generates the circuit diagram, performs simulation and routing of the conductor pattern. The routing may to a large extent be done automatically, but the designer can choose to specify critical paths manually.

The layout consists of information about:

- Component placement.
- Conductor pattern between the components, in one or more wiring layers, solder lands and hole pads.
- Holes for component leads, via holes for electrical contact between different conductor layers, registration holes for accurate positioning of the circuit board during solder processing and component mounting.
- Contour of the board.
- Printing mask for solder resist and solder paste printing, etc.

The information in the CAD system is post-processed to a format suitable for the further processing, which is photo- or laser plotting. One also obtains information for numerically controlled drilling and milling machines that are needed for production of the wiring board, pick-and-place machines, testing and test fixtures, component listing for purchase, drawings and other documentation.

The photo plotter, please refer to Figure 5.3, generates photographic films that correspond to the different patterns on the wiring boards: Conductor patterns with solder lands, solder resist, solder paste print, component marking for the mounting, etc.

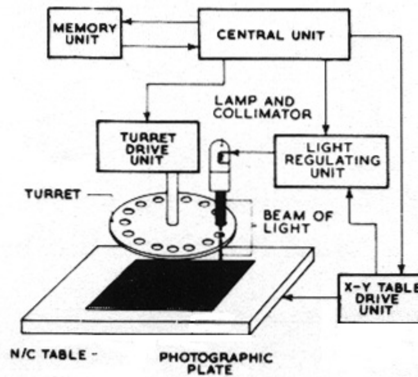


Fig. 5.3: Photo plotter, schematically.

The film that is to be plotted in the photo plotter, lies on moveable a table, which can be moved in the x- and y-direction, controlled by the data from the CAD system. A light source illuminates the film over a small area at a time, through a so-called plot wheel. The wheel has openings of different sizes, so it is possible to choose the size of the film area that is illuminated at any time. We can illuminate lines with constant width by moving the x - y table while the light goes through a particular opening. The width of the conductor can be changed by rotation of the wheel, bringing a different opening into position. A single flash illuminates a circular area, and areas of complex form are made by moving the table back and forth and "paint" with a small light spot. The whole illumination process is done automatically. Then the film is developed.

The laser plotter is on its way to take over from the photo plotter. In the laser plotter a laser beam sweeps across the film, line by line, while it is turned on and off depending on whether the points on the line are to be blackened on the film or not.

5.4 FABRICATION OF GLASS/EPOXY WIRING BOARD LAMINATES

Epoxy resin is generally made from ethylene chlorohydrin and bisphenol-A [5.1, 5.3, 5.9 b, 5.21]. When the material is heated under pressure, the process called polycondensation takes place between these materials and the cross-linking of the polymer starts. It is still not completely cured, but in the so-called B-stage (see Chapter 3). The material melts at high temperature, and in this state it is soluble in suitable chemicals.

The laminate is made from many layers (typically 7-10) of woven glass fibre that are saturated with resin in the B-stage. They are placed layer upon layer in a lamination press, with one layer of copper foil on one or both sides, depending on what sort of wiring board is being made. High pressure and high temperature in the lamination process cause the resin to melt and create a uniform material. At that time the rest of the polymerisation process to the C-stage takes place, and we get a complete glass/epoxy material that is highly resistant to chemicals and climatic exposure.

The most common thickness of the laminate is 1.6 mm, with 18 or 35 μm Cu foil (also called 1/2 or 1 ounce, because of the weight per square foot of the copper foil). The metal is rolled or electrolytically deposited.

This process is only done by a few large specialised firms. For one or two layer wiring boards, a laminate with copper foil in large panels is the starting material for the wiring board producer. For production of multilayer boards the producer of the wiring boards must also do a laminating process, see Section 5.7.

5.5 SINGLE SIDED WIRING BOARDS

The simplest way to define the conductor pattern on single sided wiring boards is the so called print and etch process [5.1], that is suitable for coarse conductor pattern.

We start with a laminate of paper/phenolic, glass/epoxy or a mixture. After cutting to suitable standard sizes, the main steps of the "print and etch" processes are as follows, please refer to Figure 5.4:

1. Drilling or punching of registration holes.

2. Panel cleaning: Mechanical brushing or chemical rinse (light etch) to remove oxide, grease etc.

3. Printing of etch resist: An organic material that is resistant to the etch bath for the subsequent etching process is screen printed on to the surface through a printing mask with the correct conductor pattern, see Chapter 3. The etch resist is cured at elevated temperature or with UV illumination.

4. Etching: This takes place by dipping the panel into an etch bath, or using an etching machine that sprays etchant uniformly over the whole surface, until all copper has been dissolved where it is not covered by etch resist. Common etchants are solutions of $CuCl_2$ or $FeCl_3$. Then the panel is rinsed.

5. Stripping: The etch resist is dissolved in a suitable solvent.

6. Printing of solder resist: An electrically insulating, organic layer (for example an epoxy), is screen printed on top of the conductor pattern, with openings for the solder lands and hole pads for the component holes.

7. Curing of the solder resist, in heat or in UV light, to evaporate the solvents and increase the resistance to chemicals and thermal and electrical stress.

8. Cleaning of the copper solder areas: At this stage of the process, the copper is oxidised, and the panel is exposed to a mild micro etch with subsequent cleaning, to get good solderability.

9. Deposition of solder coating: To avoid oxidation of the copper and to protect the solderability during storage, a thin solderable layer (about 1 µm thick) of organic material is often deposited by dipping or by roller coating.

10. Punching of holes and edge contour, or drilling/milling: Paper/phenolic and certain other materials can be punched, which is the most efficient method at high production volumes. Glass/epoxy will quickly damage the punching tool, therefore holes are instead drilled and the edge contour is milled by numerically controlled drilling and milling machines.

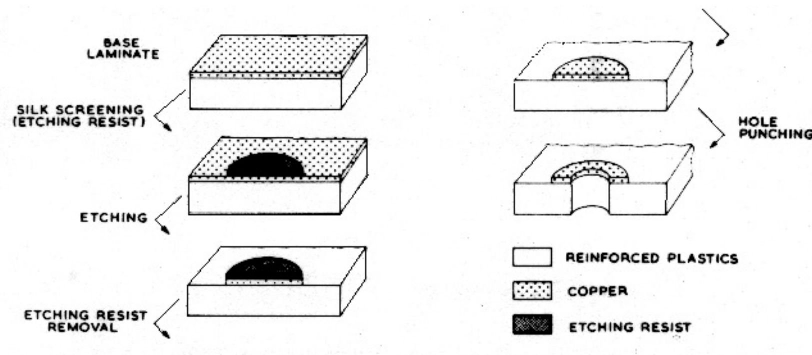


Fig. 5.4: Process steps of "print and etch" process.

This is a subtractive process. That means that the conductor pattern on the boards is defined by removing material (etching of the copper). Additive processing, where one builds up the conductor pattern, is described in Section 5.8.

There are several modifications of this process, such as the following in step 3: To fabricate narrow and complex conductor patterns the pattern is defined photographically (please refer to Section 3.4), instead of screen printing. A photo sensitive dry film resist is laminated on to the panel. It is negative, meaning that after illumination the non-illuminated parts of the resist are removed. The panel is illuminated through a negative film, meaning that the conductor pattern on the film is transparent, while the rest is black. The dry film remaining after development serves as an etch mask.

A third alternative for etch resist is to use plated metal instead of organic material, and in this case tin/lead is selectively plated. The process is described in Section 5.6.

5.6 DOUBLE SIDED THROUGH HOLE PLATED BOARDS

Double sided, through hole plated wiring boards are the most common used type for industrial electronics. They are normally made from glass/epoxy. A key factor is that we have conducting connections from one side to the other side of the board through via holes. Many different versions of the process are available to make such boards. Here we will describe two of them: Panel plating and pattern plating. (A thorough description is given in [5.1, 5.3, 5.21]).

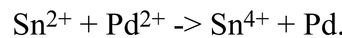
5.6.1 Process

We start with a glass/epoxy laminate with double sided Cu foil, normally 18 μm thick. The process for panel plating is as follows, please refer to Figure 5.5:

1. Drilling of registration holes, component holes and via holes.

2. Cleaning of the surface and holes ("deburring"), and a mild etch to ensure adhesion in the subsequent steps 3 and 4.

3. Activation for chemical plating: The panel is dipped into a solution containing Sn^{2+} ions, to increase the sensitivity of the surface. The Sn^{2+} ions are adsorbed on the surface. The activation takes place in an acidic solution of palladium chloride, that is transformed into metallic Pd. Reaction:

   $$Sn^{2+} + Pd^{2+} \rightarrow Sn^{4+} + Pd.$$

   In the plating process, Pd catalyses the deposition of copper. (There is still some doubt about the detailed mechanism, see [5.2]).

4. Chemical plating [5.1, 5.2] of Cu: The panel is dipped into a reducing bath containing Cu^{2+} ions for example in the form of dissolved $CuSO_4$. Formaldehyde, HCHO, is the common means of reduction. In this bath, Cu^{2+} is reduced to Cu that covers the whole surface, including the holes, also where the surface is electrically insulating. At the same time formaldehyde is oxidised into acetic acid.

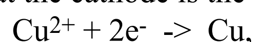
   The plated thickness is approximately 3 μm. The purpose is to create an electrically conducting surface everywhere, for the subsequent step.

   The chemical plating is very critical. The composition of the bath is complex, and if the composition, temperature, "bath loading" (the ratio between plated area and bath volume) is outside acceptable values, Cu^{2+} may be reduced to metallic Cu in the bath itself, which is then ruined.

5. Electrolytic plating of Cu: The panel is dipped into an electrolyte that contains Cu^{2+} ions, such as $CuSO_4$ dissolved in H_2SO_4. The panel forms the negative electrode (cathode), and a metallic copper plate forms the positive electrode (anode) of an electrolytic cell. At the anode copper is dissolved:

   $$Cu \rightarrow Cu^{2+} + 2e^-.$$

   The reaction at the cathode is the following:

   $$Cu^{2+} + 2e^- \rightarrow Cu,$$

thus, metallic copper is deposited on the panel. Approximately 25 – 30 μm Cu is normally plated, in order to get good coverage in the via holes.

6. Pattern definition: Dry film photoresist is laminated on to both sides, normally negative resist. The resist is illuminated through a positive photographic mask and is developed. The pattern is therefore black on the photomask, and the photoresist will dissolve where there is a pattern, during the development.

7. Tin/lead plating for etch masking: The panel is connected to the cathode of an electrolytic bath containing Sn^{2+} and Pb^{2+} ions. The anode is metallic Sn/Pb alloy. The electrolyte is based on fluoroboric acid, HBF_4. The ratio between the concentration of the ions in the bath and on the anode, is such that the deposited layer of metal on the panel will be approximately the eutectic mixture 63Sn/37Pb (percent by weight). The normal thickness is about 7 μm. After this the photoresist is dissolved in a suitable solvent, for instance methylene chloride.

8. Etching: The Cu foil is etched simultaneously on both sides, analogous to step 4, Section 5.5, but with an ammonia-based etch bath, which does not attack Sn/Pb. The plated Sn/Pb serves as an etch resist. After the etching, the Cu is covered with Sn/Pb where we want conductor pattern and solder lands, as well as in the holes through the board.

9. If it is desired to have Sn/Pb on the completed board, a "fusing" step follows. It consists in heating of the board to a temperature where the alloy melts and changes its crystalline structure. It flows and covers the nearly vertical edges of the etched copper. We get an intermetallic copper/tin interfacing layer. The heating may take place in hot air or oil, by IR radiation heating, etc.

The tin/lead layer serves two purposes: It is both an etch mask and it makes a durable, solderable surface.

If one wishes clean copper surface on the completed boards, a new etching step replaces step 9. In this step the Sn/Pb is removed.

Finally, organic solder resist is deposited, as described in steps 6-7 in Section 5.5. For boards with pure copper surface, a solder coating may also be deposited.

In a slightly different process, pattern plating, the pattern is defined with photoresist after drilling of the holes and activation, step 3, see Figure 5.5. The copper is then plated only at the desired conductor pattern and in the holes. Then tin/lead is deposited and the photoresist is stripped. The copper is etched, but in this process it is only the original thickness (17 μm) which has to be etched away. In this way, waste is reduced and improving pattern definition is obtained by reduced underetch (Section 5.8.1). This process dominates today.

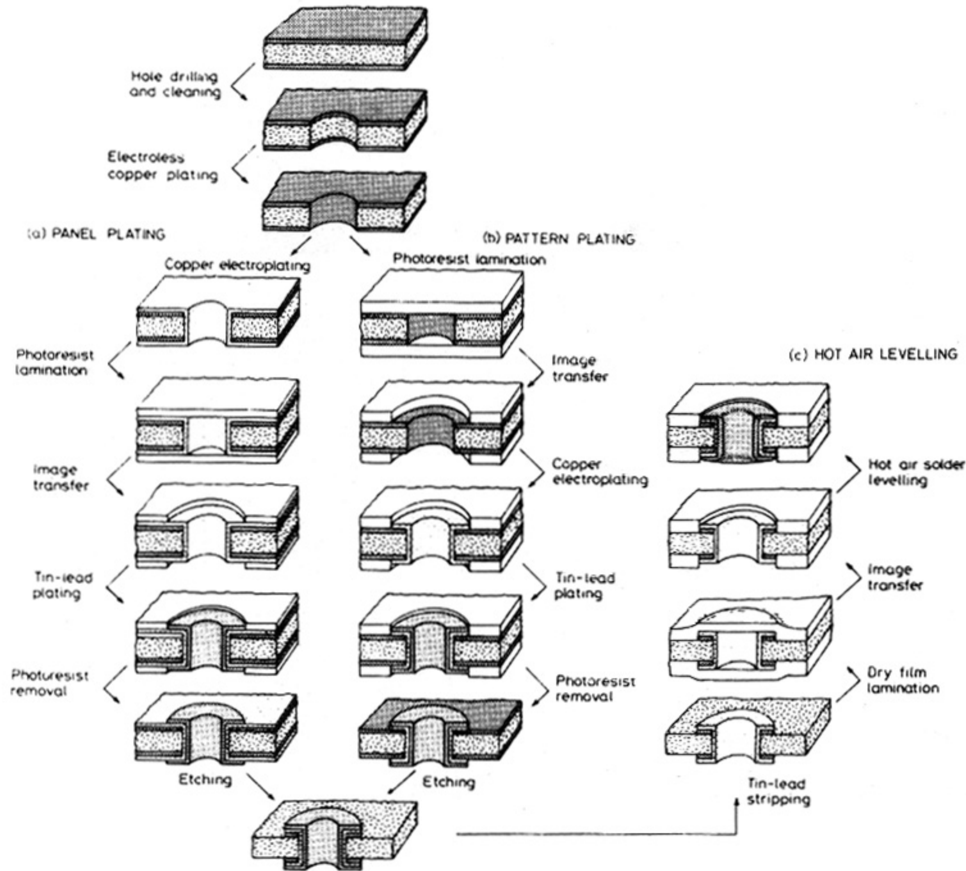


Fig. 5.5: Through hole plated PWB, process steps: a) panel plating, b) pattern plating, c) hot air levelling.

5.6.2 Choice of surface metallisation and solder resist

A tin/lead layer on the surface will react with the copper underneath, during long time storage before component mounting and soldering. An intermetallic compound is created, which is not solderable. If this has occureded, the wiring boards must be discarded. It is customary to allow a maximum storage time of one year, which is rarely a limitation nowadays, since all storage is attempted to be reduced to a few days. (The storage time may still be of importance for spare boards for repair.)

A drawback of greater practical importance shows up after assembly and soldering of the components: All the tin/lead layer melts during the soldering process, even that which is on the conductors underneath the solder resist. At extended conductor areas for ground planes and wide, high current conductors, the solder metal is re-distributed and it will create big wrinkles, drops and "bags". This is normally not acceptable for aestetic reasons. Another potential problem arises when conductors are located close to one another. Between the neighbouring conductors, there may be small openings underneath the solder resist, and the tin/lead may create short circuits when it melts. For this reason, a bare Cu surface underneath the solder resist is required in many cases.

Bare Cu on the solder areas has another handicap: It will oxidise and give a reduced solderability. Particularly for surface mounting of components with small/narrow component terminals, the demands for good solderability are very rigid.

In addition to the two main types of surface, tin/lead all over or bare copper all over, we have a third type with tin/lead deposited only on the component solder pads and in the component holes: Selective tin/lead deposition or "hot air/hot oil levelling", see Figure 5.6. In this process the panels with bare Cu, and solder resist deposited, are dipped in to a bath of molten solder alloy, so that tin/lead wets all copper areas that are exposed. The hot, strong air (or oil) stream blows off superfluous tin/lead on the surface and in the holes, so only a layer 20 - 100 μm remains. Normally this is considered the best type of surface metallisation.

The printing process for solder resist gives relatively poor dimension control, typically 0.3 - 0.5 mm. Often smaller distances than this are needed between the solder lands and electrical insulation on the surface, by high component density and high conductor density. Then an organic, photosensitive solder resist is used which is deposited all over the board area. One type is a relatively thick foil (typically 75 μm), that is laminated on the board in vacuum. It is designated dry film. Another type is printed on in liquid form, but also over the whole area. It is called wet film. In both cases the solder resist is exposed through a photographic film to make openings for solder lands, etc. Then it is developed and cured. With such photo-processable solder resist, the distance to the solder lands can easily be reduced to 0.1 - 0.15 mm (see Chapter 6, Figure 6.4). The thick dry film may in certain instances give problems with soldering of SMD components: Instead of getting contact between the terminals and the solder lands and solder paste, the component body may "ride" on the dry film, and the solder metal may melt without soldering the terminals. This can be avoided by a suitable design of the printing stencil for the solder paste, in a way that ensures that the solder paste is deposited with sufficient thickness.

The dry film on the other hand has an advantage: it may cover via holes such that they are plugged ("tenting process"), see Figure 5.6. We avoid then getting solder alloy into the holes during wave soldering, which may create problems. We also get the advantage of "vacuum-tight" holes during testing, when the boards are sucked to the test fixture (see Section 7.6).

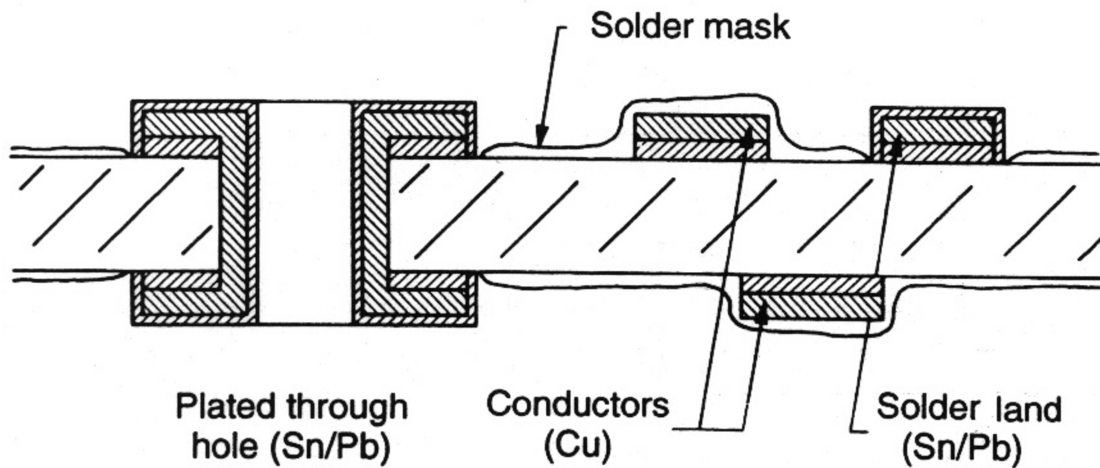


Fig. 5.6.a: Selective Sn/Pb surface coverage with hot air levelling. The alternatives, bare Cu or Sn/Pb on all Cu surface, are shown in Figure 5.2 b).

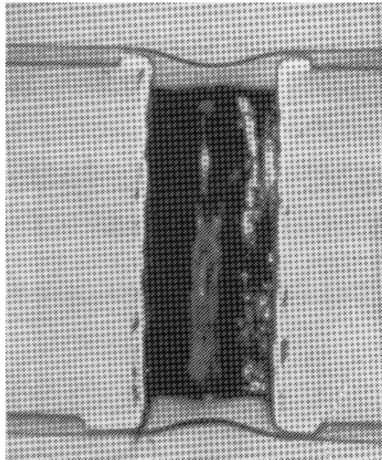


Fig. 5.6.b: "Tenting", i.e. covering of the via holes by dry film solder resist.

5.7 MULTILAYER PRINTED WIRING BOARDS

Multilayer printed wiring boards are laminated together by several double sided boards, inner layer and outer layer, with "prepreg" between. For glass/epoxy based boards the prepreg material is glass fibre impregnated with epoxy, then cured to the B-stage.

The most common types of multilayer boards only have via holes that run all the way through the whole laminate. For a 4-layer board the process is as shown in Figure 5.7:

1. Drilling of registration holes in all layers. Chemical/mechanical rinse.

2. Conductor patterns on the panels with inner layers are defined by photo processing.

3. Conductor patterns on the inner layers are etched, and the panels are rinsed.

4. "Black" or "brown"-oxidation of the Cu-surfaces: These are special oxidation processes in high temperature, which have the purpose of giving a rough surface and improving the adhesion in the lamination process following later.

5. Baking: Heating of the panels to evaporate water and solvents.

6. Lamination: The panels are placed on top of each other with accurate registration by guiding pins in the registration holes, with a single sided panel for outer layer on top and at the bottom, and prepreg between each panel. The stack is pressed together in a lamination press typically at 10 - 25 atmospheres of pressure at 170 °C, for 30 - 90 min. In this process the epoxy softens in the prepreg material, fills all non-uniformities, and polymerises completely to the C-stage.

7. Drilling of via holes through the board for subsequent through hole plating. The drilling process is more critical than for double sided boards, because here we must have electrical contact between the hole plating and the inner layer conductor layers at certain places. Often the epoxy softens and creates an insulating layer on the walls of the holes ("smearing"). To remove this layer, an etch process is used, often plasma etching ("de-smear").

The subsequent processing for pattern definition on the outer layers, through hole plating, etc., is similar to that for double layer through hole plated boards, Section 5.6.

"Buried via holes" are plated holes that connect inner layers, without appearing at the surface, please refer to Figure 5.8 b. Such holes occupy space only on the layers where they have the electrical function to connect neighbouring layers. However, making them require that the inner panels are processed as complete double layer through hole plated boards before the lamination process. The completed boards will be denser, but more expensive. "Blind via holes" connect an outer layer to an inner layer, please refer to Figure 5.8 c). They may be made with precise laser- or regular drilling after the lamination has been carried out, see Figure 5.8 d.

Multilayer boards permit complex interconnection patterns. Normally we put voltage supply and ground on separate inner layers with extra thick Cu foil (typically 70 μm). This way of design gives significantly better noise properties for the completed circuit; both reducing sensitivity to external electromagnetic fields and reducing radiation ("electromagnetic compatibility", EMC). This is of special significance for circuits with high signal frequencies and digital circuits

with short pulse rise- and fall time. For such boards a controlled characteristic impedance is also needed, see below, Sections 5.11 and 6.7.

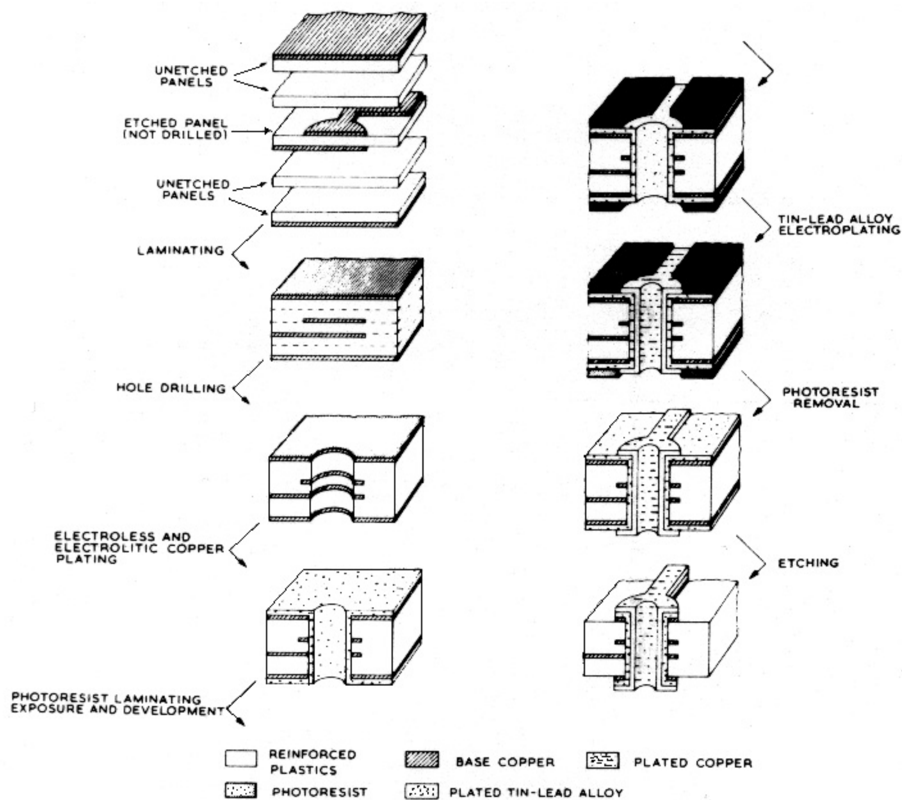


Fig. 5.7: Process steps for multilayer printed wiring boards with holes only through the board.

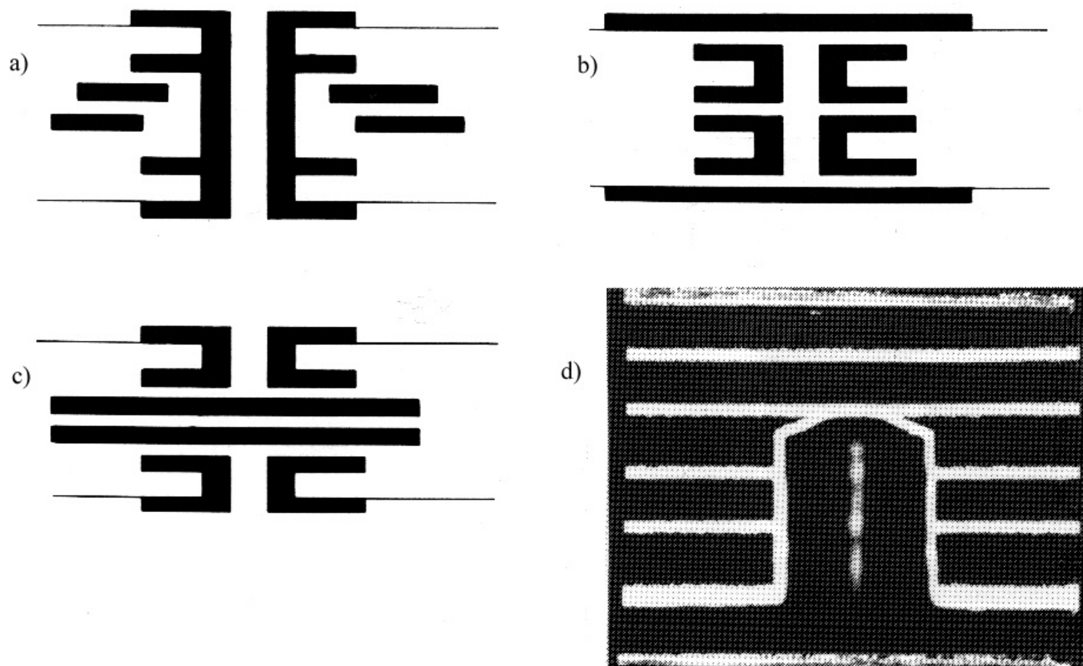


Fig. 5.8: Types of via holes: a) Through hole. b) Buried hole. c) Blind hole. Figure d) shows a microscope section of a drilled blind via. (Contrave´s "Denstrate" process).

Multilayer boards with 12 - 16 layers are quite common, with up to 40 - 50 layers being made. However, the process becomes very costly, and the production yield becomes low, particularly when the conductor widths and the via pads at the same time are small, and the aspect ratio for the via holes (the ratio of hole length to hole diameter) is high.

5.8 FINE LINE WIRING BOARDS, ADDITIVE PROCESS

The demand for high component density and high density of conductors on the printed wiring boards is steadily increasing. While advanced boards in 1965 could be made with 0.3 mm conductor width, today we are below 0.1 mm, see Figure 5.9 a). The limitations are in the etching and other parts of the process.

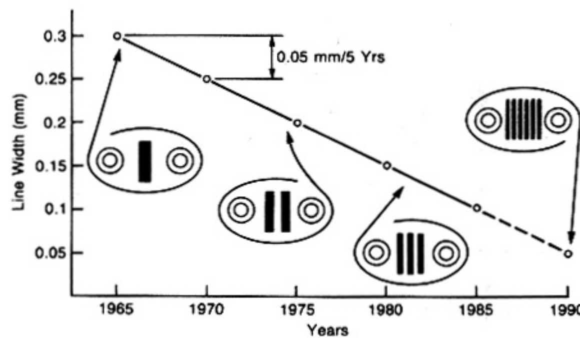


Fig. 5.9 a): The development of minimum line width from 1965 until 1990. The figures in the ovals tell how many conductors can be positioned between the leads of DIP-components with a lead pitch of 0.1" (number of "channels").

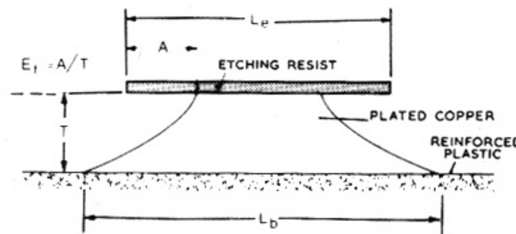


Fig. 5.9 b): Underetch and etch factor.

5.8.1 Limitations in dimension control due to etching

By etching of copper foil we get an undesirable lateral etching at the same time as the etch dissolves copper downwards. This is called underetch, see

Figure 5.9 b). Please refer to also Figure 2.10, Chapter 2. The degree of underetch may be defined by an etch factor E_f:

$$E_f = A/T,$$

where A = sideways etching and T = the thickness of the copper foil. In practice E_f is between 0.7 and 3, the lower the better. At the bottom the conductor normally becomes wider than the nominal width, $L_b > L_e$.

There is always some uncertainty in the etching speed of the bath. Therefore, we need to use a longer etching time than the ideal time to be sure to etch through the thickness of the foil. This gives an increased underetch. To some extend it can be compensated for by designing the conductors somewhat wider than what we need in the completed wiring board.

Control of the conductor width is important: With too much underetch we get, in the worst case, a discontinuity of the conductor. If the conductor is too narrow, the conductor resistance increases and the maximum current carrying capacity of the conductor is reduced (see Section 6.3). For high frequency circuits with constant characteristic impedance, the conductor width is one of the dimensions that determines the impedance (see Section 6.7). Variations in the conductor width on the wiring board therefore will give variations in impedance and poor high frequency performance of the circuit.

These factors limit how narrow conductors we can make in a subtractive process, particularly when the foil is thick. To make the conductors narrower, the foil that is to be etched must be thinner, or a fully additive technique must be used.

5.8.2 Fine line wiring boards

As the electronics gets more complex, the need for high conductor density increases. By use of smaller conductor widths and distances, we can also manage with fewer conductor layers in a multilayer wiring board. To utilise the space we save, the via holes must also be smaller.

Conductor widths and distances below approximately 150 μm are called "fine line" dimensions, as opposed to the normal 0.2 - 0.4 mm. While normal via holes are 0.5 - 1 mm in diameter (Section 6.3), "mini-via" holes are made with diameter down to 0.3 mm and below. They may also be made without the Cu pad around them, to save even more space.

Fine line processing uses Cu foil with thickness down to 5 - 10 μm, to reduce the underetch. Careful process control and extreme cleanliness are needed, including an accurate control of temperature and humidity to avoid uncontrolled thermal expansion during the processing [5.5]. High precision films for patterning are needed, and the illumination must be done with collimated light under clean-room conditions, see Figure 5.10. Alternatively, the photoresist is illuminated on each laminate directly with a controlled laser, without use of a photo mask.

The production yield becomes lower the smaller the line widths are. The practical limit today is 75 - 100 µm, without resorting to more untraditional processes. Holes down to 0.2 mm diameter have been used in Japan.

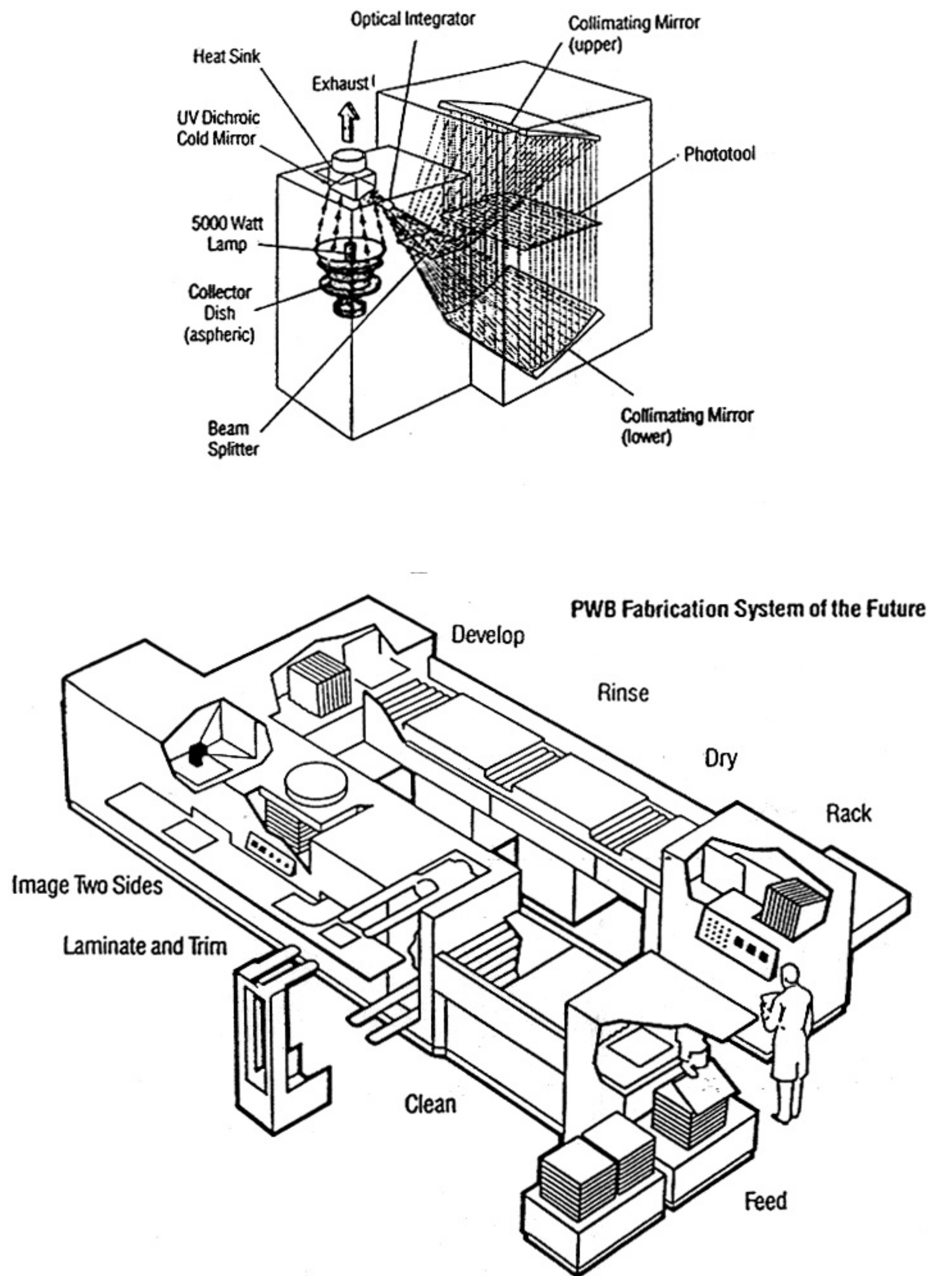


Fig. 5.10: Top: Machine for double sided illumination with parallel light, for pattern transfer from photographic film for fine line printed wiring boards. Bottom: Automatic in-line system for lamination of photoresist, illumination and development, in an enclosed clean room atmosphere [5.5 b].

5.8.3 Additive process

The conductor pattern is defined by etching in subtractive process, as discussed above. The plating is an additive process, meaning that material is built up. The procedure described in Section 5.6 is a combination of the two.

It is also possible to generate conductor pattern in a completely additive processing [5.1, 5.2]. In this case we start with a bare laminate, without Cu foil on top of it. Cu is deposited selectively, only where we need wiring pattern. To achieve this, chemical plating must be used throughout, because we can not obtain external electric contact to all leads as required for electrolytic plating.

The advantages of additive processing are:
- Finer patterns (smaller conductor widths and distances) are obtainable, because we have no underetch.
- There will be less waste of raw materials (copper, etching chemicals), and less environmental problems.

The disadvantages are:
- The processing is slow, more complex and more costly.
- Proper adhesion between Cu and the laminate may be difficult to achieve.

To achieve good adhesion small quantities of metal salts and oxides are added in the base laminate to catalyse the plating process. Alternatively, one can deposit a layer of a special coating on the surface, or treat the laminate chemically to roughen the surface.

The main steps in such a process are, see Figure 5.11:

1. Drilling of holes.

2. Surface treatment: etch in H_2SO_4 or similar.

3. Activation for chemical plating.

4. Pattern definition: Photoresist application, exposure through photo mask, developing.

5. Chemical plating: The plating is selective, on the activated surfaces that are not covered by photoresist.

6. Stripping of the photo resist.

7. Printing of solder resist. (Alternatively: Use of photo-processed solder resist).

As previously mentioned the chemical plating is a sensitive and slow process. The "semi-additive" process is somewhat less sensitive. Here the chemical plating (approximately 5 µm) is done uniformly over the area before step 4, and electrolytic plating is used in step 5. After step 6 approximately 5 µm are etched from the whole surface, so that we end up with Cu only on the desired pattern.

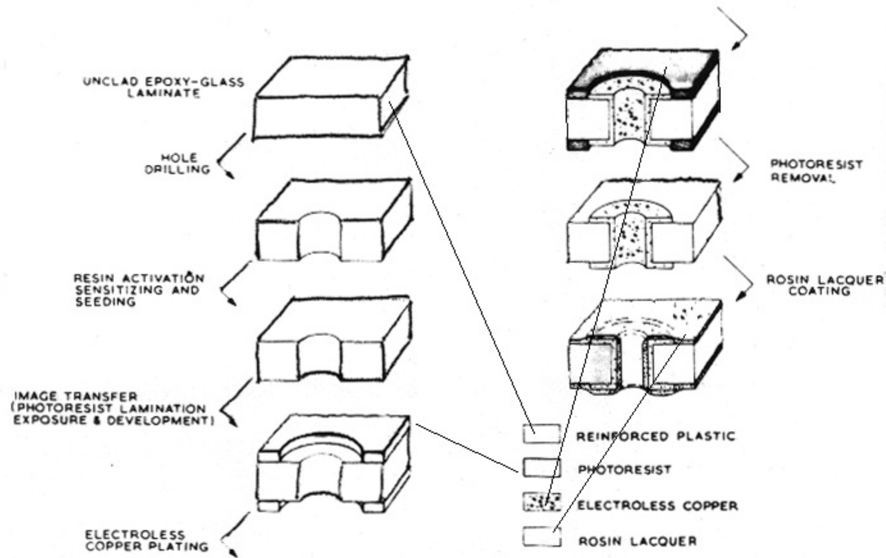


Fig. 5.11: Additive process: process steps.

5.9 METAL CORE BOARDS

For surface mounted printed circuit boards with large leadless chip carrier packages we need thermal compatibility, meaning nearly the same thermal coefficient of expansion (TCE) for substrate and component. This can be obtained by one or two metal cores in the wiring board, composed of a combination of metals with low TCE: "metal core boards", see Figures. 5.2 d) and 5.12 a) - b). The most common metal core combination is a copper/Invar/copper structure, (copper clad Invar) for example 12.5/75/12.5 % thickness ratio, see Figure 5.12 b). Invar has TCE 1.7 ppm/°C [5.3], which is lower than ceramic. By choosing the thickness of each layer of the laminate correctly, one may "design in" the desired TCE for the complete wiring board. If a thick core is used, the expansion of this core will determine the expansion of the whole wiring board. If not, we also have to take into consideration the glass/epoxy and the Cu foil in the other layers. Due to the temperature variation of the properties of the materials and due to standardisation of the thicknesses available, the match will not be ideal [5.6], but it will be good enough even for very demanding requirements. More details about thermal design will be discussed in Section 6.6.

Another advantage of the metal core board is that the thick metal gives excellent thermal conductivity and effectively spreads the heat away from components with high power dissipation. The boards will however be much more costly than ordinary FR-4 boards (typically 4 - 5 times price difference).

The production of metal core boards is similar to that of ordinary multilayer boards. The holes in the core may be drilled or etched before the core is laminated together with the other layers.

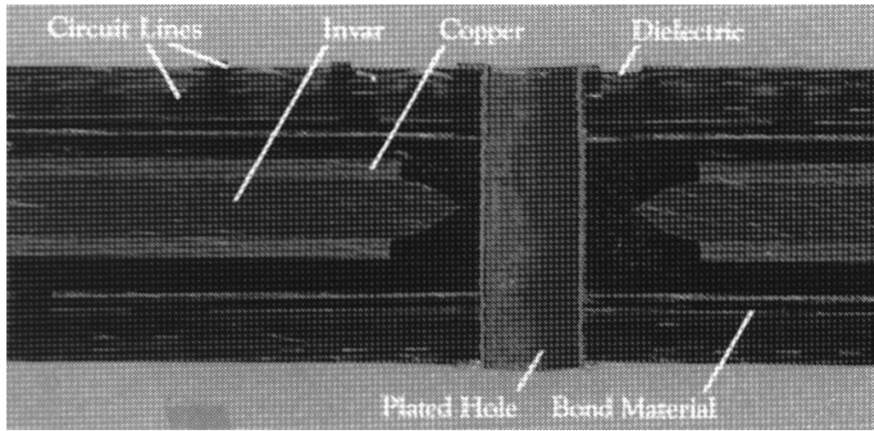


Fig. 5.12 a): Cross section of metal core board with one Cu/Invar/Cu core (Texas instruments).

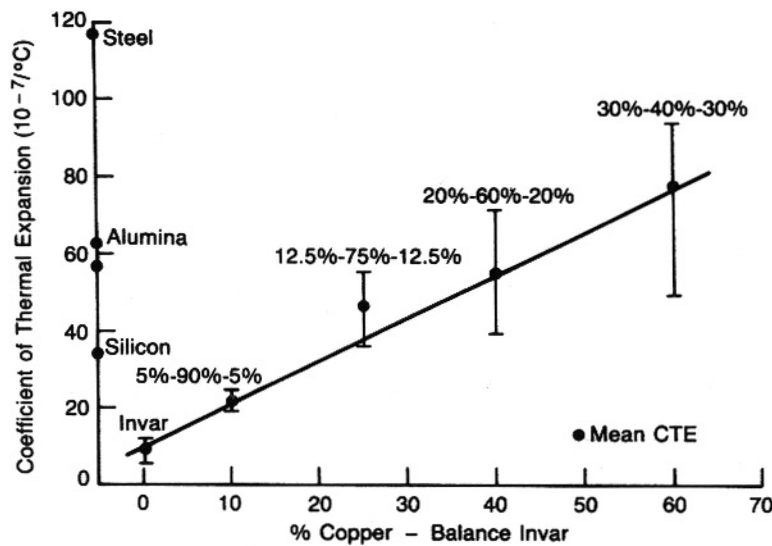


Fig. 5.12 b): Thermal coefficient of expansion of Cu/Invar/Cu, as function of the composition (Texas instruments).

Many other materials have been used for making surface mounted circuit boards with adjusted thermal coefficient of expansion and better properties at high temperature than glass/epoxy: Kevlar/epoxy, kevlar/polyimide, quartz/polyimide, metal core boards with molybdenum, tungsten, etc. instead of Invar. There are positive and negative properties to be found in each of them and have not found very broad use as of today [5.4].

For power electronics that dissipate very high power but are normally simple in their circuit function, a thick aluminium core, insulated with an anodic aluminium oxide layer and a layer of epoxy is often used, please refer to Chapter 8.

5.10 NEW MATERIALS FOR DEMANDING WIRING BOARDS

When thermosetting polymer materials are heated to temperatures above their glass transition temperature T_g, non-reversible material changes occur after a short time (see Section 3.3), which may damage the materials and the wiring boards. The thermal coefficient of expansion is drastically changing when T_g is past, see Figures 3.7 and 5.12. At the same time the polymer softens.

Epoxy with fibreglass reinforcement in the x-y direction is anisotropic, see Figure 5.13. The thermal coefficient of expansion, α_{FR-4} in the x-y direction is a weighted average of the value for glass fibre (α_{gf} = 3 - 5 ppm/°C), and epoxy. Below Tg (≅ 120 °C) the expansion coefficient of the epoxy is α_{ep} ≅ 40 - 60 ppm/°C, and α_{FR-4} ≅ 12 ppm/°C (slightly different in the x and the y direction due to the direction of the weaving of the fibreglass). In the z-direction, the coefficient of expansion generally is determined by the epoxy, because the glass fibre does not limit expansion of the epoxy in the z-direction.

When T_g is exceeded, α_{gf} will dominate strongly in the x-y direction, because the epoxy is soft, and α_{FR-4} is reduced, see Figure 5.13 a. In the z-direction, however, α_{FR-4} will increase correspondingly as for the epoxy alone, see Figure 5.13 b.

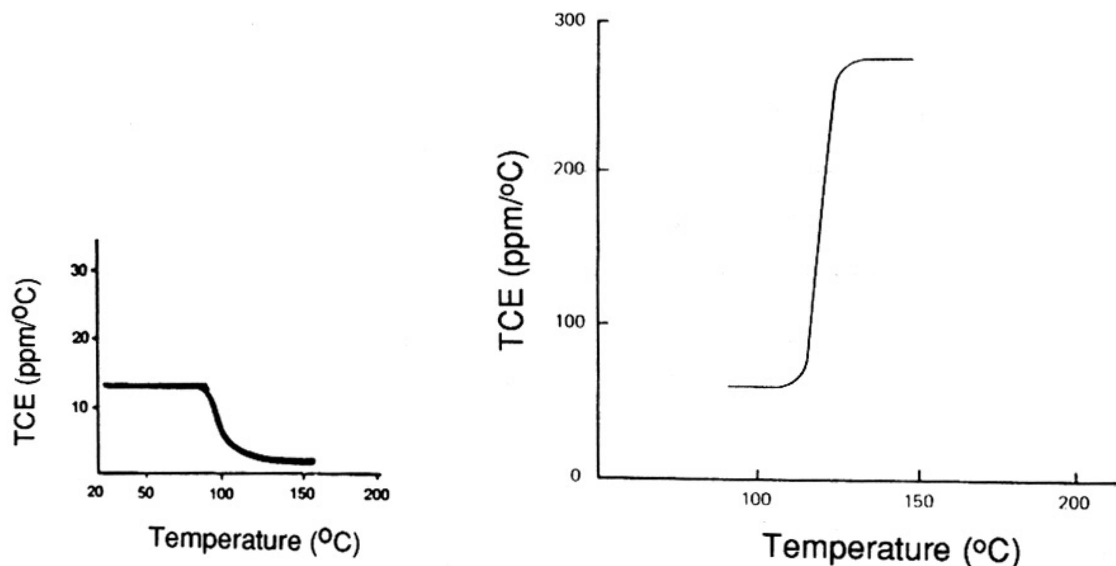


Fig. 5.13: TCE for FR-4 below and above T_g in a): the x or y direction, b): the z-direction [5.2].

The large expansion in the z-direction may cause fracture of the copper plating in the via holes during the soldering process and during high temperature use, as copper has a TCE that is only 17 ppm/°C. Alternatively there may be latent damage in the plastic with warpage, bowing and dimensional changes. This is most harmful when the board has large SMD components with rigid demands on planarity (Chapter 9).

These problems are more pronounced at lower T_g and have excluded paper/phenol laminates for other than cheap consumer electronics. Improved types of epoxy have been developed with higher T_g and better dimensional stability. Among them are "multifunctional epoxy", "tetrafunctional epoxy", and the combination bismaldeimide triazin (BT)/epoxy [5.7, 5.3]. Table 5.2 shows some important properties for these materials and other high performance materials that are discussed in the next paragraph. The TCE for some materials was shown in Figure 3.7 b).

Table 5.2: Material parameters for polymers for printed wiring boards [5.7, 5.3]

Material	ε_r	Tan δ (at 1 MHz)	α ($T < T_g$) [ppm/ ^oC]	T_g [^oC]
Paper/phenolic	4.7	0.025		95
Bisphenol epoxy (FR-4)	4.3 - 5	0.02	33 -60	130
Multifunctional epoxy	4.3 -4.5	0.02	140	145 - 180
Tetrafunctional epoxy	4.3 -4.6	0.02	55	> 150
BT/epoxy	3.5 - 4.2	0.012	100	185 - 225
Cyanate ester	2.8 - 3.6	.002 - .005	50 -100	250 -290
Polyimide (Pi)	3.0 - 4.6	.002 - .01	35 - 80	230 - 315
PTFE (Teflon)	2.1	.001	70 - 120	250 *)

*) Melts, no regular glass-transition

5.11 WIRING BOARDS FOR HIGH FREQUENCIES

5.11.1 Demands on high frequency circuit boards

The developments in monolithic IC technology give possibilities of circuits that operate at steadily higher frequencies. The clock frequencies for microprocessors, signal processors and custom designed circuits increase to 50, 100 MHz and even higher frequencies. The bandwidth in electronics must be significantly higher, to maintain short rise- and fall times. For radio- and microwave circuits, the frequency is up to 10 GHz and above.

This poses new demands on the substrate. It often needs to have:
- Controlled characteristic impedance
- Multilayer structure
- Low relative dielectric constant
- Low dielectric losses

In addition, we have other requirements, applying also to boards for low frequency circuits:
- High thermal conductivity
- Thermal compatibility to ceramic components
- Fine line dimensions
- Simple processing
- Low price

The demands mentioned in Section 5.2 are equally important.

Which factors are most important depends on the application but today's standard material, glass/epoxy (FR-4), and today's standard processes and structures do not suffice [5.9]. In this section, we will discuss some of the important properties, and some types of high performance wiring boards that are commercially available.

5.11.2 Important properties and parameters, new materials

For high frequency use, we need to have a controlled characteristic impedance, Z_0, as mentioned above (see Section 6.7 and [5.24]). This implies that there must be a ground/voltage plane between every signal layer. Conductor widths and thicknesses in the dielectric must be controlled to small tolerances. ε_r must be close to a constant, independent of temperature, moisture content, and frequency.

The dielectric attenuation needs to be low. It is given by (see Section 6.7):

$$\alpha_d = \pi\, \varepsilon_0^{1/2} \varepsilon_r^{\;1/2} \tan\delta\, f/c.$$

Here ε_0 is the dielectric constant, ε_r = the relative dielectric constant, tan δ = dielectric loss tangent (please refer to Sections 3.2.3 and 4.3.1), f = frequency, and c is the speed of light.

For the high frequency wiring boards it is therefore important that ε_r of the dielectric is low, as well as the loss tangent, particularly for big wiring boards with long signal paths. Low ε_r also gives the high signal speed, low parasitic capacitance, and less crosstalk. It gives the possibility to use thinner dielectric and achieve higher conductor density [5.8], please refer to Section 6.7.

FR-4 has not got good properties at high frequency, please refer to Table 5.2. The loss tangent is high, furthermore ε_r varies with frequency, please refer to Figure 5.14 so Z_0 becomes frequency dependent [5.9].

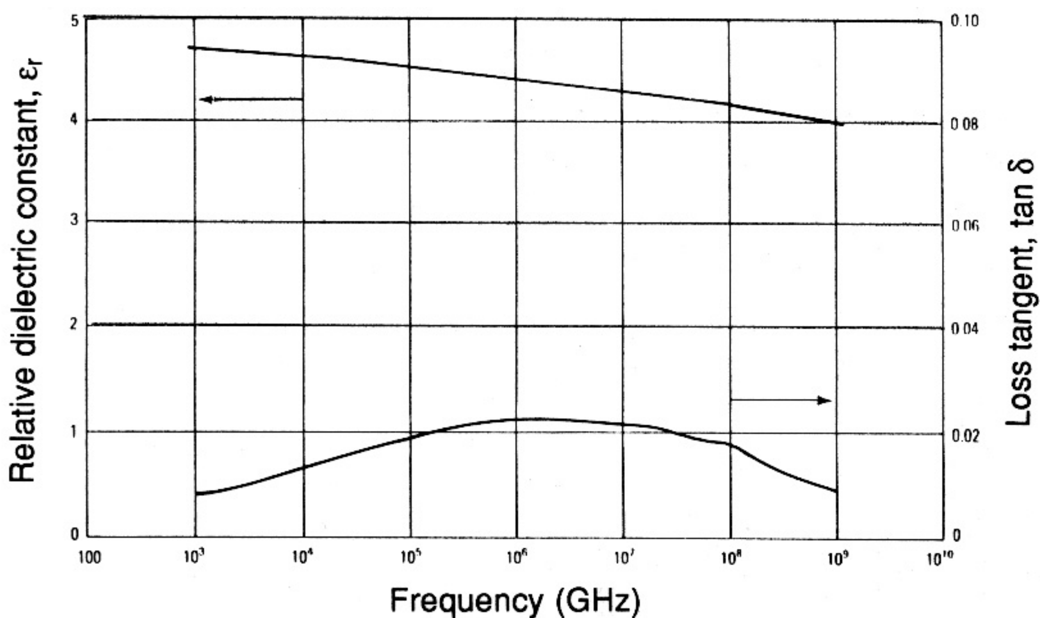


Fig. 5.14: Frequency dependence of ε_r and tan δ for FR-4 [5.9]. Relative dielectric constant, ε_r Loss tangent, tan δ

The "ideal dielectric" is air, with $\varepsilon_r = 1$ and tan $\delta = 0$. Of the practically useful material PTFE (Polytetrafluorethylene, Teflon) is the closest, see Table 5.2. It can also withstand high temperatures but the material is soft, and it bends easily. It is so chemically inert that it is difficult to process, and Cu conductor foil has poor adhesion to it. With certain additives PTFE has for many years been in use as a microwave "soft substrate", under names such as Duroid from Rogers Corp. Normally there is a ground plane on one side of the soft substrate, and one conductor layer with "microstrip" geometry (please refer to Section 6.7) on the other side. Several types of multilayer circuit boards from several manufacturers are based on PTFE as dielectric, see below.

Various types of polyimide also have low dielectric constant, low loss and high glass transition temperature. Polyimide has been combined with aramid (Kevlar) or quartz fibres instead of glass fibre, to obtain lower loss and lower ε_r but there are problems in machining Kevlar and quartz, making such laminates costly. Polyimide can also be used on substrates of metal, ceramic or silicon without fibre reinforcement. An important handicap of most polyimides is that the materials are hygroscopic and absorb several percent moisture. That may create problems during soldering as well as during operation of the complete product: ε_r will change with the moisture content, and corrosion will increase.

A new class of materials with the potential to be the next generation of standard dielectrics, are cyanate esters [5.3, 5.10, 5.11]. These materials have high T_g, low thermal coefficient of expansion, relative low ε_r and low loss, good adhesion to Cu, and good chemical stability.

5.11.3 Commercial products

Many companies are in the process of introducing new and improved types of laminates/materials on the market. We shall only mention a few examples. Rogers Corp. offers a fluoropolymer composite, structured as shown in Figure 5.15 a). The printed wiring board with RO2800 gives good high frequency properties, Table 5.3. However, it requires non-standard PWB processing [5.8, 5.13]. The surface needs to be treated with the poisonous sodiumnaphtalene to improve the adhesion to Cu, and lamination takes place at 350 °C, (as opposed to 175 °C for glass/epoxy multilayer boards, Section 5.7). Rogers also has one type suitable for flexible boards or cables, RO2500, with similar properties.

Gore Corp. (which also markets Goretex-materials for raincoats, etc.), has developed prepreg materials based on Teflon with air pores. Some properties are shown in Table 5.3. The material may be laminated together with FR-4, as shown in Figure 5.15 b), and gives a combination of conventional processing, yet low effective dielectric constant and low losses in the dielectric between signal conductors and the corresponding ground plane [5.14].

Fortin Industries offer laminates based on cyanate ester, with low ε_r and high T_g, Table 5.3. The processing is similar to that of FR-4.

Table 5.3: Materials parameters for important materials combinations and some commercial products for high performance printed wiring boards.

Material	ε_r	tan δ at 1 MHz)	K [W/m °C]	α (T<T_g) x-y (and z) [ppm/°C]	T_g [°C]
FR-4	4.6	.02	0.2	12-16	125
				(60)	
PTFE/glass	2.35	.001	0.26	24	250
				(260)	
Pi/glass	4.4 -4.8	.01 -.015	0.35	11-14	220 - 270
				(60)	
Pi/quartz	3.4 - 4	.005	0.13	6-8	270
				(34)	
RO2800	2.8	.0014	0.44	16-19	327*)
				(24)	
RO2500#)	2.5	.0025			
Fortin/CE	2.8-3.6	.003-.009	0.3	ca. 15	110 - 250
				(50-350)	
Gore	2.4 -2.6	.01	ca. 0.2	12	120 -180
				(50)	
Alumina	10	.0001	30	5-7	-

*) Melting point
#) Used for flexible boards and high frequency flat cables.

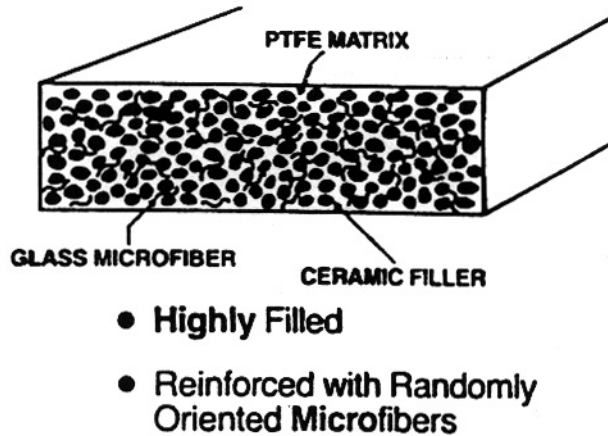


Fig. 5.15 a): Structure of Rogers material RO2800.

Measured attenuation for some new types of high frequency PWB materials are shown in Figure 5.16.

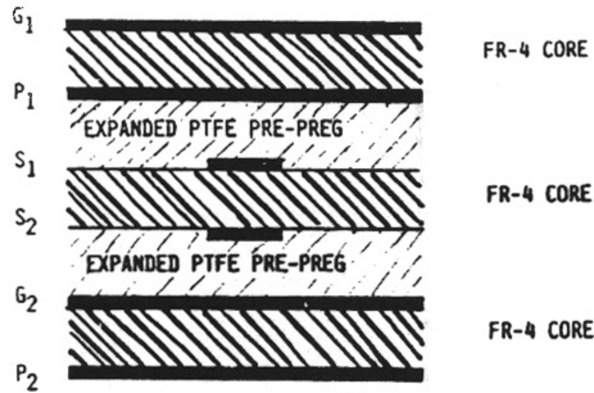


Fig. 5.15 b): Combination of Gore-Ply and FR-4 gives a simple process, and at the same time low dielectric losses and reduced capacitance to ground.

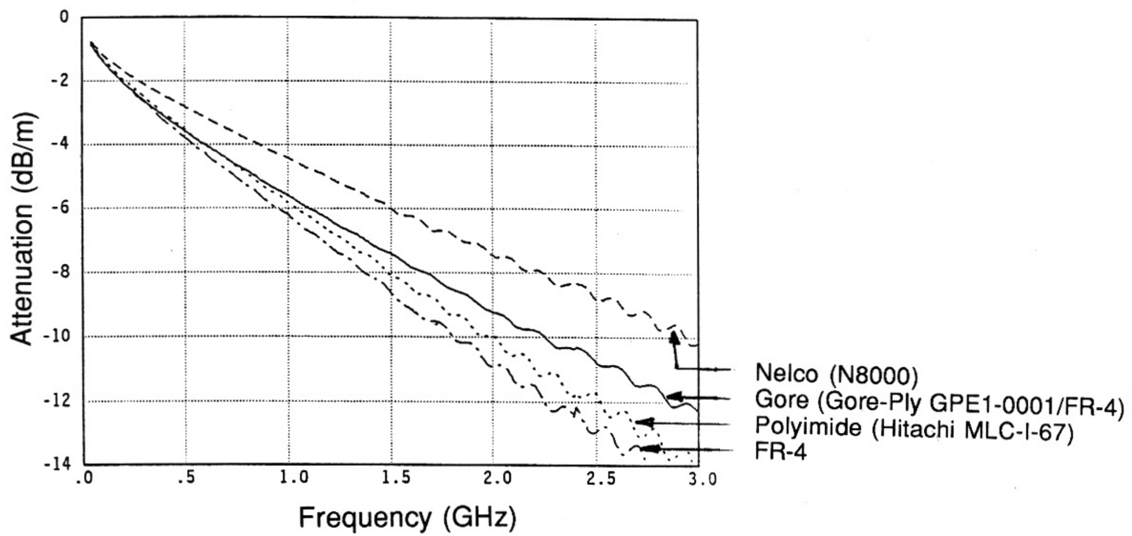


Fig. 5.16: Attenuation in (dB) as function of frequency for a one meter long stripline, for the high performance materials Gore, Nelco and polyimide, compared to FR-4 [5.24].

More complex processes have been tested by Martin Marietta [5.14], Ericsson [5.15] and other companies.

A special process that gives extremely high performance is "Multiwire" and "Microwire" from the US company PCK, see Figure 5.17 [5.16]. A Cu/Invar/Cu core forms the ground plane. The dielectric and a layer of adhesive are laminated on top. Then insulated conductors are placed in the layer of adhesive one by one, with a computer controlled tool, see Figure 5.18. First one conductor layer is placed primarily in the x-direction, then one layer that is primarily along the y-direction. Thereafter a dielectric layer is again deposited, and if necessary, the structure is repeated by a new ground plane and new layers of conductors. On the surface, Cu is plated for solder lands. Contacts between the conductor layers and between conductor and solder lands are obtained by "burning" via holes by laser. The laser evaporates the dielectric and the insulation on the conductors. Subsequently Cu is plated in the via holes to obtain contact. Controlled characteristic impedance and very high conductor density characterise "Microwire", but there are few producers, and the technology is expensive.

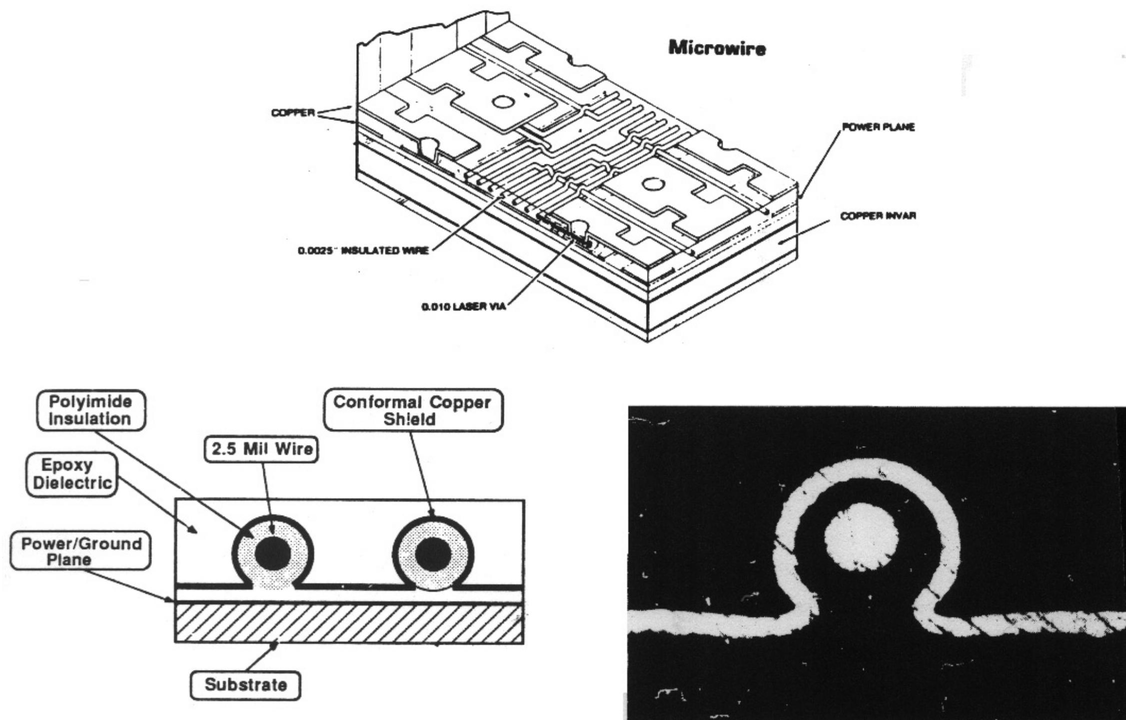


Fig. 5.17: Top: Microwire from PCK, with conductors insulated with organic insulation, and a metal foil as ground plane. Bottom: Next generation technology, where each conductor has its own metal shield [5.16].

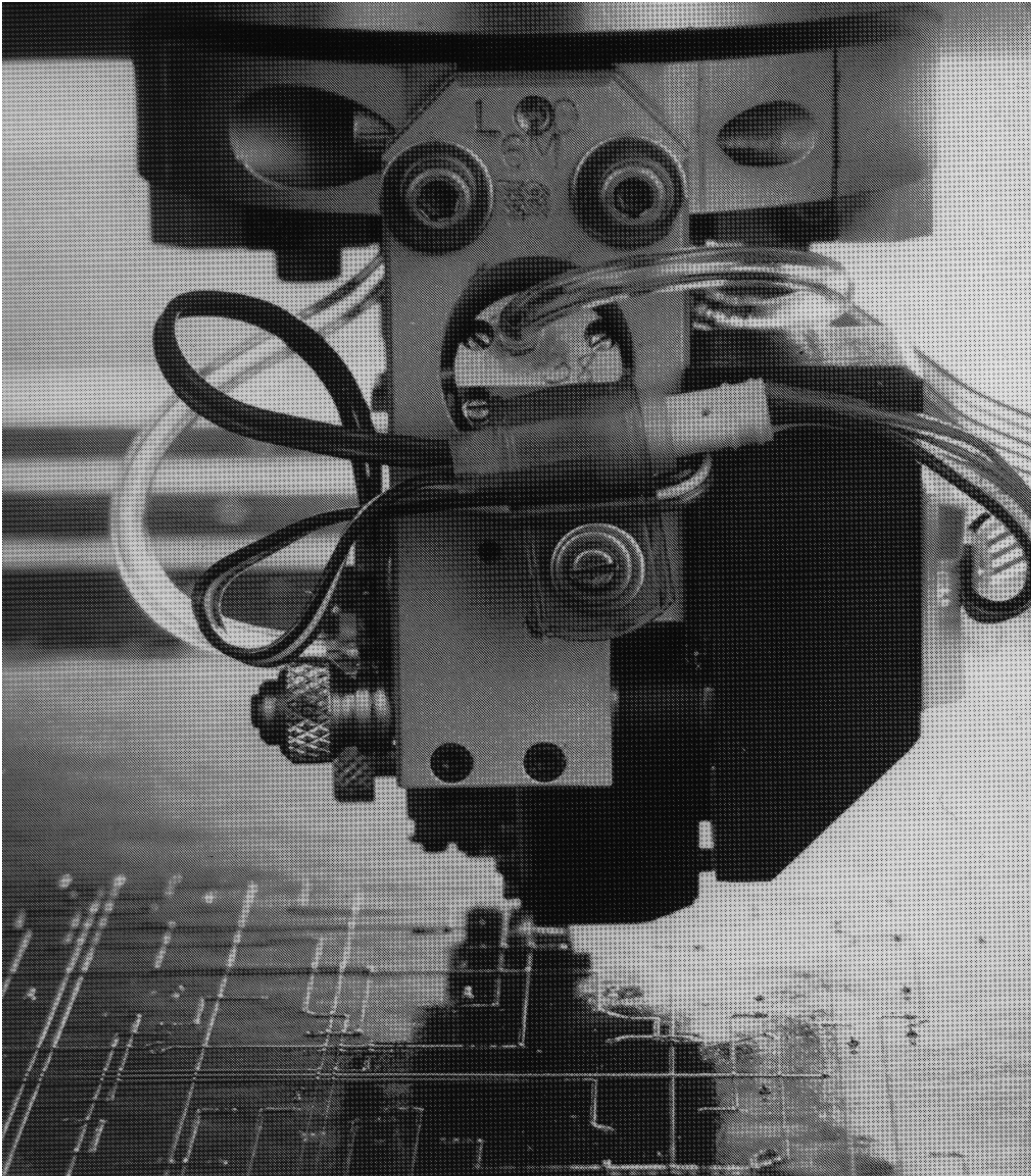
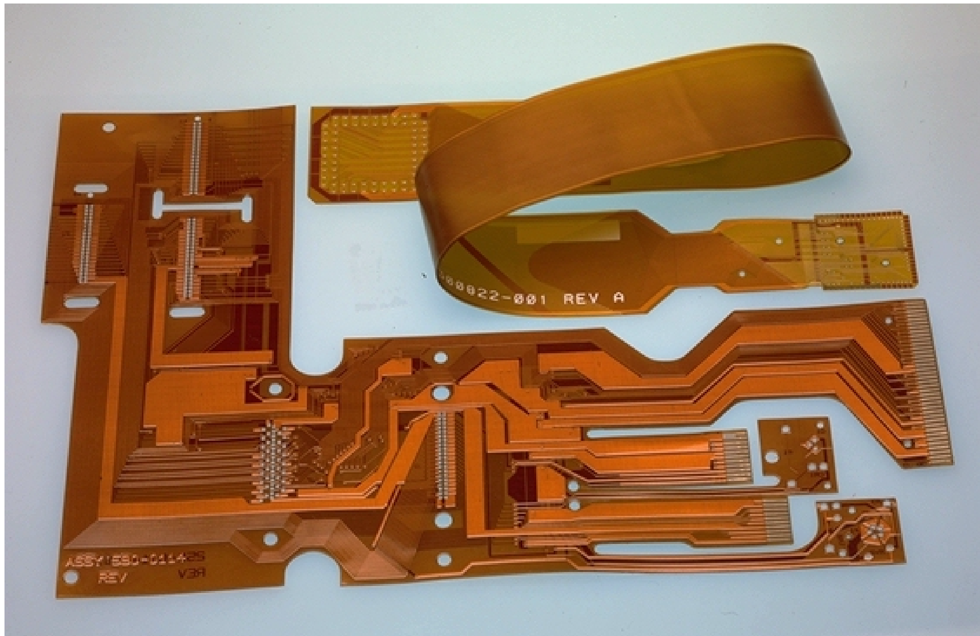


Fig. 5.18: The equipment head that deposits the conductors on the laminate for Microwire.

5.12 FLEXIBLE PRINTED WIRING BOARDS

Flexible wiring boards are used in products that are moveable during use (dynamic): Disk drives for computers, printers, etc., or static, where the board is bent in the right shape and remains in this position during operation. Examples of this are cameras, see Figure 5.19 and other compact products with circuitry

packed into odd-shaped volumes. A special type of flexible boards is the membrane switch panel. Even if membrane switch panels are not carrying components in the normal sense, we shall describe them here.



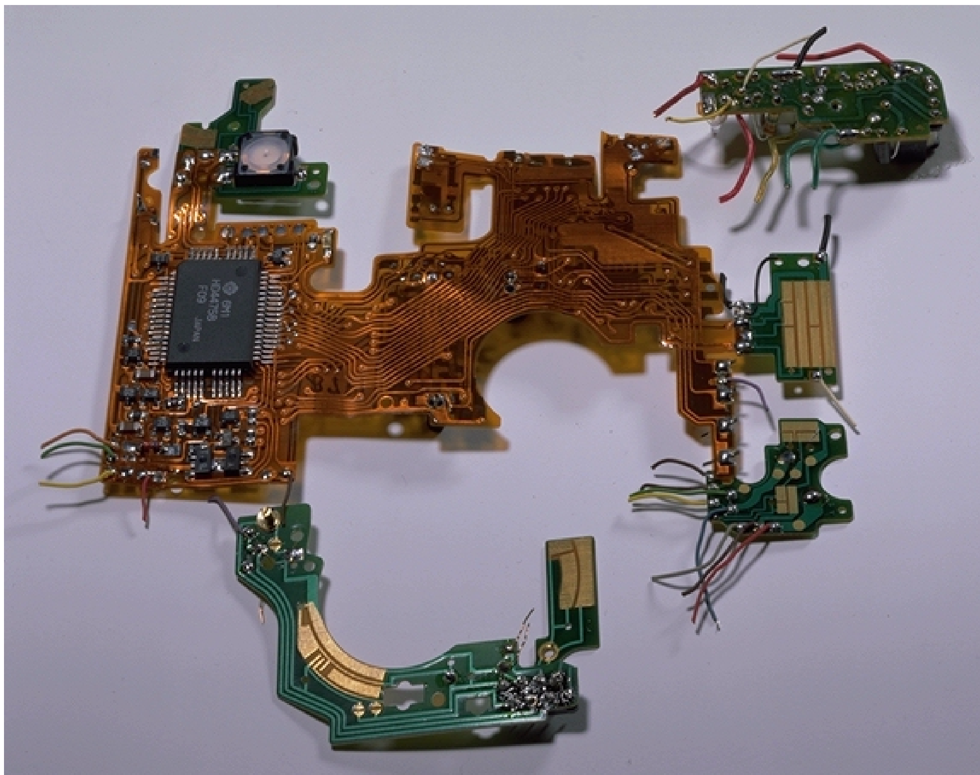


Fig. 5.19: Flexible printed wiring boards. Bottom: Most of the electronics in Minoltas camera Maxxum 9000 is on two flexible printed circuit boards.

Flexible PWBs are made primarily from polyester and polyimide (specially known under DuPont´s trademark Kapton). Thin glass/epoxy is also used to some extent, and PTFE for microwave frequencies. Some characteristic properties are given in Table 5.4. For regular circuits, polyimide is used the most. (Similar polyimide foil is also normally used as the base material of the film for tape automated bonding (TAB), see Chapter 3.) Polyester is particularly used for membrane switch panels.

Table 5.4: Properties for materials used for flexible printed wiring boards. (Data: Schoeller Elektronik).

Typical values	Unit	Glass Epoxy	Polyester base laminate	Polyimide base laminate
Solderability	°C/s	260/10	230/1	260/10
Max. continuous operating temperature	°C	150	110	220
Tensile strength	kp cm^{-2}	1750	1500	1700
Peel strength to copper	kp	4,5	1,8	1,3
Moisture absorption	%	0,5	0,8	2,5
Coefficient of linear expansion	$°C^{-1}$	1,1 10^{-5}	1,5 10^{-5}	2,0 10^{-5}
Etch shrinkage: Machine direction /transverse direction	%	0,2 - 0,8	1,0 - 0,55	0,45 - 0,25
Dielectric constant (60 Hz)		3,4	3,25	3,5
Dissipation factor (1 kHz)		0,037	0,006	0,003
Resistivity	ohm cm	1,6 10^{13}	10^{17}	4 10^{16}
Cost ratio (laminate only)		1,4/2	1	2/3
Comments		Not suitable for continuous folding use. Max. peel strength to copper and minimum elongation.	Sensitive to solder heat. Lowest cost. Good physical and electrical properties	Non-flammable. Outstanding physical and electrical properties.

The dimensional stability of these materials is not so good as for example in FR-4. This must be considered during the design. High absorption of moisture in polyimide is also of importance.

5.12.1 Regular flexible boards

The thickness of the polyimide layer may be 0.05 - 0.2 mm, and the substrates may have single sided or double sided conductor pattern, possibly with through hole plated via holes. This gives the structures shown in Figure 5.20. Multilayer structures are also made. The combination of flexible parts and rigid parts, "flexi-rigid" is common. The rigid parts may be passive stiffeners without conductor pattern, or they may be laminated together with a flexible part, through hole plated, with components mounted, and become the part of a complex multilayer flexi-rigid structure.

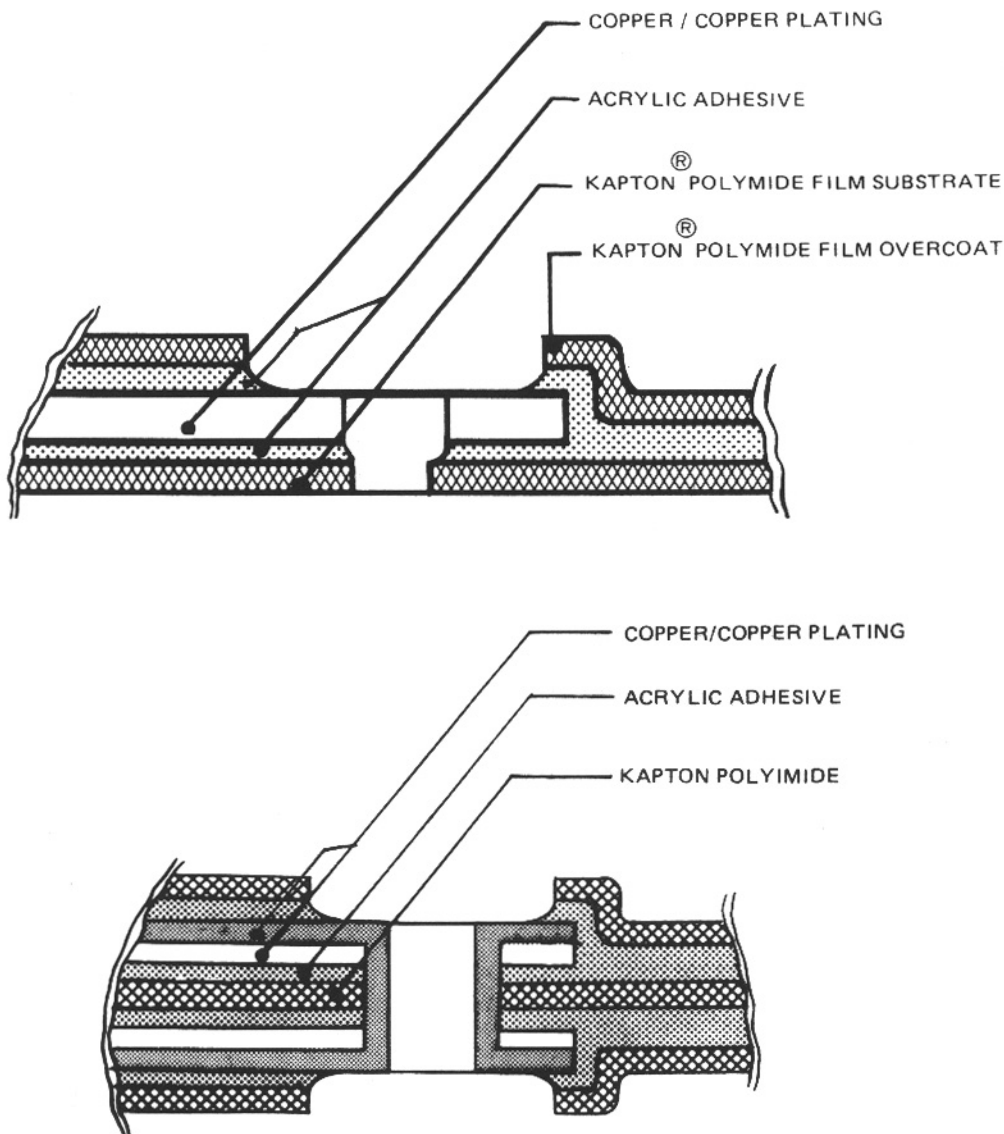


Fig. 5.20: Cross section of flexible PWB: Top: Single layer conductor foil, bottom: Double layer conductors with through hole plating.

The processing of flexible boards is similar to that of rigid boards [5.3, 5.17, and 5.18]. To get the copper foil to adhere, in case of a polyimide based board, an adhesive layer of epoxy or acrylic is used between the polyimide and the copper

foil. A cover layer serving as solder resist is normally laminated on top with a layer of adhesive underneath. Printing, photo processing, plating and etching takes place from roll to roll. That is, the process takes place while the film moves through the machines and the process baths. Holes are punched, and edge contours are punched or cut with a computer controlled knife.

5.12.2 Membrane switch panels

Membrane switch panels are used as replacement for ordinary low current switches or keyboards [5.20]. In addition, they may be shaped as informative and decorative fronts for instruments, consumer products, etc. The structure is shown schematically in Figure 5.21. All the switching elements are defined on plastic foil (normally polyester) by screen printing of the conductor patterns. The two contact points in each switching element are kept apart by a spacer layer. When the contact is pressed, the two parts touch and give a short circuit.

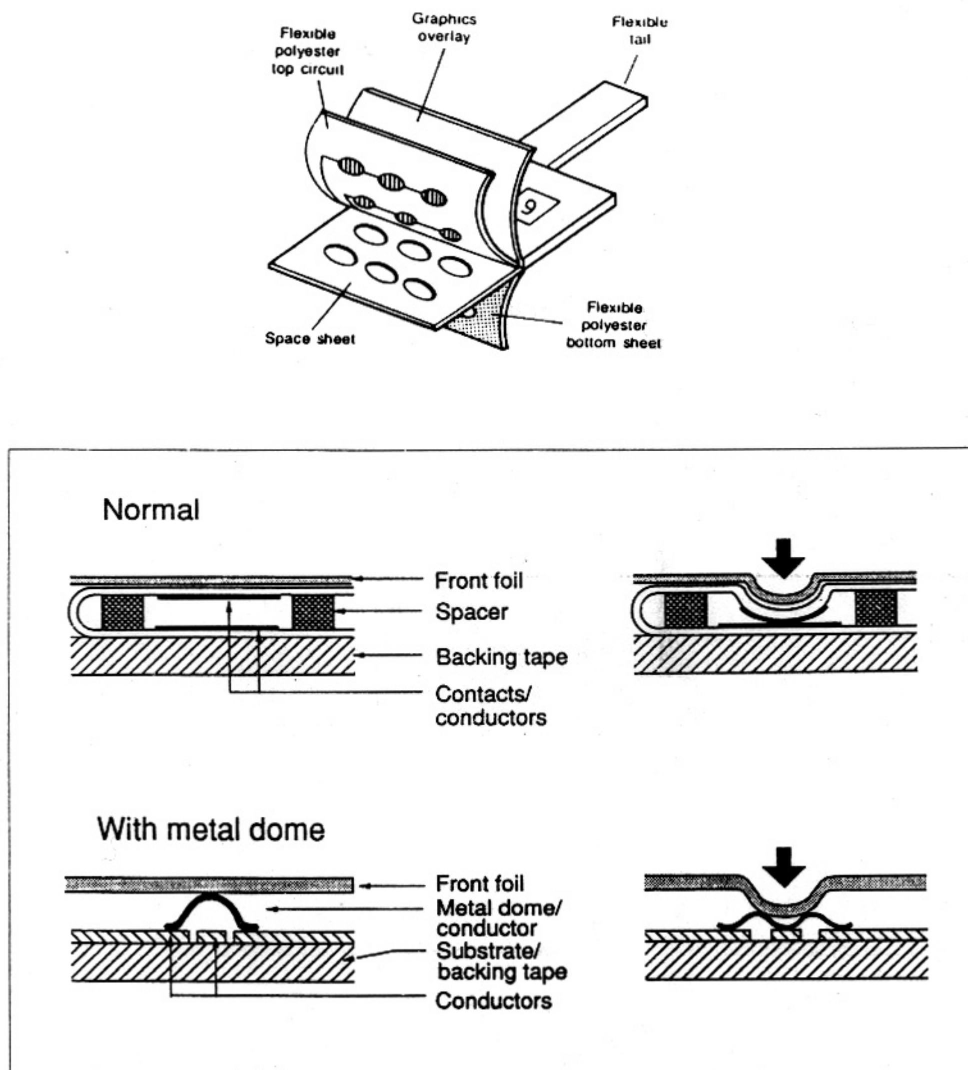


Fig. 5.21 a): Membrane switch panel, schematically. Top: Structure, bottom: Cross section of a normal panel and a panel with metal dome [5.20].

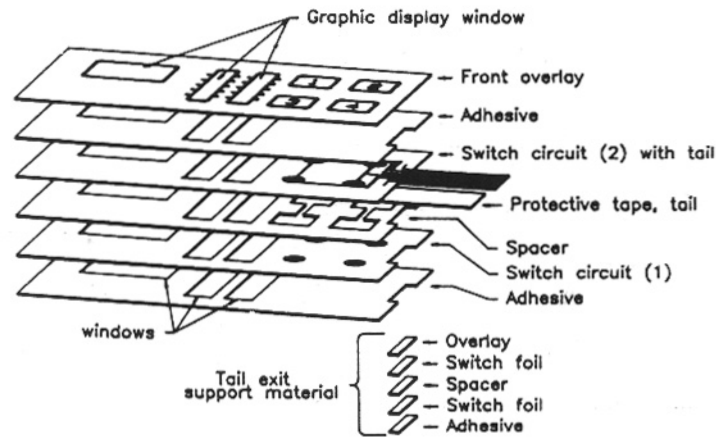


Fig. 5.21 b): Exploded view of simple switch panel [5.20].

The complete panel is composed of 5 - 10 laminated foil layers, Figure 5.21 b), see also Section 6.9 and Figure 6.39.

To obtain a direct "finger feeling" of a closed contact one may use a metal membrane ("dome") as a part of each contact point, see Figure 5.21 a). One may also have transparent areas, with light and information behind, see Figure 6.40.

The production of membrane switch panels is based on screen printing of the pattern and information on the front plate, screen printing of conducting polymer pastes for conductors and switch contact areas (see details in Section 8.3 about polymer thick film technology), punching of contours and lamination of the foil layers with adhesive layers between them. Polyester is used the most for the layers containing the conductor pattern. However, this material can not withstand normal soldering temperatures.

5.13 MOULDED BOARDS IN THREE DIMENSIONS

Printed wiring boards are generally planar and laminated from thin layers of epoxy or other polymers with reinforcement and with Cu foil for conductor layers, as described previously. Mechanical, structural parts holding batteries, electrical components of odd shapes, etc., are made as separate parts that are screwed or glued together. Around the printed circuit board, there is normally a chassis or box of some kind.

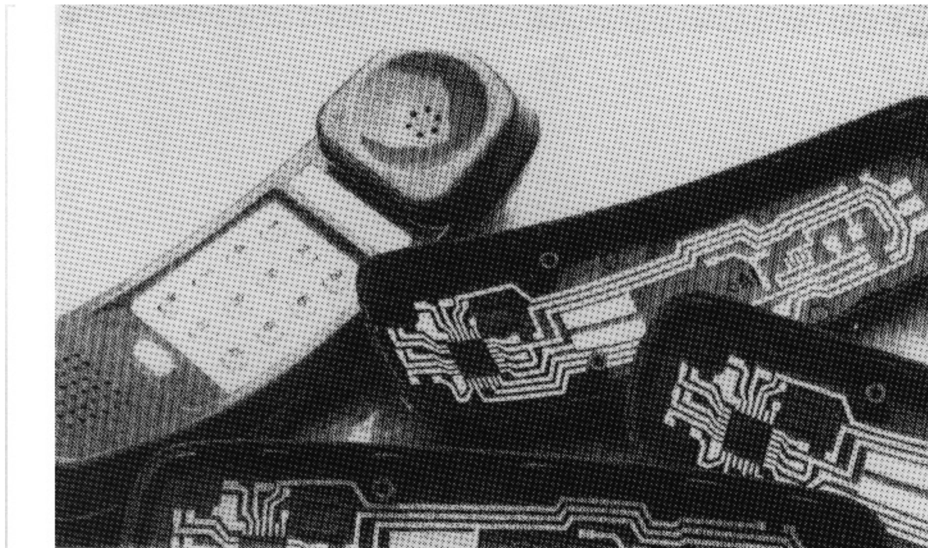
Using suitable materials and technology, it is often possible to combine the wiring board and structural parts in one moulded part, please refer to Figure 5.22 [5.25]. Such substrates may be 3-dimensional, having integrated conductors, and the components mounted directly on them by soldering, gluing or wire bonding. The moulded carrier may also have integrated connectors, knobs, pressure contacts and structures that make automatic component mounting and subsequent assembly particularly simple. The technology for 3-D moulded

boards may simplify the structure and the production of simple electronic circuits substantially.

The plastic materials that are used for this type of substrates are called engineering plastics and they are high quality thermoplastic polymers (i.e. they may be heated repeatedly to over the glass transition temperature (please refer to Section 3.3). This makes it possible to recycle the waste material after the moulding process and avoid material loss that we get by ordinary PWB production. The materials used are polysulphone, polyethersulphone, polyetherimide, and others [5.20], see Tables 3.5 and 5.5. These polymers have high glass transition temperature, high mechanical strength and dimensional stability, they are chemically resistant, and absorb little moisture. However, they have low thermal conductivity and high thermal coefficient of expansion, like other polymers. To improve the thermal conductivity and reduce the thermal expansion it is possible to mix in ceramic particles such as Al_2O_3, AlN, SiC, or use a metal core [5.3].

Table 5.5: Materials used for moulded circuit boards, and their properties, compared to epoxy and polyimide [5.3, page 945].

Polymer types	Epoxy	Polyimide	Poly-sulphone	Polyether-sulphone	Polyether-imide
Manufacturer	3M Co.	E.I.Dupont	Union Carbide	ICI America	G.E.Co
Trade name	Scotchcast 5133	Pyralin	Udel	Victrex	Ultem
Thermal conductivity (W/m°C)	0,40	0,15			0,22
Glass transition temperature [°C]	110-125	260	190	230	215
UL listed temperature [°C]	130	NA	150	180	170
Coeff. of thermal expansion [10^{-7}/°C]	600	200-400	-	-	560
Dielectric const. @1 MHz	6,2	3,50	3,10	3,50	3,15
Dissipation factor @1 MHz	0,02	0,002	0,004	0,006	0,002
Dielectric strength [V/mm]	20000	45000	48000	-	33000



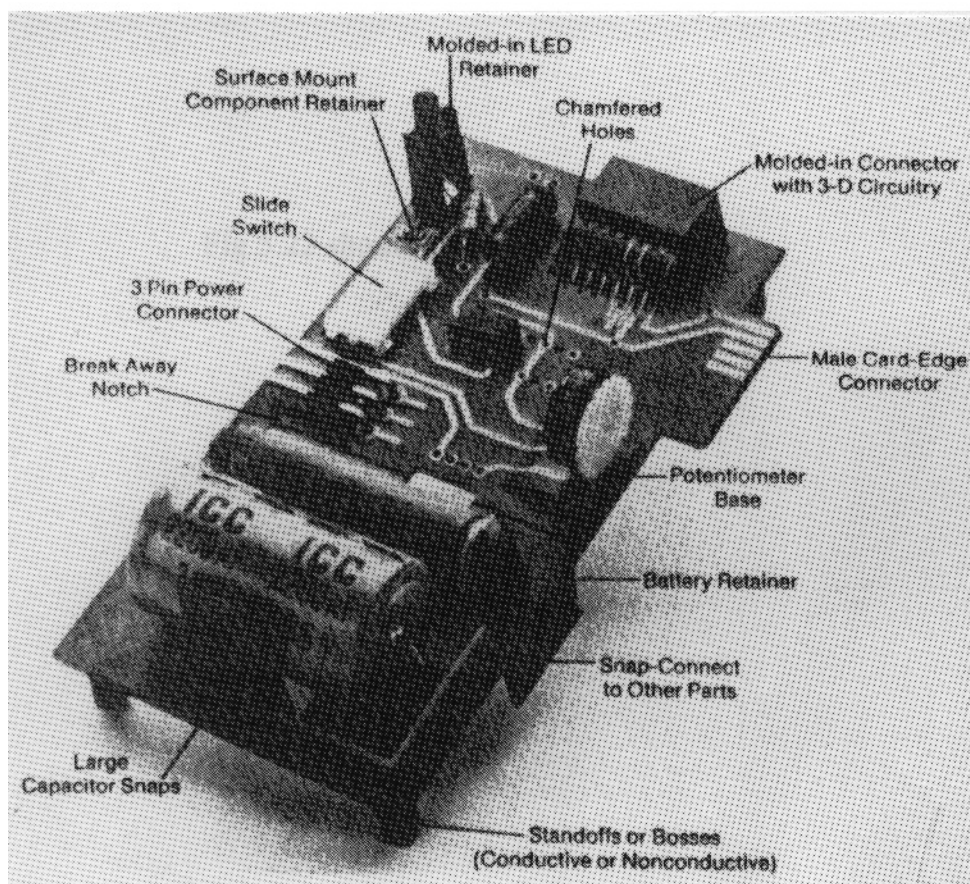


Fig. 5.22: 3 dimensional moulded component carriers, applications [5.23].

The shaping of the plastic is done by injection moulding, analogous to that used for plastic component packages. There are several ways to produce the conductor pattern, such as [5.3, 5.19, and 5.20]:

- Chemical plating (fully additive or semi-additive process), possibly after local photo-sensitising with a guided laser.
- Screen printing of polymer thick film conductors [5.20].
- Special moulding, after deposition of conductor pattern on a temporary foil, please refer to Figure 5.23.

- Two-step moulding process, one with a plastic that is"sensitised" for chemical plating, please refer to Figure 5.24.

The productions of moulding tools and start-up of the process are specific for each product, they take time, and are costly. The technology therefore has little flexibility and is not suitable for changes and modifications. It is suitable for coarse patterns, and simple products in high production volumes. It is believed that 10 - 30 % of electronics will use moulded component substrates some years from now.

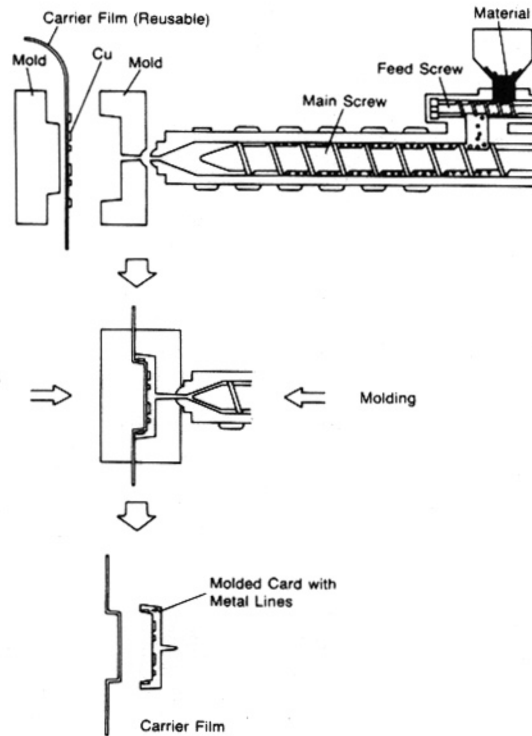


Fig. 5.23: The process for moulding of a 3-dimensional substrate with Cu conductor patterns deposited on a temporary film [5.3].

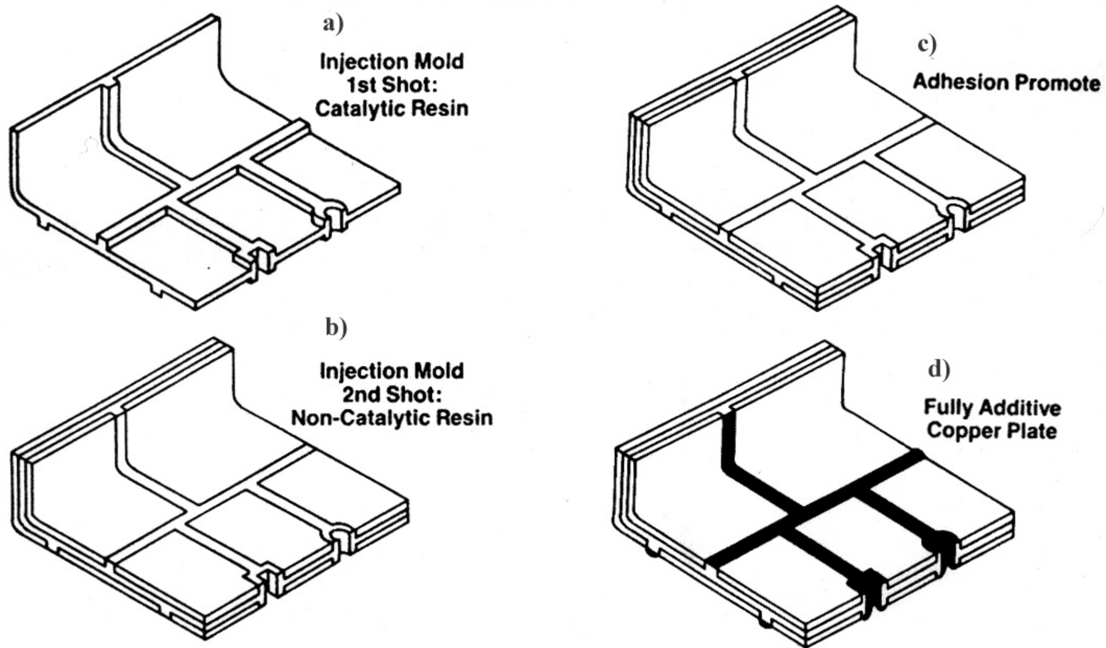


Fig. 5.24: Two steps moulding process for preparation for chemical plating of the conductor pattern on 3-D component substrates. The first moulding is done with a catalytically activated plastic, the second with "passive" plastic, where chemical plating is not sticking. (PCK, USA).

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