CHAPTER 8

HYBRID TECHNOLOGY AND MULTICHIP MODULES

8.1 INTRODUCTION

Hybrid means composite. In the context of hybrid technology, we mean a mixture of integrated components: conductors, resistors, capacitors, etc., that are manufactured as part of the substrate - and discrete components that are soldered or bonded on top of the substrate.

The traditional types of hybrid technology are thick film- and thin film hybrid technologies, that have been used since early in the 1960´s. Later polymer thick film technology (PTF) has appeared. During the last years multilayer ceramic and new forms of multilayer thin film technologies have received much attention for multichip modules (MCMs) [8.21].

The main goal of using hybrid circuits (apart from PTF), is saving space, volume and weight compared to ordinary printed circuit boards. However, we can also achieve superior high frequency properties and very high reliability. This makes hybrid circuits suitable for demanding military systems, space applications, medical electronics, as well as computers, telecommunication equipment, etc.

8.2 THICK FILM HYBRID TECHNOLOGY

8.2.1 Substrates

Important properties of thick film substrate materials are:

- Good dimensional stability during high temperature processing
- Good adhesion between substrate and printed materials
- High thermal conductivity
- A thermal coefficient of expansion matching that of other materials in the circuit
- High electrical resistivity that gives isolation between components
- Low dielectric constant
- Low dielectric loss tangent (for microwave circuits)
- Good machinability
- Low price.

No single material will satisfy all these requirements.

Various types of ceramic are used as thick film substrate materials, with 96 % Al_2O_3 (alumina) as the dominant one. Alumina has many good electrical and mechanical properties, please refer to Table 8.1. It has good dimensional stability, but because it shrinks close to 20 % during the fabrication, the dimension control is limited to typically 0.5 - 1 %.

Table 8.1 Properties of substrate materials for hybrid technology, and other important properties (In: inorganic, Semi: semiconductor, P: plastic) [8.3]

Material	Relative permit-ivity ε_r	Dielectric Loss Factor (at 10 GHz, 25°C), tan δ_ε	Specific Thermal Conduct-ivity K_{th} [W/cm °K]	Linear Thermal Expansion Coefficient (at 25°C) $\Delta l/l/\Delta T$ [10^{-6}/°K]	Temper-ature Coefficient of ε_ρ $\Delta\varepsilon/\varepsilon\Delta T$ [10^{-6}/°K]	Type	Remarks
Al_2O_3 ceramic (99.5% pure)	9,8	0,0001	0,37	6,3	+136	In	
Al_2O_3 ceramic (96% pure)	9,4	0,001	0,35	6,4		In	
Sapphire	9,4; 1,6	0,0001	0,42	6	+110 +140	In	Aniso-tropic
Quartz glass	3,78	0,0001	0,017	0,55	+13	In	
Corning glass	5,75	0,0036	0,012	4,6		In	
Beryllium oxide Ceramic (BeO) (98%)	6,3	0,006	2,1	6,1	+107	In	Dust is poison-ous
Semi-Insulating GaAs	12,9	0,002	0,46	5,7		Semi	
(High-resistive) Silicon ($\rho=10^3$ ohm cm)	11,9	0,015	1,45	4,2		Semi	
PTFE	2,1	0,0003	0,002	106	+350	P	
Polyolefin (Glass reinforced)	2,32	0,0007	0,005	108	+480	P	
PTFE	2,55	0,001	0,003	16-100		P	
Aluminium			2,2	23,8			For
Copper			3,93	17			comp-
Invar				1,5			arison

It is brittle, and this limits the maximum size to 10 - 15 cm. After the material has been sintered, it is not easy to shape it. However, it can easily be cut by breaking after a partial cut is made by a high power laser. For small circuits, it is common to print and mount components on many substrates that are produced together and then broken apart in the end, to make a rational production process. Holes through the substrate may also be made by laser, but it is simpler to form the substrate contour and punch holes while the ceramic is pliable, before the sintering. Please refer to Sections 3.2.3 and 8.5 below.

The thermal conductivity of 20 - 30 W/ ^oC is approximately 100 times better than for organic substrate materials, and the low thermal coefficient of expansion, 6 ppm/^oC, is advantageous for the mounting of ceramic components and semiconductor chips.

For circuits with very high power dissipation AlN substrates are used today, with 5 times or higher thermal conductivity than Al_2O_3. Many properties are similar to those of Al_2O_3. The thermal coefficient of expansion is somewhat lower, 4.5

ppm/°C. This, and different surface properties, give a need for special printing pastes on AlN, to avoid flaking off during the high temperature processing. BeO has even higher thermal conductivity than AlN. However, its use is limited by the fact that dust and vapour from BeO are very poisonous. High price is also connected to this fact.

For high volume products with lower electrical demands, enamel coated metal is used as substrate, to some extent. Big circuits can be made, and we achieve electrical grounding in the substrate. For details see [8.1].

8.2.2 Materials for conductors, resistors, dielectrics

Conductors, resistors and dielectric materials are applied in paste form by screen printing and they are transformed/sintered by heating to high temperature, "firing". The pastes have three main ingredients:

- Functional element (metal-, alloy- or oxide particles)
- Matrix or "binder" (glass particles)
- Organic solvents and "temporary binder".

The organic, temporary binders are polymers that give control over the printing properties. They decompose and evaporate early in the firing process, together with the solvents. The glass particles melt in the firing process, adhere to the substrate, bind the active particles together and give stability for the circuit. The high firing temperature, typically 800 - 900 °C, see Figure 8.1, is important for the long term stability and reliability.

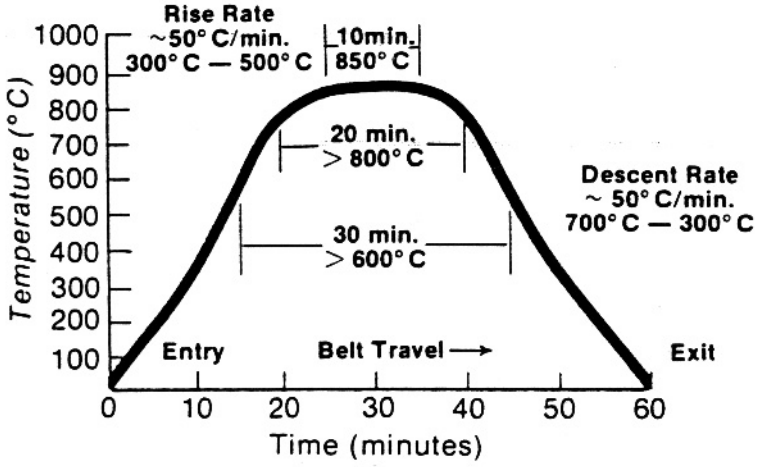


Fig. 8.1 Typical temperature profile for thick film firing [8.1]

Conductors

The conducting pastes should give:

- High electrical conductivity
- Strong adhesion to the substrate
- Excellent solderability for soldering of packaged components
- Reliable bondability for wire bonding of naked IC chips.

Price is also an important parameter.

Normally one conductor paste can not satisfy all these criteria, and it is necessary to make several conductor prints.

The most used conductor systems are gold, copper, alloys of palladium/silver, palladium/gold and platinum/gold, with properties shown in Table 8.2. Noble metal systems are used because the heat treatment takes place at above 800 °C, where other metals are ruined by oxidation. However, gold and platinum are expensive materials, so the material cost is an important factor in the final price of the circuit. Gold is very well suited as basis for bonding, but it is not suitable for soldering. This is because gold is very quickly dissolved in solder metal during the soldering process, and it gives a brittle intermetallic composition with poor reliability properties. Pure silver has a strong tendency for migration [8.1], which may cause reliability problems after some time. However, silver/palladium gives little migration, it is excellent for soldering, and is well suited for making contact areas for printed thick film resistors. Therefore, this alloy is the most used as conductor material, although it has lower conductivity than the pure elemental conductors. Silver is also used in alloys with platinum.

Copper has high conductivity and low price. However, strong oxidation in air at high temperature makes it necessary that copper must be fired in a neutral nitrogen atmosphere. That gives a more complicated and costly process and has impeded the use of copper conductors.

Nickel is also used to some extent, but it has lower electrical conductivity than the other materials.

Typical thicknesses for the conductors are 5 - 10 μm after firing. The sheet resistivity is typically between 2 and 25 mohm/sq, please refer to Table 8.2.

Table 8.2 Properties of thick film conductor systems [8.2]

Comparison of Parameters for Thick-film Conductors			
	AgPd	*Cu*	*Au*
Sheet Resistivity (mohm/❒)	25	1,8	2,5
Breakdown Current (mA/mm width)	3000	10000	10000
Thickness	10-20	15-30	5-15
Minimum With (μm)	150	150	50
Through-hole Diameter	0,4-1,5	0,4-1,5	-
Number of conductor layers	1-3	1-5	1-5
Substrate Area (cm^2)	0,2-100	0,2-200	0,2-50
Substrate Thickness (mm)	0,6-1	0,6-1	0,25-1
Tin-Lead Soldering Properties on Thick Film Conductors			
Parameter	*AgPd*	*Cu*	*Au*
Solderability	Good	Good	Unsolderable
Wetting	Good	Good-excellent	-
Leach Resistance	Fair-good	Excellent	-
Adhesion	Excellent	Excellent	-
Visual Quality	Good	Excellent	-

Resistors

Important properties of thick film resistors are:

- Large range of available resistor values
- High stability
- Low thermal coefficient of resistivity, with little spread over the substrate
- Low voltage dependence of the resistance
- Good noise properties.

The resistor pastes consist of the same three main ingredients as the conductor pastes, but the active elements have lower electrical conductivity. They are most often based on various types of oxides of ruthenium: RuO_2, $BaRuO_3$, $Bi_2Ru_2O_7$. In addition, oxides of iridium, rhodium and osmium are used. They may be produced with sheet resistance down to approximately 1 ohm/sq, and up to 10^9 ohm/sq, for a 25 μm thick print. The sheet resistivity is determined by the active material in the paste, the amount of glass matrix mixed in, and the details in the processing. The tolerance in achieved resistance is lowest for the intermediate values of sheet resistivity.

We obtain termination of the resistors by printing a conductor underneath or on top of the ends of the resistor, see Figure 8.2.

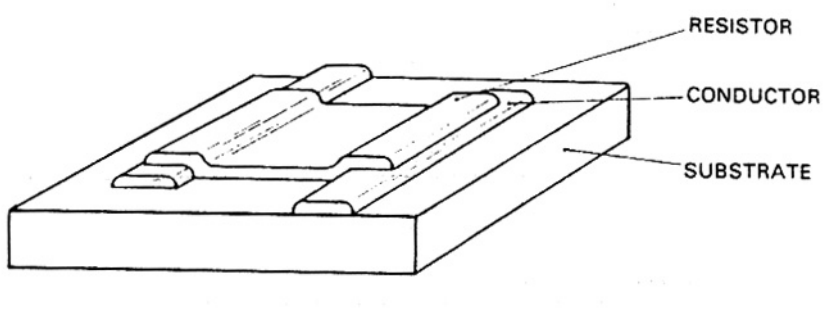


Fig. 8.2 Thick film resistor with termination.

Some typical resistor properties are shown in Table 8.3. Resistance drift lower than 0.5 % under harsh climatic conditions over long periods of time makes thick film hybrid technology attractive for demanding applications. The difference in drift between several resistors on the same substrate is typically 0.1 %. The temperature coefficient of resistance depends on the material, and it is typically in the range +/- 100 - 700 ppm/°C, with variation over a circuit, for resistors printed with the same paste, below +/- 15 ppm/°C.

The tolerance in absolute resistance after printing and firing is typically +/- 10 - 20 %, and the relative tolerance between resistors on the same substrate one order of magnitude lower. However, by laser trimming one can achieve tolerances down to approximately 0.5 % absolute, and 0.1 % relative value.

Table 8.3 Typical properties of thick film resistors [8.1]

Tolerances as fired	±10 – ±20%
Tolerances, laser trimmed	±0.5 - ± 1%
TCRs:	
5 to 100K ohm/sq (-55° to 125°C)	±100 - ±150 ppm/°C
100K to 10M ohm/sq (-55° to 125°C)	±150 - ±750 ppm/°C
Resistance drift after 1,000 hr at 150°C no load	+0.3 to -0.3%
Resistance drift after 1,000 hr at 85°C with 25 watts/in^2	0.25 to 0.3%
Resistance drift, short term overload (2.5 times rated voltage)	<0.5%
Voltage coefficient	20 ppm/(V) (in)
Noise (Quan-Tech):	
At 100 ohm/sq	-30 to -20 dB
At 100 Kohm/sq	0 to +20
Power ratings	40-50 watts/in^2

Dielectrics

Dielectric materials are printed to obtain insulation between various layers of conductors, to produce capacitors, and as passivating cover on top of the whole circuit. For insulation, low capacitance between conductors is desirable and we use materials with low dielectric constant. For capacitors, materials with high dielectric constant are used, to achieve high capacitance with little area consumption. Important properties of dielectric materials:

- High insulation resistance
- High breakdown field
- For insulators: Low dielectric constant
- For capacitors: Suitable dielectric constant, low temperature coefficient and low voltage coefficient of dielectric properties
- Low loss tangent
- Low porosity

For insulation layers, aluminium oxide is the common functional element, together with glass. The glass melts and crystallises during firing at 850 - 950 °C, but it does not melt if heated again. The relative dielectric constant is typically ε_r = 9 - 10, and breakdown field strength 20 V/μm.

The dielectrics for high value capacitors consist of ferroelectric materials with ε_r up to above 1000, similarly to ceramic multilayer capacitors, please refer to Chapter 4. However, the properties of these materials change drastically near the Curie temperature, see Section 4.3 and [8.1]. Barium titanate is used, with additives of strontium, calcium, tin or oxides of zirconium to change the Curie temperature and to reduce the temperature coefficient in the temperature range of use. That gives ε_r = 1000 - 3000 and temperature coefficient up to approximately +/- 5000 ppm/°C. For small capacitors the pastes of magnesium titanate, zinc titanate, titanium oxide, and calcium titanate are used, with ε_r = 12 - 160, and temperature coefficient +/- 200 ppm/°C.

Table 8.4 Typical properties of printed and discrete capacitors [8.2]

Capacitor	Capacitance range	Absolute Tolerance [%]	ε	Isolation Resistance [Mohm]	Tan δ [%]	TCC [ppm/°C]	Voltage Range
Thick-film I	2 pF/mm^2	5 - 20	12	>10^6	<0.25	45	50-200
Thick-film II	8 pF/mm^2	10 - 30	50	>10^4	<1.5	500	50-200
Thick-film III	50 pF/mm^2	10 - 30	500	>10^4	<2.0	2000	50-200
Thick-film IV	150 pF/mm^2	10 - 30	2000	>10^3	<4.0	-400	50-200
Ceramic-chip NPO	1 p F - 4 nF	1 - 10	10	>10^5	<0.1	±30	50-200
Ceramic-chip X7R	0.1 - 1.5 nF	3 - 20	1200	>10^5	<2.5	800	50-200
Tantalum-chip	0.1 - 100 μF	5 - 20	25	Maximum leakage current 0.5 - 3 μA	<6.0	500	4 - 50

Capacitors are not suitable for laser trimming. That, in addition to the above mentioned disadvantages, is the reason why printed capacitors are used only in small values and for uncritical purposes (decoupling capacitors, etc.). Some properties of printed and discrete capacitors are compared in Table 8.4.

Pastes for the protection layer on top of thick film circuits are composed such that they may be fired at lower temperature, approximately 500 °C, and affect the previously printed layers as little as possible.

8.2.3 Production process

The layout of the circuit is made by CAD tools, photo plotting or laser plotting, analogous to the ones used for layout of multilayer PCBs in Chapter 5. Photographic films are produced for the pattern of each layer. From these films, screens for screen printing are produced, using a photolithographic process.

When a print has been made the circuit is dried in an in-line furnace at typically 100 - 150 °C. Then the firing is done in a different furnace at 700 - 1000 °C. The process is repeated for each layer, but all resistor layers are fired in the same process step, after the conductor layers. To achieve good reproducibility for resistors the temperature profile, the top temperature and the time have to be very precisely controlled, maximum deviation in temperature is below 1 °C.

The smallest conductor width that can be achieved with ordinary printing technique is approximately 100 μm. (Using an extra photolithography and etch step this may be reduced to 50 μm.)

It is possible to make conducting contact between the top side and the bottom side of the substrate by printing through holes in the substrate. This is done by sucking the paste through the hole by use of vacuum on the bottom side of the substrate while the printing on the top side is done. To achieve reliable contact the substrate is then turned around and the paste is printed again from the other side in combination with the vacuum. It is common to have all the conductors

and discrete, surface mounted components on one side and the resistors on the other for easy laser trimming.

Figure 8.3 shows the typical process flow for a simple circuit with two conductor layers and one resistor layer. Dielectrics are normally printed twice to avoid pinholes that may cause short circuit faults through the insulating dielectric.

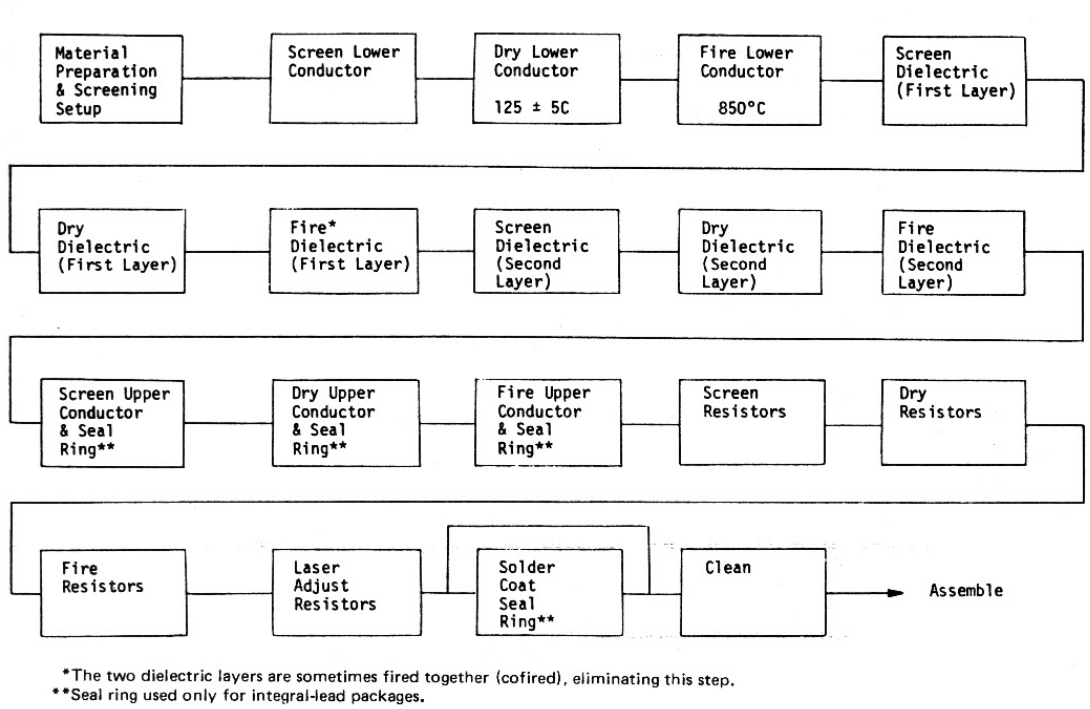


Fig. 8.3 Process flow for production of thick film circuits [8.1]

Testing is normally done on the substrates before component mounting, as well as on the completed circuits with the components mounted. Test probe-cards, as shown in Figure 8.4, are used for the contacting. During the testing the resistors are adjusted by laser trimming (previously sandblasting). It is done by a powerful pulsed YAG-laser automatically focused on one spot of the resistor, evaporating the resistor material, while the resistance value is measured. The laser focus is moved and it removes material along a track, until the resistance value is inside the desired tolerance. The resistance will always increase by the trimming; therefore the resistance after printing is made 20 - 30 % lower than the desired end value. Three normal trim geometries are shown in Figure 8.5. With an L- cut the coarse trimming is done with a track perpendicular to the resistor length, and the fine trimming to accurate value is done by the track along the direction of the current. Digital trimming gives the best stability and noise properties but occupies more substrate area.

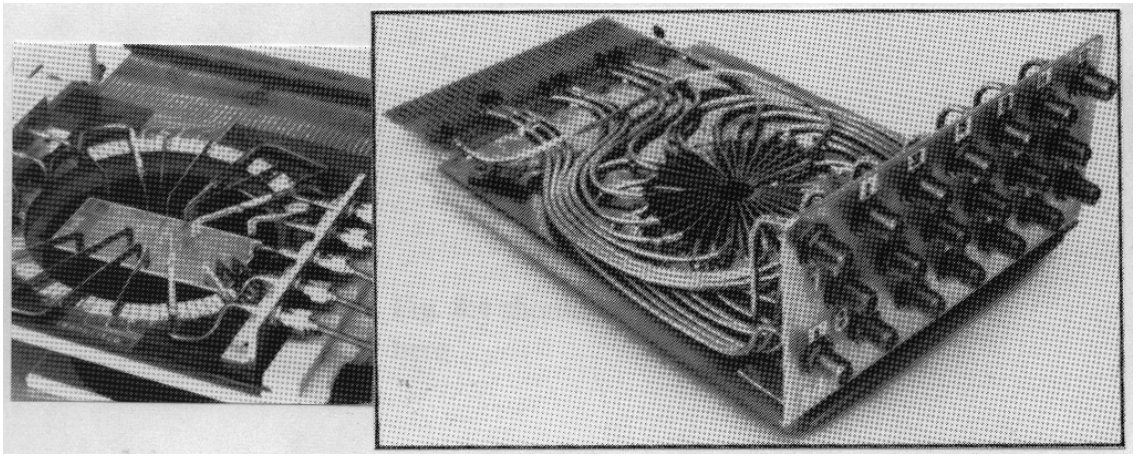


Fig. 8.4 Probe card for testing of thick- and thin film hybrid circuits. Coaxial probes are used for high frequency signals.

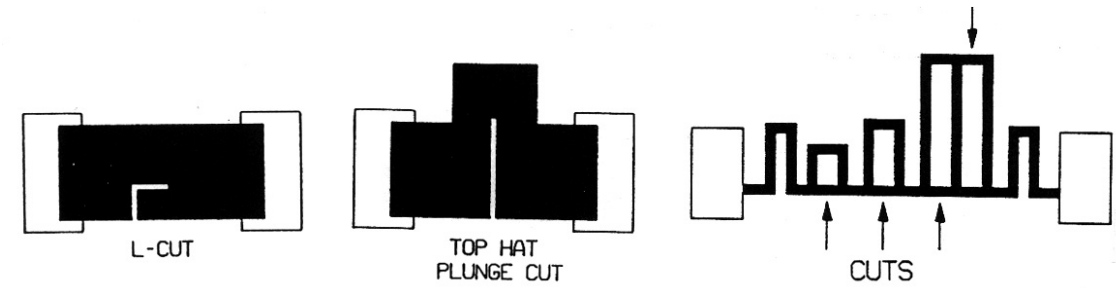


Fig. 8.5 Laser trim cut forms: a): L-cut, the most common, b): Top hat plunge cut, c): Digital trimming, which is most used for high precision thin film resistors

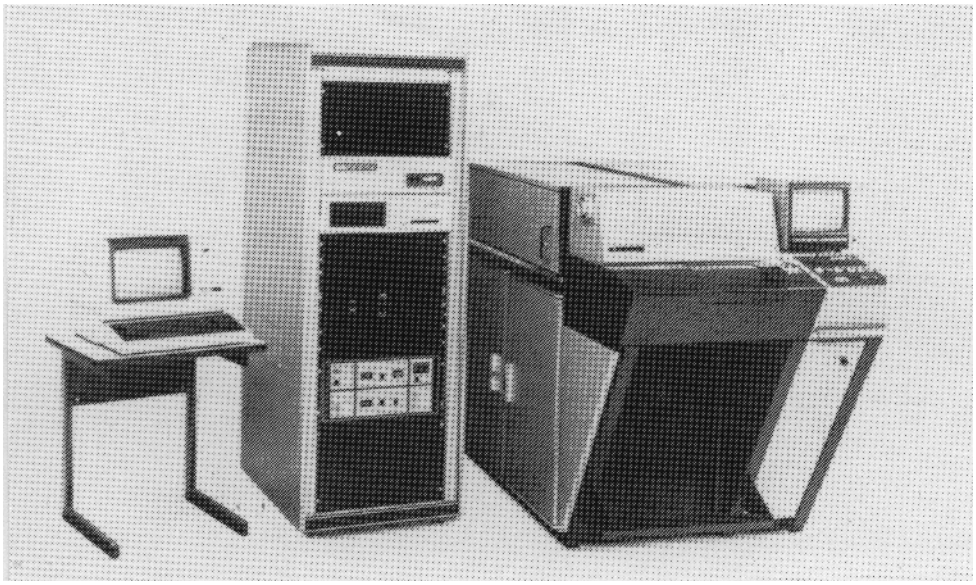


Fig. 8.6 Laser trimmer for thick film hybrid circuits, ESI Model 44

Alternatively active functional trimming may be performed. Then one measures a circuit function (the frequency of an oscillator, the amplification of an amplifier, etc.), and the value for the critical resistor is trimmed until the correct value of the measured parameter is achieved.

After completing the trimming of a resistor, the X - Y table on which the circuit is placed is automatically moved and the next resistor is trimmed. A laser trimmer is shown in Figure 8.6.

8.2.4 Component mounting, encapsulation

Soldered, encapsulated ICs, as well as wire bonded naked chips, are used on thick film hybrids. SMD passive components are soldered by using solder paste and reflow soldering, or they are glued with electrically conductive adhesive. Reflow soldering is done with a hot gas convection belt furnace, an IR. (infrared) furnace or vapour phase furnace. The process for "chip-and-wire" mounting and for soldered hybrid circuits is shown in Figure 8.7. Normally, soldered SMDs are not used on circuits together with wire bonded chip-on board, because of the danger of contamination from the solder process. This may make the surface unsuitable for wire bonding and/or give poor long term reliability. Conformal coating is an extra protection by an organic material over the components and substrate, for example Parylene. Conformal means a coating covering all surfaces. It gives mechanical and environmental protection and binds loose particles.

The hybrid circuits may be used unencapsulated or they may be mounted in metal- or ceramic flatpack packages. Circuits with naked ICs are encapsulated hermetically or the naked chips may be protected by drops of epoxy ("glob top" encapsulation).

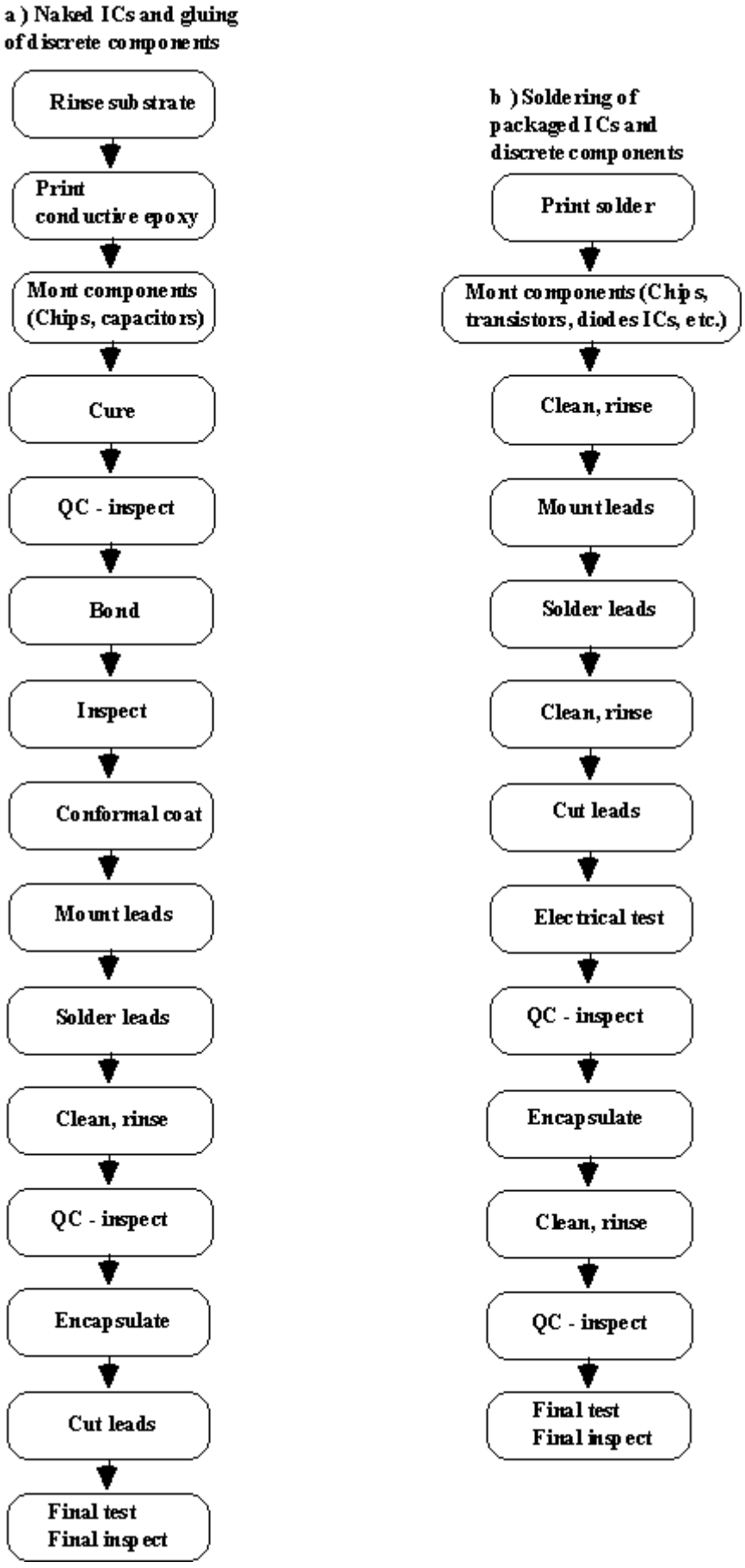


Fig. 8.7 Process flow for mounting of thick film hybrid circuits based on:
a): Naked ICs and gluing of discrete components.
b): Soldering of packaged ICs and discrete components [8.7]

8.2.5 Design rules

Some of the general design guidelines for PCBs, given in Chapter 6, also apply for hybrid circuits. The smallest conductor widths and distances are normally 0.2 mm. The resistances in conductors and in resistors are calculated like in Section 6.3.1. The demands for low voltage drop in high current circuits may cause the need for wider conductors.

The smallest length and width for resistors are 0.5 - 1 mm. The ratio between length and width should be between 0.1 and 10. For resistors that dissipates much power the resistor area should be increased such that the dissipation is maximum 100 mW/mm^2.

The same dimensions as given in Section 6.3.4 may normally be used for solder lands in reflow soldering.

An efficient ground plane is achieved by metallising the complete underside of the substrate.

Detailed design guidelines are given in [8.1 - 8.4].

8.3 POLYMER THICK FILM TECHNOLOGY AND MEMBRANE SWITCH PANELS [8.5]

8.3.1 General

In polymer thick film hybrid technology (PTF) conductors, resistors and insulating layers are made in several layers on ordinary printed wiring board laminates, flexible substrates and injection moulded plastic materials that can serve as combined printed circuits and chassis [8.5 a)].

The main purpose of PTF is to achieve lower cost than what is achievable with conventional PCB technology or with high temperature thick film hybrid technology. In certain cases, one can achieve technical properties that are difficult to obtain with conventional technology. PTF, on the other hand, has disadvantages that limit its use.

PTF is used ordinarily on substrates of paper/phenolic or glass/epoxy, when ordinary stiff printed circuits are to be made, or polyimide or polyester for flexible boards or membrane switch panels. The starting material for conductors, resistors and insulation is in paste form, and the transfer takes place by screen printing, like in high temperature thick film hybrid technology. The curing processes are also analogous to those of high temperature thick film, but they are performed at considerably lower temperatures. After the printing of a layer, it is dried to evaporate the solvents. Then it is cured by heat or irradiation.

The design of PTF-based printed circuits is similar to that of high temperature thick film design.

The most important advantages of PTF are the following:
- Low price.
- Simple processes.
- Quick production of prototypes and full production volumes.
- PTF is well suited for repair/modification of regular printed wiring boards.
- Printed resistors can be made.
- Additive technology, little waste and environmental problems.
- Substrates: Regular printed wiring board laminates.
- Specialities:
  * Membrane switch panels.
  * Low price contacts for keyboards and for contact points to elastomeric contacts for LCD displays.

Important limitations of PTF:
- PTF circuits satisfy only moderate environmental requirements.
- Only moderate complexity can be achieved.
- High sheet resistivity in the conductors (> 10 x that of Cu foil), except when plated conductors are used (please refer to Section 8.3.2, on platable Cu paste).
- Special design rules.
- Limited solderability.
- The materials have limited shelf life before they are used.
- Limited availability (i.e. few producers).

Varieties of PTF technology

The most used varieties of PTF technology on rigid substrates are the following:

1. Simple carbon technology for keyboards, contacts, sliding potentiometers, please refer to Figure 8.8.

2. Membrane switch panels, please refer to Figure 8.9.

3. PTF for a limited number of simple conductor crossings. Most of the conductors are in copper foil, but PTF makes an additional conductor layer, with insulation under each conductor, for crossing over copper foil conductors. This version of PTF is often used for repair/modifications.

4. One complete PTF conductor layer in addition to Cu foil. PTF insulation is printed all over the board, except on contact areas, Figure 8.10 a). This is an extension of type 3.

5. Multilayer boards, Figure 8.10 b) and c): Double sided PTF, normally also with Cu foil conductors on one or both sides. One can have electrical contact through holes by PTF through hole printing, to avoid copper through hole plating.

6. Printed PTF resistors, in combination with the types above, please refer to Figure 8.10 d).

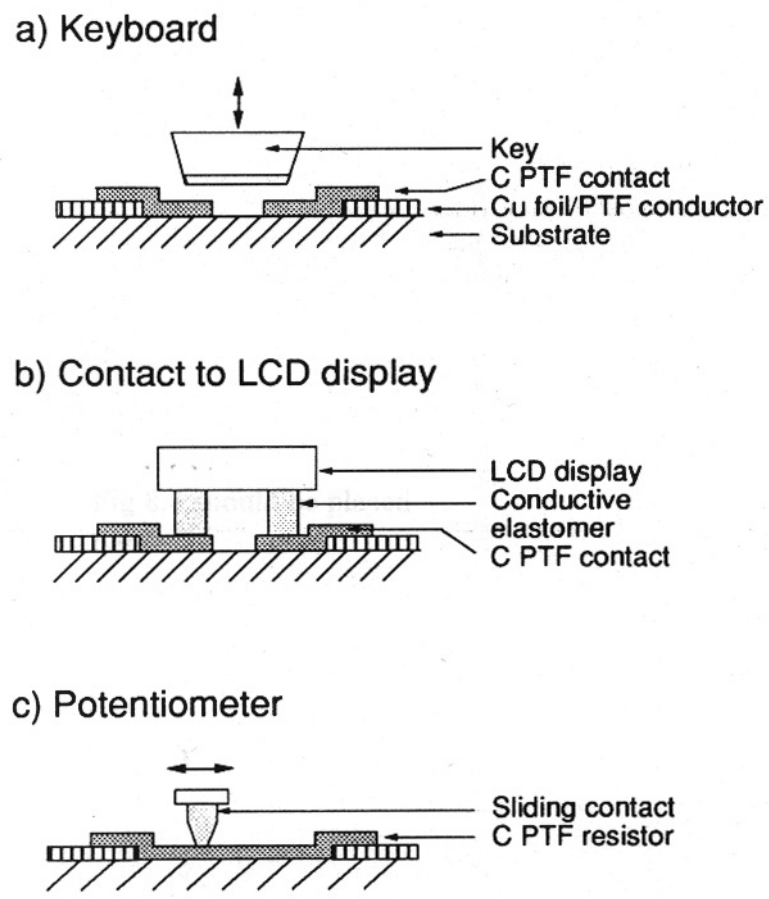


Fig. 8.8 Polymer Thick film (PTF) carbon technology, for:
a): Keyboard contacts.
b): Contacts of LCD-displays.
c): Sliding potentiometer [8.5].
CPTF means carbon type PTF

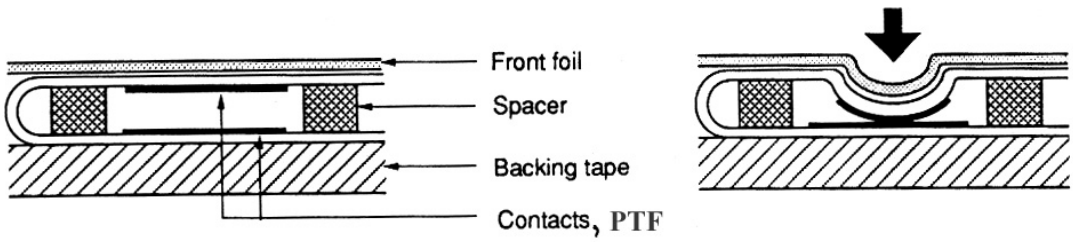


Fig. 8.9 Membrane switch panel, principle [8.5]

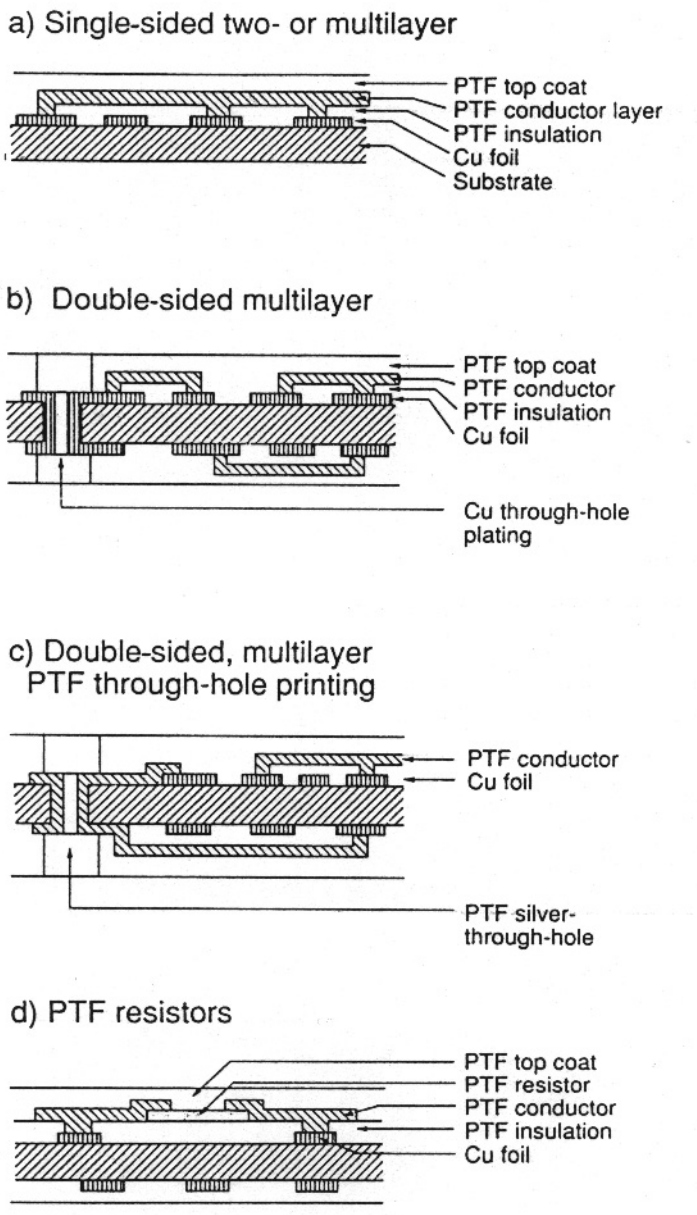


Fig. 8.10 PTF based printed wiring boards:
a): Single sided board with PTF for one complete conductor layer on top of one Cu foil conductor plate.
b): Double sided, through hole plated board with one extra PTF conductor layer on each side.
c): Double sided board through hole printed PTF conductor, instead of through hole plating d): PTF resistor [8.5].

PTF is much used for membrane switch panels, as mentioned above. To some extent ordinary, flexible boards of types 1 - 3 are also made.

The simpler varieties of PTF are used extensively in consumer electronics from the Far East. Its use in the USA and Europe is considerably less, but Finland has been a European pioneer country.

8.3.2 Materials

The conductor pastes and the resistor pastes consist of conducting particles in a matrix of polymers that serves as a binder and in addition to give adhesion to the substrate. Solvents are added to give the desirable printing properties. The insulating pastes have no conductive particles.

The polymer matrix

Thermoplastic as well as thermosetting polymers are used, please refer to Chapters 3 and 5. The first type is completely cured before use. The desired viscosity for printing is achieved by adding solvents, and the polymer solidifies by evaporation of the solvent.

The thermoplastic materials have lower strength as binders, and (often) poorer adhesion to the substrate. In addition, this type of polymers will have poor resistance to various solvents. On the other hand, they are very simple to use. Thermoplastic materials are used primarily for membrane switch panels.

Most PTF pastes for rigid boards are composed of thermosetting polymers. Cross linking takes place during the curing process, and the matrix becomes stronger. The most common types are phenol-, epoxy- and polyimide based. Various types of polymers may be in a mixture.

The curing is done in a regular convection furnace, by IR heating, microwave heating or vapour phase condensation heating, analogous to the vapour phase reflow soldering. The two first methods are the most common.

Many pastes have UV cured polymers. Such pastes are often solvent free. This gives certain advantages regarding dimensional stability from the printing to the completely cured product. Such pastes contain substances that catalyse the polymerisation process when the paste is irradiated with UV light. They are primarily used as dielectrics.

Active ingredients

Silver is used the most as conductive element, but also copper or carbon. The choice of the best suited active material depends on the requirements for the conductors. Silver has high electrical conductivity and gives no problems with regard to oxidation of the surface. However, silver based pastes give migration problems. Furthermore, they normally require plating of another metal on top to be solderable. Copper has approximately the same electrical conductivity as silver and gives considerably less migration problems. However, copper may give problems with oxidation of the surface, poor solderability and high contact resistance. There are also copper pastes that are directly solderable.

Asahi Chemical, in Japan, produces a copper paste that is close to insulating after being printed. Metallic copper is plated on top of the printed pattern by chemical plating (without external current, please refer to Chapter 3). Then the sheet resistance is the same as for Cu foil of the same thickness.

Carbon has considerably poorer conductivity than silver and copper and is suitable only for special conductors, such as keyboard contacts with low current. However, carbon gives neither migration nor oxidation problems, and it is so stable that it is normally unnecessary to cover it with an insulating top layer. Carbon is also used as the dominant active ingredient in resistor pastes.

In addition to the electrically conducting ingredients, we often have additives that contribute to give the right consistency and colour, particularly in the dielectrics. These may be of different types, for example ceramic particles.

The homogeneity of the paste mixture is of great importance for the result. A certain degree of sedimentation will always take place during storage, and good mixing is necessary before use. For resistor pastes this may reduce the predictability and repeatability of the resistor values at printing. Japanese producers often make their own resistor pastes immediately before use, in order to avoid this problem. However, normally the commercially available resistor pastes may be used with good results.

8.3.3 Typical process

Below we give a typical process for types 2 - 4 boards (Section 8.3.1). The starting material is a laminate with a single sided etched conductor pattern in Cu foil.

1. Cleaning of the board
2. Printing of PTF insulation layer, 2 prints, drying in between
3. Drying
4. UV curing
5. Printing of PTF conductor
6. Drying
7. Curing in IR in-line furnace
8. Chemical plating of metal (Optional)
9. Printing of top layer
10. Drying
11. Curing in IR furnace.

It is most common for PTF conductors to use Ag-based or Cu-based conductor material. Step 8, chemical plating, may be done on top of Ag in order to improve the solderability of the PTF conductor on the solder lands. It is also used on Cu platable conductor paste, as mentioned earlier. The process for the chemical Cu plating is similar to that which is used in production of through hole plated printed wiring boards. The details are given in Chapter 5 and [8.18].

Detailed design rules are given in [8.5 b)].

8.4 THIN FILM HYBRID TECHNOLOGY

8.4.1 Conventional thin film technology: Substrates and materials

Thin film circuits consist of conductor layers, resistor layers and dielectric layers, similarly to thick film circuits. However, the thin film thicknesses are normally 1 μm or less, an order of magnitude less than for thick film. Processes from silicon technology are used for deposition and definition of patterns. That gives higher circuit density than in thick film. The materials are also generally different. In this section, we shall concentrate on the form of thin film hybrid technology that has been in use since the 1960´s, with one layer of conductor, one layer of resistor and an inorganic dielectric.

The substrate materials that are used the most, are glass and 99.6 % alumina. The fine conductor dimensions in thin film require a smoother and more uniform surface underneath, so the substrates are polished. For high frequency use, low losses are important and the purer quality alumina, used in thin film circuits, has lower tan δ than the substrates used in thick film technology, Table 8.1.

The metals that are used the most for thin film conductors are gold and aluminium. Gold is chemically stable, it has high electrical conductivity and good bondability. However, as previously mentioned, gold diffuses very fast into many other conductor and insulating materials. Together with gold special elements are used as diffusion barriers, and in addition as adhesion layers, because gold has poor adhesion to many materials. Nickel is suitable for diffusion barrier, a nickel/chromium alloy improves the adhesion, and it is also suitable as resistor material, see below. The much used Au - NiCr system is deposited by vacuum evaporation or by sputtering, please refer to Chapter 3. Gold may also be electrolytically plated, particularly for microwave circuits, where a 5 - 10 μm thick layer gives low conductor resistance, which is important to achieve low high frequency loss. (Please refer to Section 6.7).

Aluminium is used much as electrode material for thin film capacitors. Various materials are used for dielectric depending on whether one wants to make capacitors, multilayer insulation or passivation. For passivation SiN_3 is well suited. SiO_2 is used much for insulation between conductor layers, because it has low dielectric constant ($\varepsilon_r = 4$), and high breakdown field strength (10^6 V/cm). Both are produced by chemical vapour phase deposition. For capacitor dielectric SiO is used, or SiO_2, Al_2O_3, Ta_2O_5. They are produced by vacuum evaporation, or chemical deposition, or anodic oxidation [8.2].

Resistors are made, as mentioned, from NiCr, as well as Ta_2N, by vacuum evaporation or by sputtering.

While we can achieve over 6 decades of variation in sheet resistivity in thick film hybrid technology, the range we achieve with practical thicknesses in thin film technology is only between approximately 10 and 1000 ohm/sq. Some properties are shown in Table 8.5, and more details about all thin film materials and deposition processes are given in [8.1 - 8.3].

Table 8.5 Properties of thin film resistors
(δ: skin depth. Evap: Vacuum evaporation. Sp: Sputtering) [8.3]

Material	*Specific Surface Resistance ($t << \delta$), $R_f = \rho / t$ (in ohm)*	*Temperature Coefficient of the resistance, $\Delta R/(R\ \Delta T)$ (in $10^{-6}/°K$)*	*Stability $\Delta R/(R\ \Delta T)$ (in %/1000h)*	*Production method*
NiCr (nickel-chrome)	40 - 250	-100 - +100	<0,2 good	Evap
Cr (chrome)	10 - 500	-300 - +300	medium	Evap
Ta (tantalum)	40 - 200	-200 - +200	<1 medium	Sp
Ta_2N (tantalum-nitride)	10 - 100	-60 - +30	<0,2 good	Reactive sp
Ti (Titanium)	5 - 2000	-500 - +500	medium	Evap
Cr-SiO Cement	500 - 2000	-250 - +250	<0,5 medium	Flash sp

8.4.2 Production process

Figure 8.11 shows the process steps for the most common form of thin film circuits, with one conductor layer and one resistor layer. In the first step, the resistor layer is deposited all over the substrate. If the circuits are small, many circuits are made on the same substrate, and they are separated at the end of the production process. A diffusion barrier is deposited and then the conductor metal. It is preferably done in the same vacuum chamber, in order to have a clean surface and good adhesion. These are standard processes that require special equipment and clean room facilities, normally smaller thin film circuit producer companies will buy the substrates processed to this stage.

Conductor and resistor geometries are defined by photolithography and etching. A few drops of photoresist are deposited and spread by the centrifugal force when the substrate is rotated on a spinning table. The conductor pattern for circuits is defined by exposing the resist through a photo mask, development and curing. Then the gold is removed by etching where it is not wanted. A solution of potassium iodide may be used, without dissolving the NiCr layer. If the need exists for conductor widths less than 2-3 μm, the etching is done by reactive ion etching, which etches fast vertically, but more slowly horizontally, and thus reducing the underetching.

A new step of photoprocessing is done to define the pattern of the resistors, and the diffusion barrier and the resistor films are etched where they are to be removed, for example with nitric acid. (Where the circuit has conductor pattern, there is still the resistor layer underneath the conductor material, see Figure 8.12.)

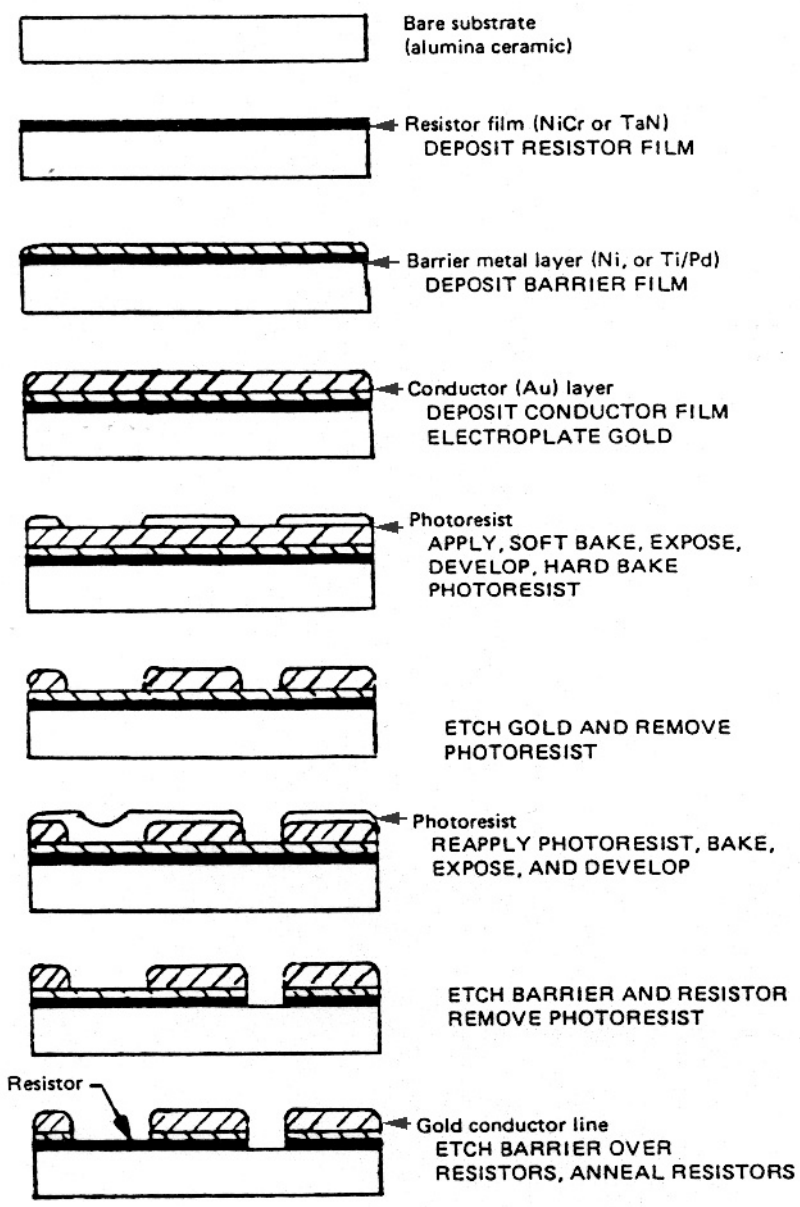


Fig. 8.11 Process flow for production of thin film hybrid circuits

Finally, the circuit is cured in air at 250 - 350 °C for some hours, to make a passivating layer of chromium-oxide to protect and stabilise the resistors.

An example of a microwave circuit that has plated gold conductors and capacitors is shown in Figure 8.13.

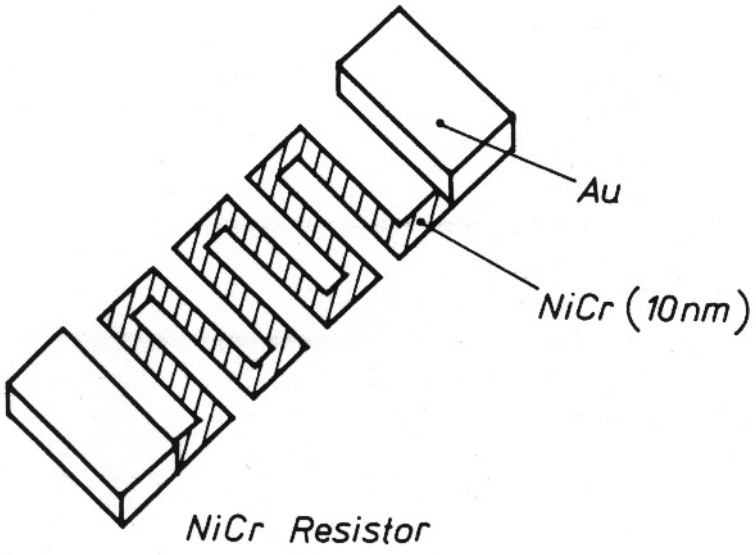


Fig. 8.12 Structure of thin film resistor with gold termination.

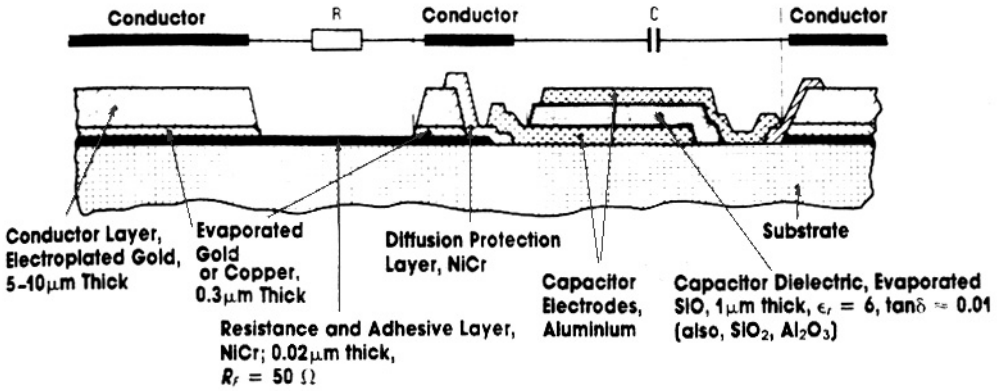


Fig. 8.13 Thin film microwave circuit, schematically [8.3].

Thin film components

A type of "components" that is very suitable for being made by thin film technology is precision R/C networks. They are also available as off-the-shelf components for mounting on other thin- or thick film substrates.

Diodes and transistors can also be fabricated. Large thin film diodes made from Cu_2S/CdS hetero-junctions give low price solar cells, and thin film transistors have been under development for 10 - 15 years. A matrix of thin film transistors is of great interest for the control of big LCD screens for flat televisions, etc. The structure is similar to Si -MOS transistors, see Figure 8.14, and CdSe as well as Si/H are used as the semiconducting material.

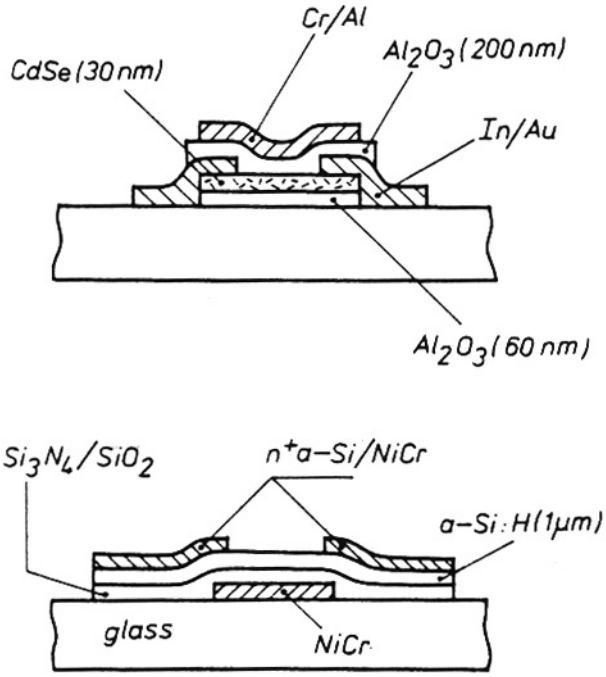


Fig. 8.14 Thin film transistors, structure [8.2]

The complete thin film circuit

When the thin film substrate has been completely processed, resistors may be laser trimmed like in the case of thick film circuits. After this, components will be mounted on the substrate. Integrated circuits are normally mounted in the form of naked chips that are glued on to the substrate and wire bonded. Discrete resistors and capacitors are normally mounted with conductive adhesives for electrical and mechanical contact and not soldered. In most cases, the complete circuit will be mounted in a hermetic package that is made of ceramic, or in most cases of metal. Terminal points on the substrate will be connected to the leads of the package by wire bonding. A welded or soldered metal lid on the package ensures hermeticity and good reliability.

8.4.3 Multilayer thin film, multichip modules

This is an extension of conventional thin film technology, but with many conductor layers, that makes it possible to achieve a very high circuit density. We may also achieve a controlled characteristic impedance and good high frequency properties. Multilayer thin film is one of the technologies for multichip modules, MCM-D, as mentioned in Section 2.7.

The normal substrates are either 99.6 % alumina or silicon wafers. Figure 8.15 shows a cross section. The dielectric most often used is polyimide, approximately 10 µm thick. Al, Cu, and Au are used as conductor metals. IC process technology makes it possible to achieve a minimum conductor width/distance of 25 µm or less, i.e. a higher conductor density than any other

substrate technology (except full wafer scale integration). AT&T has been a pioneer in this technology. Over 100 companies and research labs had this technology under development/production in 1992 and it will be a mainstream technology for high performance systems during the coming years. One high performance product employing the technology is the mainframe computer VAX 9000, of Digital Equipment Corporation. Si substrates are used and TAB-mounted Si chips [8.16].

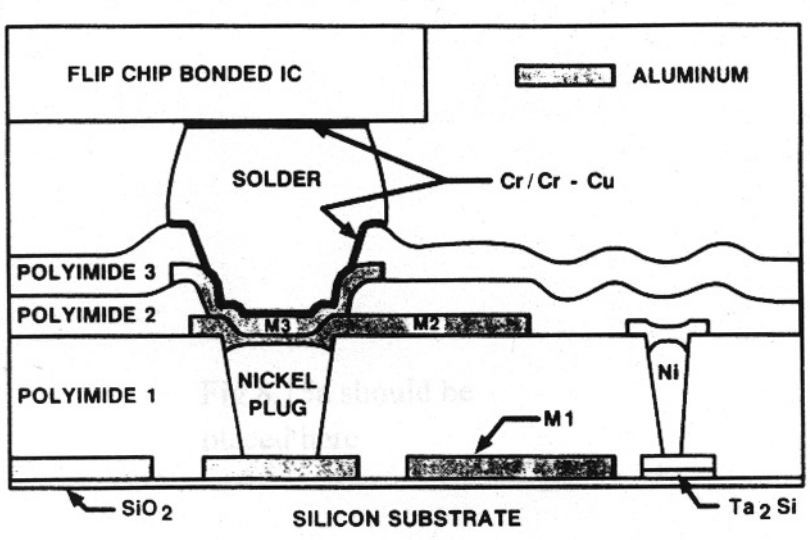


Fig. 8.15 a): AT&T´s structure for multilayer thin film [8.25]. See also Figure 2.13 [8.7]

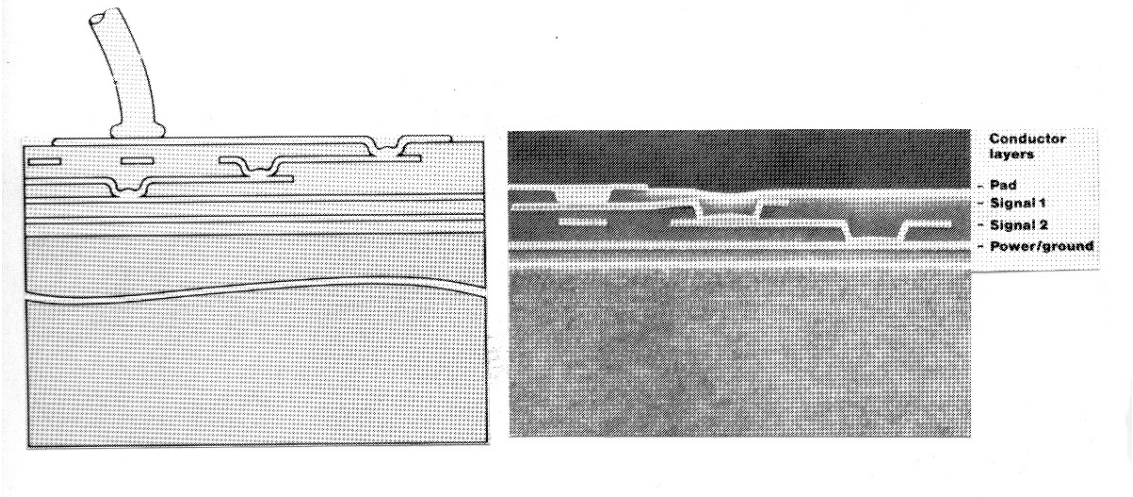


Fig. 8.15 b): Cross section of Raychem´s High Density Interconnect (HDI) schematically and observed through microscope

A typical process is as follows:

1. Spinning of polyimide insulation
2. Deposition of Al metallisation (sputtering, 5 µm, R=6 mohm/sq)
3. Photolithography and wet etch of conductor pattern
4. Spinning of polyimide
5. Etching of via holes. Several methods are used, this is a critical point.
6. Repetition of steps 1 - 5 for multilayer
7. Metallisation and etching of the surface metal (5 µm Al or 2 µm Au).

Some design rules for Raychem´s "High density interconnect" (HDI) technology are shown in Figure 8.16 [8.8]. The characteristic impedance as a function of the ratio conductor width/dielectric thickness is shown in Figure 8.17. Tan ∂ of the dielectric and typical attenuation as function of the frequency are shown in Figure 8.18. We see that all the way up to 10 GHz the losses in the conductor dominate, the dielectric loss is negligible. The dielectric constant depends on the moisture absorption in the polyimide: ε_r = 3.4 (dry) and 4.5 (maximum moisture content, 3.5 %). Much work is in progress to develop new types of polyimide and alternative materials that are less hygroscopic.

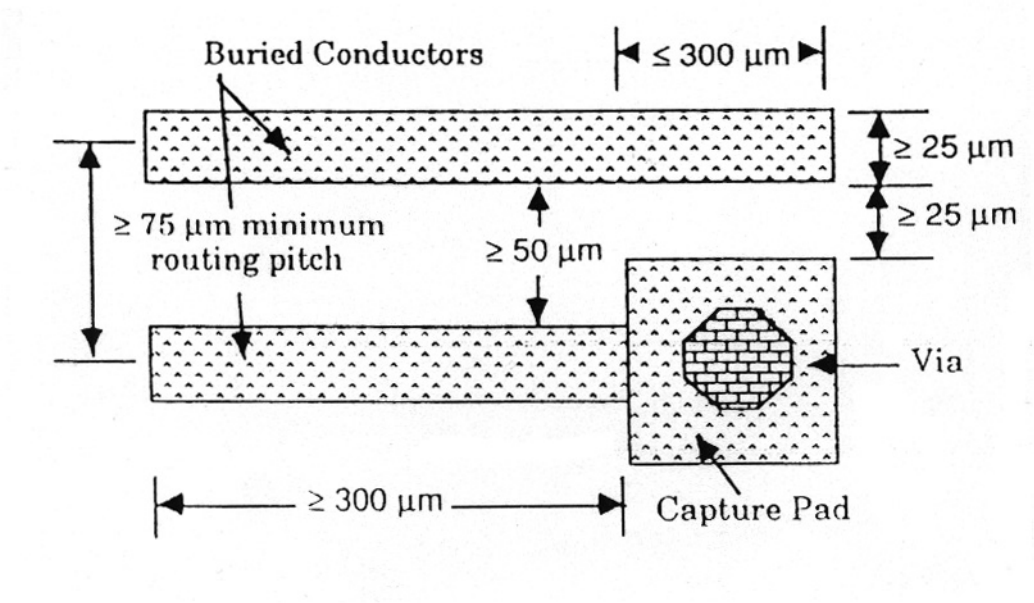


Fig. 8.16 Elements of the design rules for Raychem´s HDI technology [8.8]

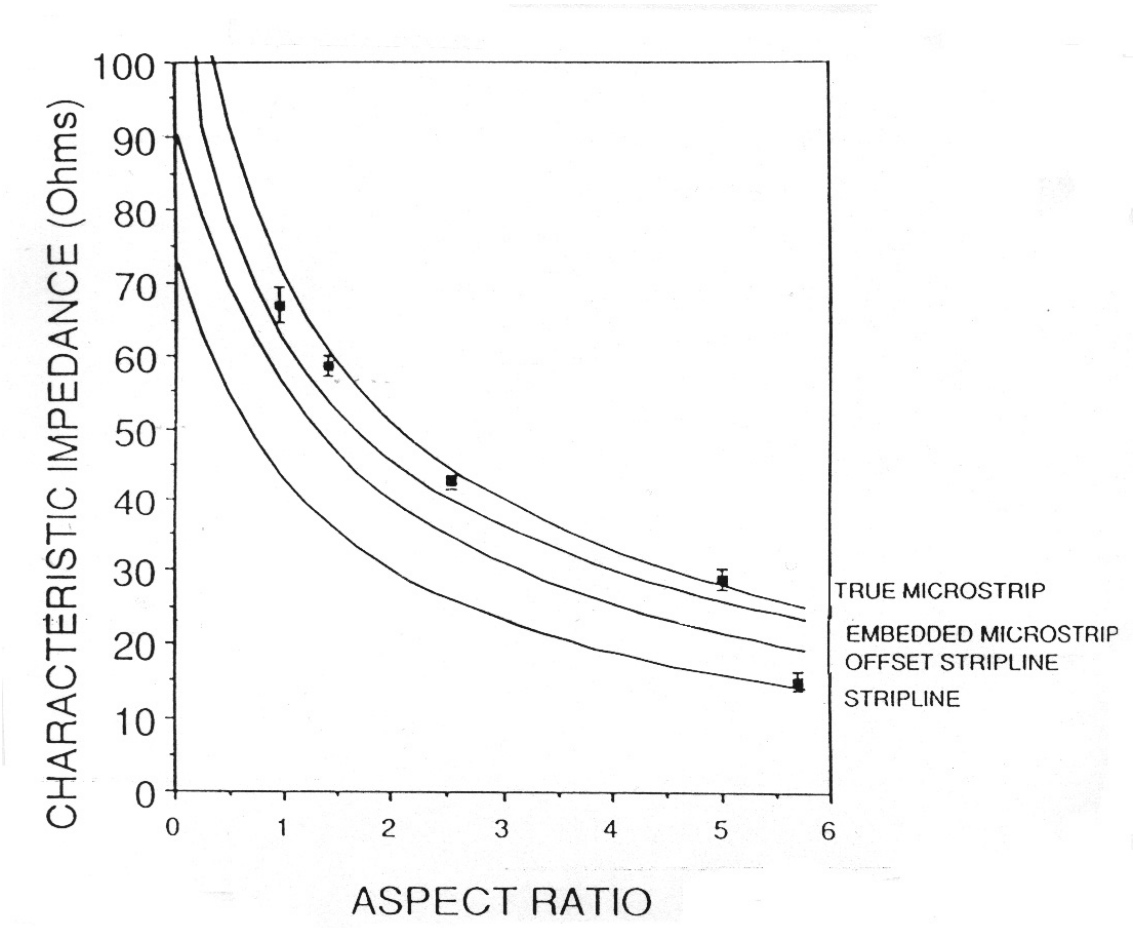


Fig. 8.17 Characteristic impedance for Raychem´s HDI as function of the ratio between conductors width and dielectric thickness.[8.8]

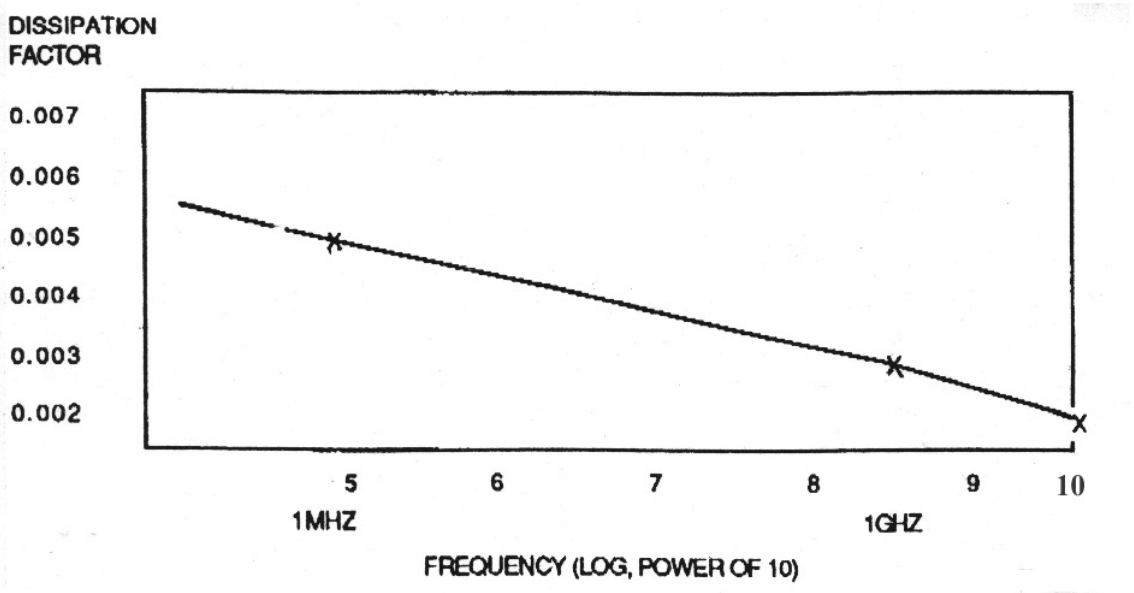


Fig. 8.18a): Dissipation factor for Raychem´s HDI [8.8]

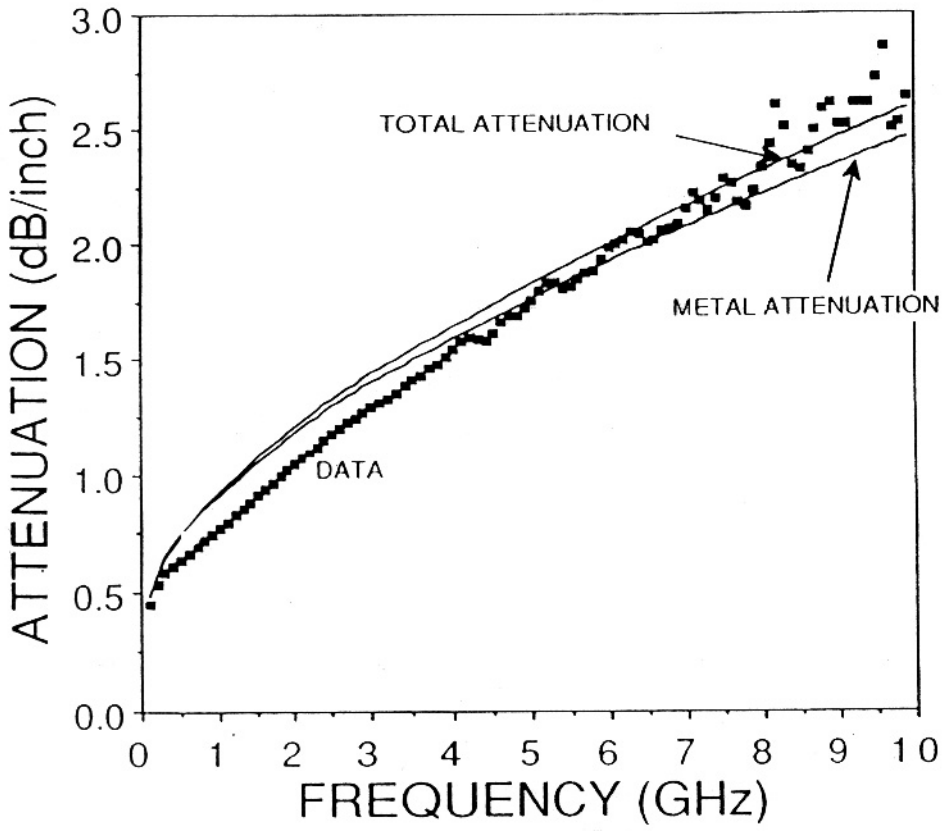


Fig. 8.18. b): Typical attenuation, as function of frequency, for Raychem´s HDI [8.8] Even at 10 GHz attenuation in the conductor metal dominates

For ICs with high dissipation it is possible to make a "thermal well", by mounting the chip directly on the substrate, without the polyimide. This is used in the VAX 9000 computer, where ECL technology gives high power dissipation.

Some advantages of multilayer thin film with Si substrates:
- Optimal thermal match between Si substrate and Si chip components
- Very good thermal conductivity in Si substrate: 150 W/°C m
- Termination resistors and decoupling capacitors may be integrated in the substrate
- Compatibility with wire bonding, TAB and flip chip. Also with gluing of discrete components
- Very high conductor density and package density
- Very good high frequency properties due to short wire lengths, low ε_r and low losses in the dielectric
- Very good mechanical properties in the Si substrate materials
- High reliability when it is hermetically encapsulated.

Some disadvantages:
- Thus far; low availability and high cost
- Polyimide is hygroscopic, and the moisture uptake may give swelling and corrosion over long time. Hermetic encapsulation is necessary.
- Immature technology.

8.5 MULTILAYER CERAMIC MODULES

8.5.1 High temperature ceramics

High temperature multilayer ceramic technology has been used for many years for ceramic capacitors and for IC packages. For packages and multichip modules, Al_2O_3 and AlN (BeO and SiC to a smaller extent) are used. For multichip modules, alumina is the most used material, with 92 - 96 % Al_2O_3 content. The structure consists of many layers of ceramic, with metallisation between the layers, and via holes through the layers for electrical contact. The best known application of large modules with many layers of ceramic is IBM´s pioneering product "thermal module" [8.6] for mainframe computers, already in 1983. The module had over 30 layers, and about 100 ECL silicon chips were mounted by flip chip soldering. Later various mainframe computer makers have used analogous technology, based on materials with even better thermal conductivity.

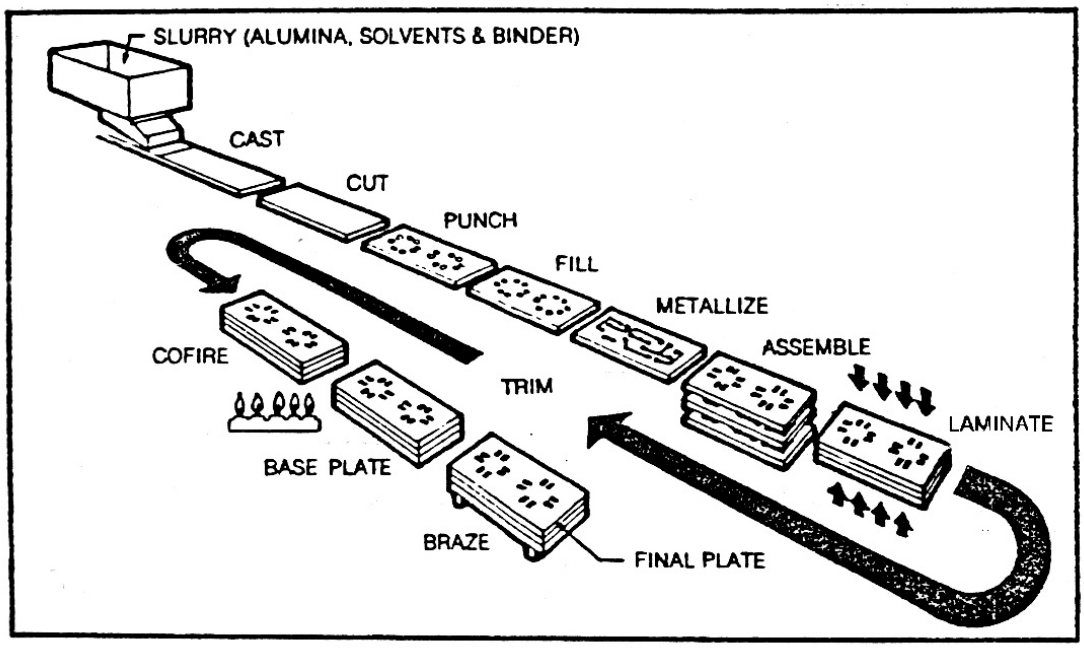


Fig. 8.19 Production process for multilayer ceramic, schematically

Fabrication

The fabrication of multilayer ceramic modules by "tape casting" is shown schematically in Figure 8.19. The non-sintered, pliable ceramic consists of alumina powder, organic binders and solvents. The material is spread from a container down on a transport carrier underneath. The ceramic "tape" ("green sheet"), is given the appropriate thickness on the transport carrier by passing underneath a "doctor blade" in a precisely controlled distance. The tape is cut to correct size, and holes and component cavities are punched out with a numerically controlled punching tool or with a permanent, product specific punching tool for high production volume of a given product. Metallisation of the via holes and fabrication of conductors is done by screen printing of tungsten (or molybdenum). These are the only metals that can withstand the high process temperature later. All layers are laminated together under hydrostatic (or uniaxial) pressure at elevated temperature, to evaporate the binder and solvent. Then the whole structure is sintered at 1500 - 1700 °C, 30 - 50 hours, in hydrogen atmosphere. For small circuits, many circuits are made on one laminate, and the individual circuits can be parted by breaking the substrate at the end of the process. Then the external contacts are brazed to the substrate and finally gold may be plated on the surface with nickel as diffusion barrier on top of the tungsten. The plating is preferably done electrolytically to achieve sufficient thickness and good conductivity, if one can make electrical contact to all parts of the conductor pattern. Otherwise, chemical plating is used.

During the process, the ceramic shrinks approximately 18 % linearly. This has to be taken into consideration during the design of the circuit, both sideways and in thickness (which affects the characteristic impedance). Normally the designer will operate in correct dimensions and the producer will scale the CAD information up by the necessary amount for production of printing screens and punching tools. The shrinkage is material- and process dependent, so the finished circuits typically have linear dimensional tolerances 0.5 - 1 %.

Properties

Some electrical, physical and mechanical properties are shown in Figure 8.20. Black ceramic is used the most, the white material has somewhat higher purity and better properties at high frequencies, but it is transparent in a range of light wavelengths and is more expensive.

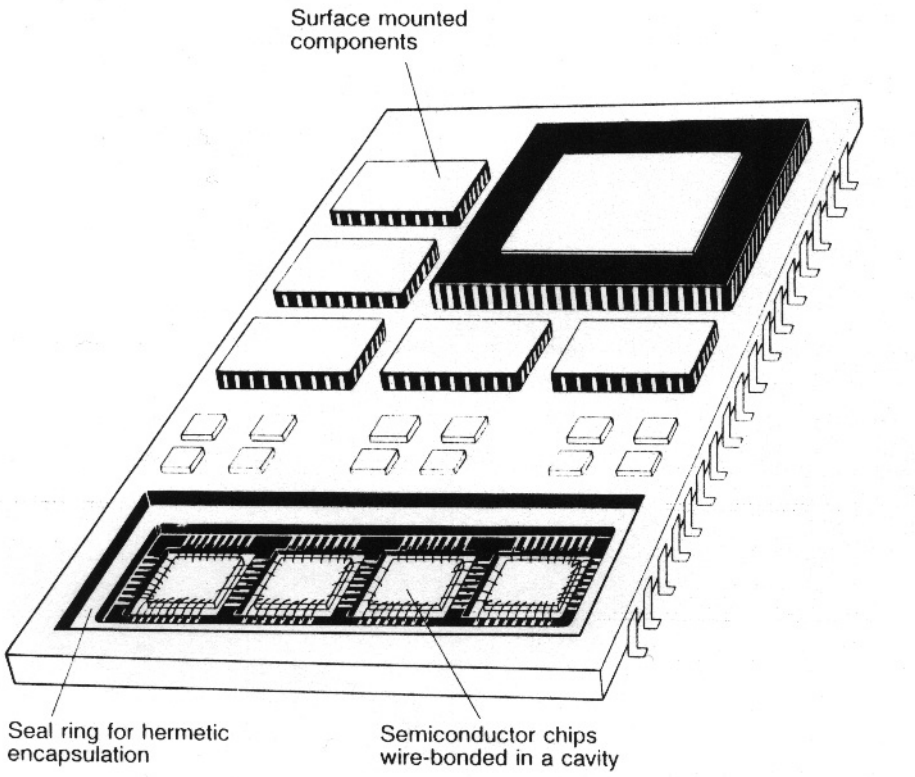


Fig. 8.20 Combination of naked chips in cavities and soldered, packaged SMD components on multilayer ceramic module [8.11].

The minimum conductor widths and conductor distances are typically 0.15 - 0.2 mm, diameter of via holes 0.1 - 0.2 mm. Extended ground planes are made as grids of printed lines rather than continuous, due to the dissimilar thermal properties of metal and ceramic during sintering. The typical thickness of the printed W conductor layer is 15 µm, for electrolytically plated Au on the surface it is 2 µm or more, with a 2 µm Ni barrier/adhesion layer between the Au and W.

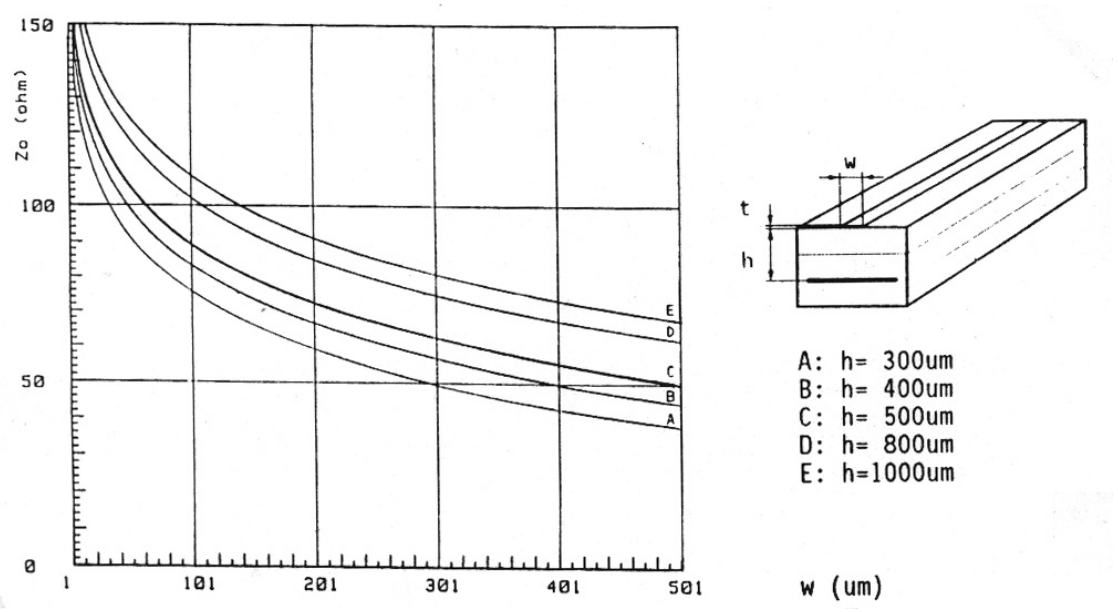


Fig. 8.21.a Characteristic impedance for typical geometries and dimensions, Al_2O_3-based multilayer ceramic: a): Open microstrip.[8.11]

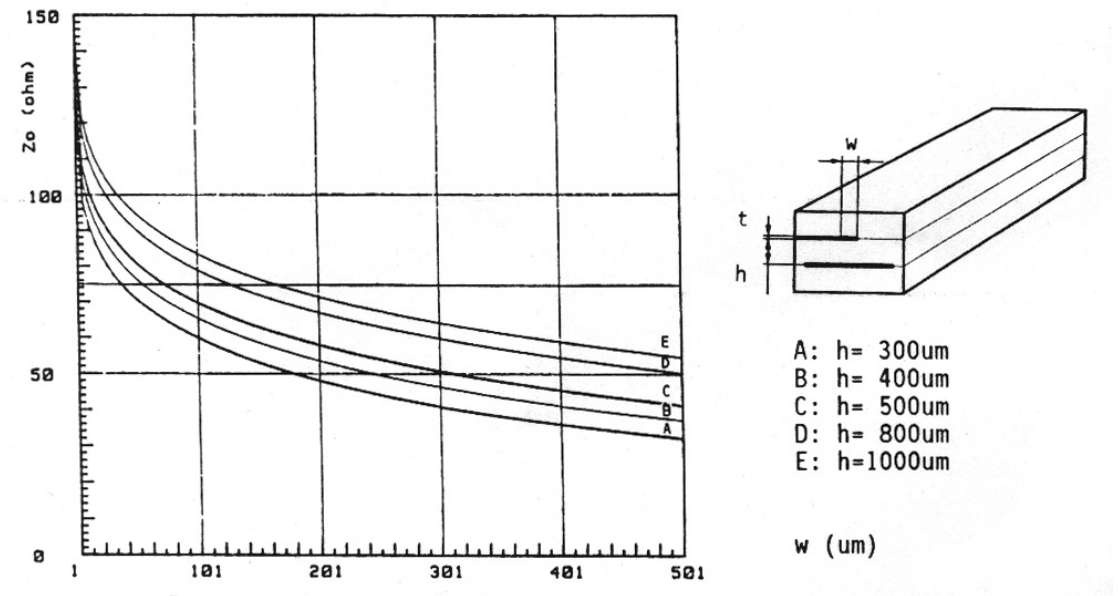


Fig. 8.21,b Characteristic impedance for typical geometries and dimensions, Al_2O_3-based multilayer ceramic: b): Buried microstrip.[8.11]

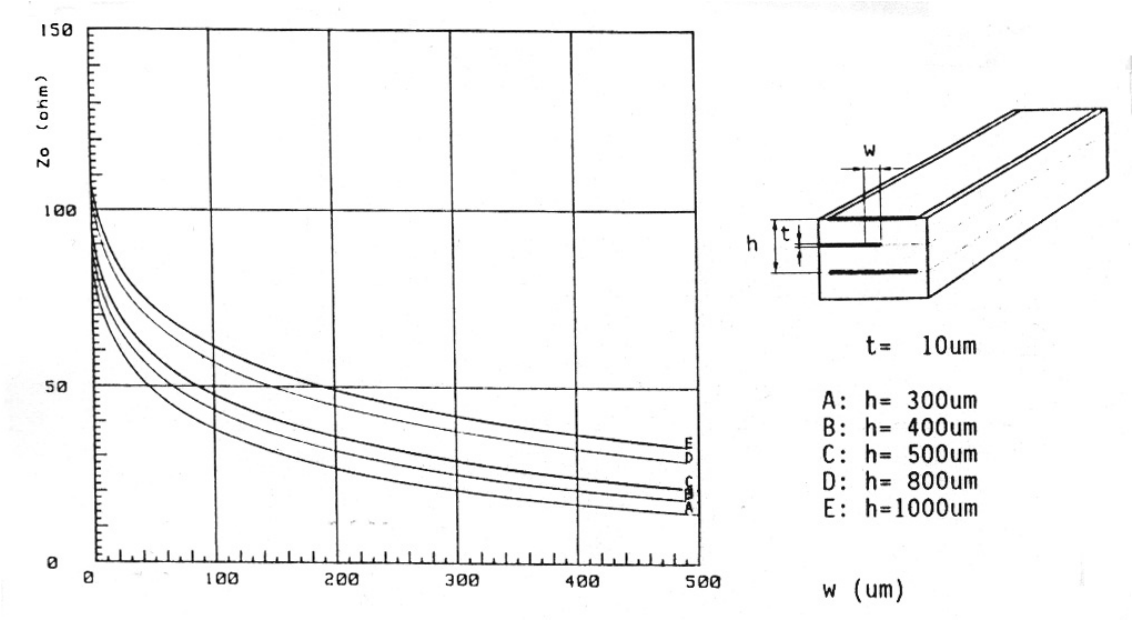


Fig. 8.21.c Characteristic impedance for typical geometries and dimensions, Al_2O_3-based multilayer ceramic: c): Stripline.[8.11]

The characteristic impedances for the common conductor geometries of multilayer ceramics are shown in Figure 8.21.

Among the advantages of high temperature multilayer ceramic are the following:

- High thermal conductivity
- Low TCE, good thermal match to Si and GaAs as well as to leadless SMD components
- Good control over characteristic impedance, good high frequency properties
- Both soldering of encapsulated components, TAB bonding of naked chips and flip chip mounting of smaller Si chips can be used (although there is not a perfect thermal match to flip chip soldered Si chips)
- Complete hermetic encapsulation is possible, or hermetic encapsulation of local areas, by using a lid over individual ICs in cavities, see Figure 8.21. High reliability.
- Many conductor layers are possible, with high production yield. This is because each layer can be inspected before the lamination, and faulty layers be discarded (contrary to thick film where one fault in one layer will ruin the whole circuit)
- Easy to mount edge contacts, coaxial contacts, etc.

Among the disadvantages are the following:

- Low electrical conductivity in the inner layers (sheet resistivity 15 mohm/sq)
- High dielectric constant gives delay, inferior pulse rise time and increased power loss and cross talk at very high frequencies
- The producers generally make standard packages in large volumes, and have high start-up cost for custom circuits.

Table 8.6: Properties of alumina-based high temperature multilayer ceramic [8.11].

Ceramic		Colour	
Property	Unit	Black	White
Al_2O_3 content	%	90	92
Density	g/cm^3	3,60	3,60
Rel. dielectric const. (1 MHz)		9,5	9,0
Loss tangent (1 MHz)	%	1,3	0,3
Breakdown field	kV/mm	10	10
Resistivity	ohm cm	10^{14}	10^{14}
Thermal coeff. of expansion (0-100°C)	ppm/°C	5,0	5,0
Thermal coeff. of expansion (0-300°C)	ppm/°C	6,5	6,5
Thermal conductivity	W/m x °C	15	17
Specific heat	W s/g x °C	80	84
Module of elasticity	N/mm^2	$3x10^5$	$3x10^5$
Conductors Property	Unit	Value	
Tungsten Sheet resistivity (0.1 mm con. width) (0.2 mm - " -) (0.3 mm - " -)	 mohm/□ 	 20 14 12	
Thermal coefficient of resistance	ppm/°C	4300	
Plated (W + Ni + Au) Sheet resistivity	 mohm/□	 3-4	

8.5.2 Low temperature multilayer ceramic

DuPont, IBM and others have introduced multilayer ceramic based on glass compositions similar to those used in thick film dielectrics, instead of alumina [8.12, 8.6, 8.21]. The fabrication is made in a process similar to that used for high temperature ceramic. The advantage of the low temperature technology is primarily that the sintering takes place at around 850 °C, 15 min., normally in air atmosphere (after a burnout at 350 °C to remove the organic binders and solvents). The effect of this is that the metal systems used in ordinary thick film technology are suitable for inner layers, with much better electrical conductivity than tungsten. Thick film firing furnaces may be used for the process. Resistors may also be printed in the inner layers. Materials in the substrate are mullite, corderite, lead borosilicate glass and others [8.21].

DuPont, one of those making the base materials, is promoting the technology among the thick film producers. The tape casting of the tape materials is done by DuPont and the user buys the tape mounted on a Mylar foil that is removed before the punching and printing. In Europe some three producers make custom designed low temperature ceramic circuits (1992), and many companies are testing out the technology. Several producers in the USA and Japan are making low temperature multilayer ceramic circuits, primarily for internal use.

Table 8.7 Electrical and physical properties of low temperature multilayer ceramic [8.12 a]

a): Electrical properties.

	Resistance [mohm/sq]	Fired Thickness [μm]
Inner Layer (Co-fired)		
Gold	5	7
Silver	5	8
Silver/Platinum	20	8
Top Layer (Post fired)		
Gold	4	8
Platinum/Gold	80	15
Silver/Palladium	20	15
Silver	4	15

b): Resistor Performance - Resistance and TCR

	Over Tape		Over Thick Film Dielectric	
	R [ohm/sq]	HCTR [ppm/°C]	R [ohm/sq]	HCTR [ppm/°C]
100 ohm/sq	122	+20	102	+65
10 Kohm/sq	10,0 k	+71	12,5 k	+41
100 Kohm/sq	92,4 k	+75	95,7 k	+73

c) Physical Properties

Thermal expansion	
Fired dielectrics	7,9 ppm/°C
96% alumina	7,0 ppm/°C
Fired density	
Theoretical	3,02 g/cm^3
Actual	>2.89 g/cm^3 (>96%)
Camber	
Fired	±75 μm (±3 mil.)
68 x 68 mm^2 (2.7 x 2.7 in^2)	
Surface smoothness	
Fired dielectric	0,8 μm/50mm
50 x 50 mm^2 (2 x 2 in^2)	(Peak to peak)
Thermal conductivity	
Fired dielectric	15 - 25% of alumina
Flexure strength	
Fired dielectric	2,1x10^3 kg/cm^2 (3,0x10^4 psi)
96% Alumina	3,8x10^3 kg/cm^2 (5,6x10^4 psi)
Flexure modulus	
Fired dielectric	1,8x10^6 kg/cm^2 (2,5x10^7 psi)
96% Alumina	0,9x10^6 kg/cm^2 (1,3x10^7 psi)

Many properties are similar to those of the high temperature system, but the thermal conductivity is about 5 times lower for the low temperature materials. The shrinkage is only approximately 12 %. The materials are more brittle than alumina, and they must be handled with caution. Some parameters are given in Table 8.7

Typical conductors minimum width and separation are 0.15 - 0.2 mm, diameter of the via hole 0.15 - 0.2 mm, and distance between via holes 0.25 - 0.4 mm. The DuPont tape is made in two standard thicknesses: 90 and 250 μm (after sintering). The surface roughness is approximately 1 μm, lot-to-lot variation of the shrinkage: 0.2 %. The relative dielectric constant ε_r = 7.5 - 8.0 (but materials with lower ε_r are available), tan δ = 0.2 - 1 %. Thermal conductivity K = 2 W/m °C. Buried, silver based conductors have quite good migration properties, and the resistors have properties similar to those of thick film resistors. Circuits with 20 layers of ceramic have been demonstrated, the potential is said to be over 40 [8.12].

Some advantages compared to high temperature multilayer ceramic technology are:

- Low process temperature, normal process atmosphere, requires low investments for thick film producers to start their own production ($ 100k - 200 k).
- Flexibility in choice of conductor materials, low sheet resistivity
- Plating is not necessary, bondable gold can be screen printed
- Resistors may be screen printed internally and on the surface
- Dielectric materials with relative dielectric constant down to 4 - 5 are used.

Disadvantages:

- New, immature technology
- Low thermal conductivity
- Brittle material, mechanically less robust
- So far, low availability.

A "transfer tape" version is also available, which is fired for each layer [8.14].

Various MCM technologies are compared in [8.22], and extensive treatment is given in the selected key reprints in [8.21].

8.6 TECHNOLOGY FOR POWER ELECTRONIC MODULES

8.6.1 General

In power electronic circuits and modules each transistor may over short periods of time conduct up to 100 A and more and occupy several square cm of silicon. Some of the major challenges are:

- Spread the heat from the silicon chip through a good thermal conductor underneath and reduce the total thermal resistance between chip and a good heat sink
- Reduce thermal stress due to material thermal mismatch
- Provide electrical insulation for voltages up to 2.5 kV and more
- Design for electromagnetic compatibility, particularly reduce the inductance to avoid large voltage spikes when large currents are switched on and off.

- Higher integration: Combining power and control on the same Si chip or on the same substrate, "smart power".

Technologies used for power circuits and modules include the following:
- Polymer on metal substrate technology
- Thick film technology
- Plated ceramic substrate technology
- Direct copper bonding (DCB) technology.
- Plasma sprayed dielectric on metal base.

8.6.2 Modest power levels

The polymer on metal technology is used for relatively low power and low voltage circuits. An Al or Cu plate is used for heat sink. It is oxidised to improve adhesion to the insulation that is organic, with additives to improve the thermal conductivity. A 35 or 70 μm Cu foil is laminated on top to provide wiring. Packaged chips are soldered on, or alternatively naked chips may be mounted with silver loaded adhesive or soldered, and wire bonded.

The thick film hybrid technology is similar to the technology described in Section 8.3, with especially wide and thick printed conductors and Al_2O_3 or AlN substrates.

In plated ceramic technology the substrate is first chemically etched in order to roughen the surface. Then a thick Cu conductor layer is plated by chemical and then electrolytic processes, and the conductor pattern is etched [8.27].

8.6.3 High power modules

Direct copper bonding (DCB) substrates have alumina or AlN ceramic insulator, typically 0.6 mm thick, and a 0.3 mm thick Cu foil on both sides [8.19]. The oxidised Cu is bonded to the ceramic by heating to a temperature slightly above 1065 ^{o}C, 20 °C below the melting point of copper. At 1065 ^{o}C a eutectic composition of Cu and 1.6 % CuO has its melting point. The molten phase wets alumina and creates a strong bond to the ceramic upon solidifying, by penetrating into the molecular structure of the ceramic. Since the copper itself does not melt, a pre-structured pattern of the foil will be maintained after the bonding process. Alternatively a uniform Cu foil may be bonded and patterned by etching. In case of AlN, a pre-oxidation step transforms the AlN surface layer into Al_2O_3 and the interface layer will be the same as for alumina ceramic [8.20]. It is important to have Cu on both sides of the ceramic, to equalise the thermal stress and reduce bowing of the substrate.

The thermal resistance is reduced by using thick Cu layers. This, however, will increase the thermal coefficient of expansion for the composition, see Figure 8.22 a), and increase the thermal mismatch to Si chips. The reliability of the DCB structure under temperature cycling will also be reduced, see Figure 8.22 b).

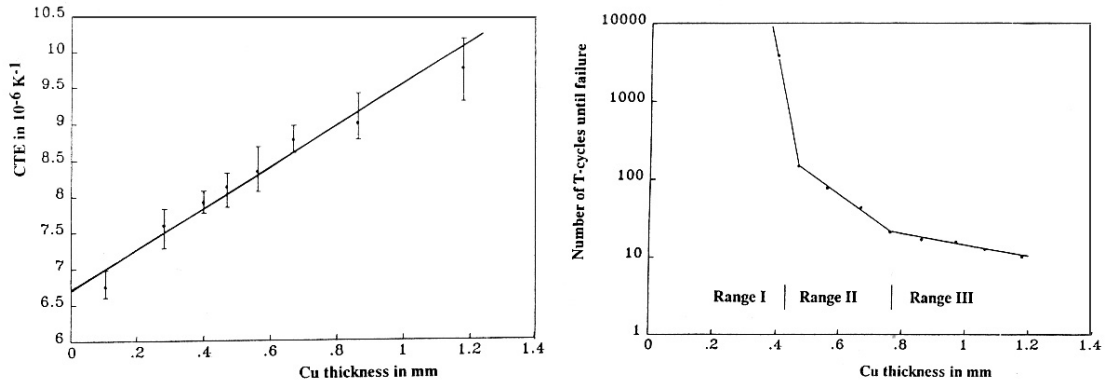


Fig. 8.22 a): The coefficient of thermal expansion for direct copper bonding (DCB) substrates with a layer of 0,6 mm alumina sandwiched between Cu layers of various thicknesses as given in the figure.
b): The number of thermal cycles to fracture for DCB substrates with varies Cu thickness. The cycles were in the temperature interval -40 - + 110°C [8.19]

The silicon chips are soldered to the substrates by high melting point solder in an inert or reducing atmosphere, and electrical connections are made by heavy Al wires. Many wires are used for each contact to reduce resistance and inductance.

In some modules the substrate is soldered to a heavy Cu plate, see Figure 8.23, for further heat spreading.

The complete modules are mounted to the heat sink below by screws. A thin layer of thermally conducting grease between module and heat sink will add significantly to the thermal resistance.

To improve the heat spreading in the substrate AlN with thermal conductivity up to 270 W/^{o}C m has been developed [8.28]. Even better thermal conductors than alumina and AlN are desirable for the dielectric in power modules. A big research effort has been started for deposition of diamond layers, with thermal conductivity of 1 000 - 2 000 W/^{o}C x m [8.29].

To reduce the cost and to facilitate production of high power modules with larger area than the DCB modules, a technology based on plasma spraying of alumina ceramic on aluminium base plates or heat sinks has been developed [8.30]. On top of the ceramic, it is then possible to spray Cu metallisation through a metal mask, providing the conductor pattern. The thermal properties are not so good as those of DCB, due to porosity of the ceramic. Furthermore, the Si chips are mounted with adhesive, giving additional thermal resistance [8.31].

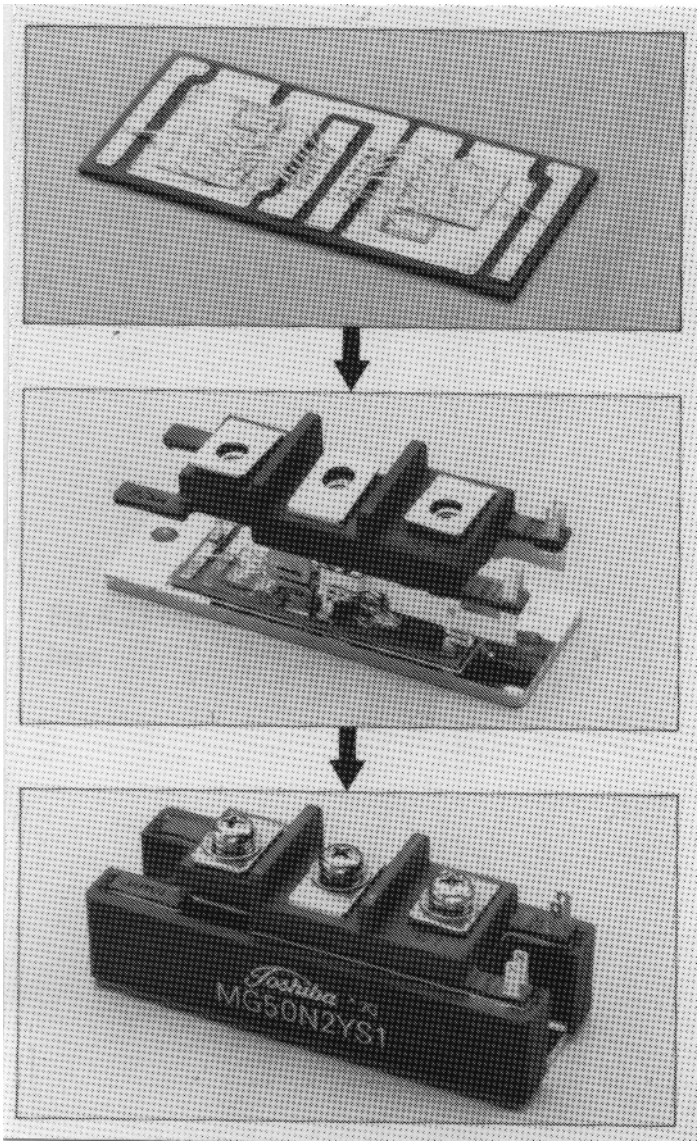


Fig. 8.23 Power electronic module [Toshiba data sheet]. The substrate (top) is DCB with AlN insulation. It is soldered to a heavy Cu plate, environmentally protected with silicone gel and mounted in a plastic package with heavy screw terminals. Each of the transistor chips and diode chips conducts up to 50 A current.

8.7 COMBINATION TECHNOLOGIES

8.7.1 Multilayer thin film on multilayer ceramic

The combination of multilayer thin film on top of multilayer ceramic is used for certain super computers, see Figure 8.24. It combines many of the advantages of both technologies. IBM has recently made a "thermal module" based on 63 layers low temperature ceramic and multilayer thin film on top [8.23].

These types of technologies are not available on the open market.

8.7.2 Thin film on thick film

AME in Horten, Norway, has developed a combination of regular thick film and regular thin film technology, see Figure 8.25. All slow and non-critical signals, in addition to ground and power planes, are made in thick film. On top are a ground plane, printed dielectric and one layer of thin film conductors for high speed signals with transmission line dimensions.

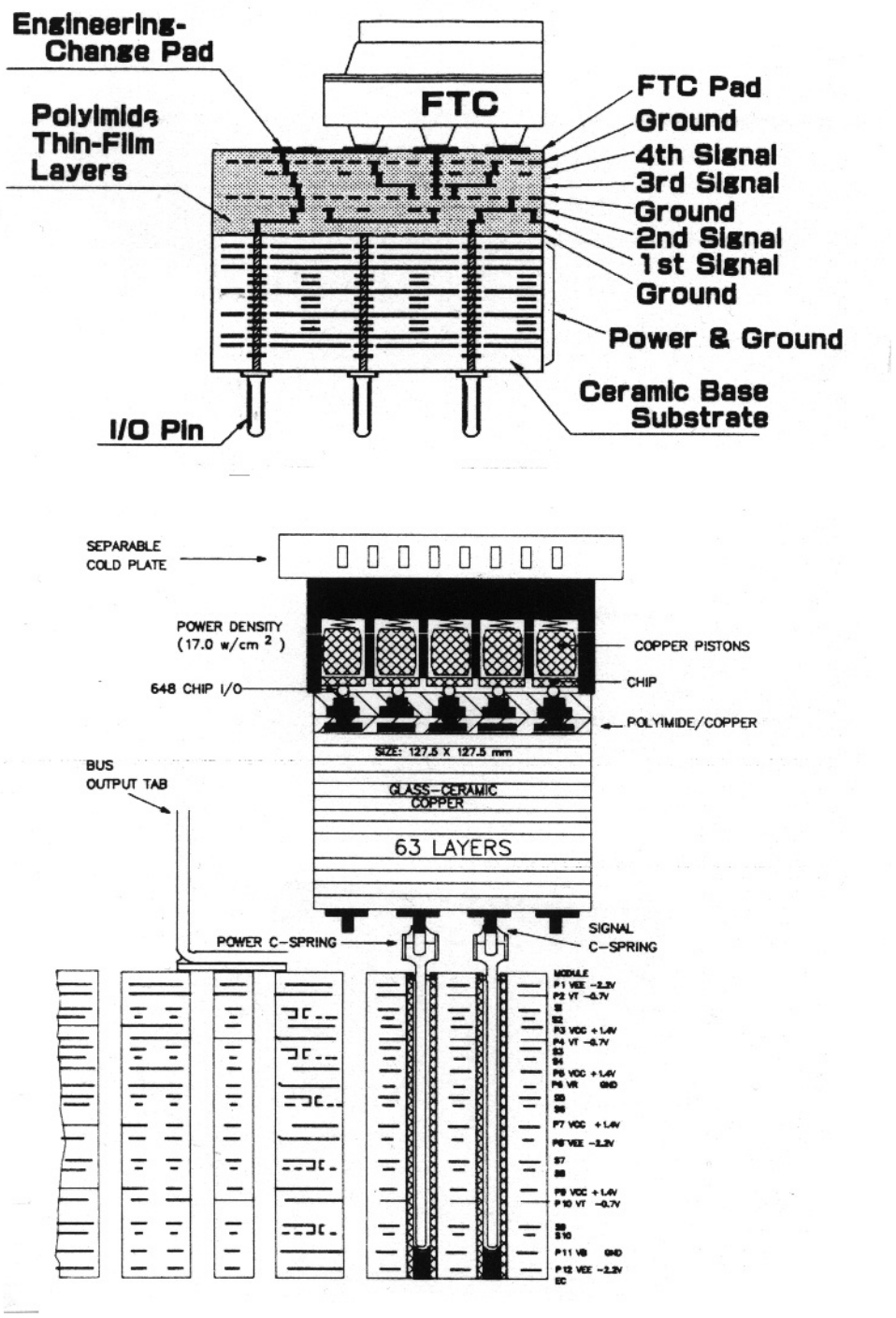
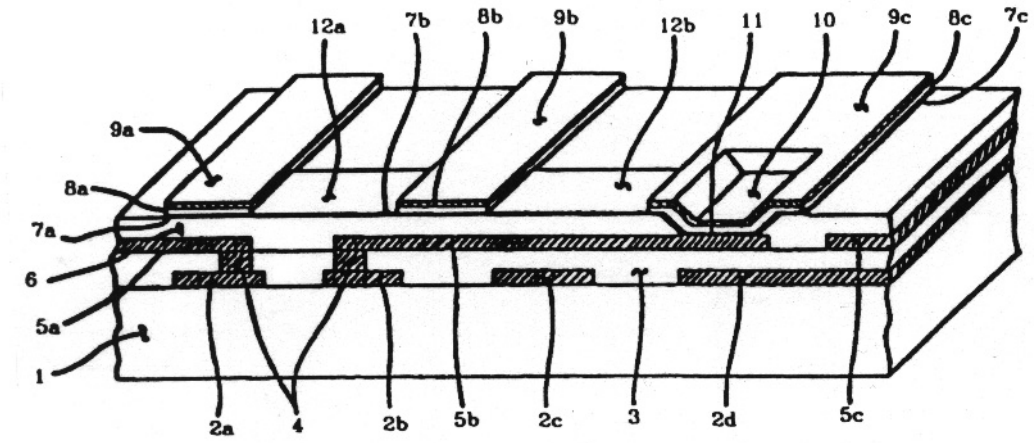


Fig. 8.24 High performance modules made in a combination of multilayer thin film and multi layer ceramic technology: a): NEC Corporation computer SX-3 [8.24] using flop TAB carrier on thin film and alumina based substrate, and b): IBM Enterprise System/9000 packaging hierarchy [8.23] using flip chip, polyimide/copper thin film on 63 layers glass ceramic substrate.



1	Alumina substrate.
2	a,b,c,d:Printed conductor on first layer.
3	Printed dielectric film.
4	Optional compensation printed in vias.
5	a,b,c: Printed conductor on second layer.
6	Glass based dielectric.
7	a,b,c,d: Tantalum nitride resistive layer.
8	a,b,c,d: Molybdenum diffusion barrier.
9	a,b,c: Thin film gold lines.
10	Via hole between thin film and thick film conductive layer.
11	Contact area in thick film. Gold-platinum or gold-palladium.
12	a,b: Resistor in thin film made by selective etching in thin film structure.

Fig. 8.25 AME´s combination technology combining thick film and thin film, cross section [8.25].

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