John Steinar Johnsen (Josse)

Senior Application Engineer

Electronics OTS
Norwegian School of Marketing

1972	Tandbergs Radiofabrikk A/S	R&D Dolby on cassette deck
1979	NorCad AS	Manager PCB Design
1989	Elektrisk Bureau / Elplex AS	IT Manager - PCB Production
1998	Elmatica AS	Sales & Application Engineer
2008	Elmatica AS	Senior Application Engineer

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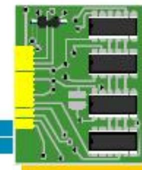
Program for 10. and 17. Mars 2014

Time, 12:15 – 14:00 both days.

- Mini BoardWalk, Schematic Simplified Tour of the PCB Manufacturing Processes
- A view on different PCB build up's, EMC considerations, PWR , GND and signals.
- Build in capasitance (BC Core), de-coupling
- Some stuff on PCB Materials, copper structure, glass and epoxy.
  Specify according to IPC 4101C/xxx
- Advanced HDI PCBs, microvia holes, buried vias, stacked and staggered microvia holes, buried holes.
- Design Rules, design aspects, errors seen.
- Introduction to Flexible and FlexRigid PCBs
- Introduction to MBPCB Metal Back PCB's. Aluminium for Power and LED applications.

Mini Board Walk



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PCB MANUFACTURING FLOW CHART

CUSTOMER
SALES DEPT
INPUT DATA
DATA PROCESS
P&M CONTROL
DRAWING
WORKING A/W
STENCIL
PROGRAMS
D.N.C
FLOW CHART

Buried via
I.V.H DRILLING
INNERLAYER SHEAR
DOUBLE SIDE
I.V.H. PLATING
INNERLAYER IMAGE
EXPOSURE
LAMINATION
PRELIM. TREATMENT
I/L ETCHING
STRIPPING
ETCHING
DEVELOPMENT
INNER LAYER PROCESS
AOI _ INSPECTION
LAY-UP
LAY-UP
BAKING
BLACK OXIDE
Multiple buried via
LAMINATION
POSTTREATMENT
LAMINATION
PRELIM. TREATMENT
LASER ABLATION
DRILLING

…to Plated Through Holes

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...from DRILLING

P.T.H. ← ELECTROLESS CU ← DESMER ← PRELIM. TREATMENT

PANEL PLATING

OUTER Layer

OUTER LAYER IMAGE ← EXPOSURE ← LAMINATION ← PRELIM. TREATMENT

TENTING PROCESS

PATTERN PLATING ← PURE TIN PLATING ← PATTERNPLATING

ETCHING ← TIN STRIPPING ← ETCHING ← STRIPPING

INSPECTION

PRELIM. TREATMENT → S/M COATING → PRE CURING

LIQUID S/M ← POST CURE ← DEVELOPING ← EXPOSURE

SCREEN LEGEND

ENIG → HOT AIR LEVELING ← G/F PLATING

E-LESS NI/AU

S/G PLATING

FINAL SHAPING

For OSP

ELECTRICAL TEST

VISUAL INSPECTION

O.Q.C. ← OSP

IMMERSION SILVER

IMMERSION TIN

PACKING & SHIPPING

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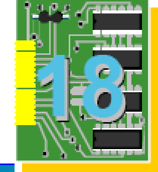
MULTILAYER BOARD WALK

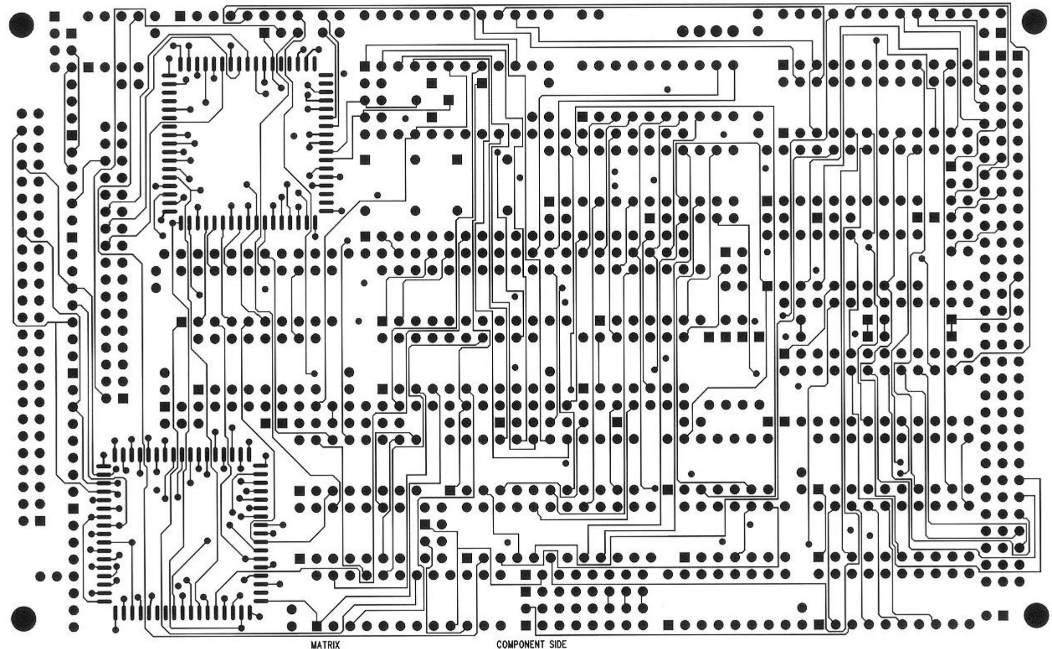


Technical
Training

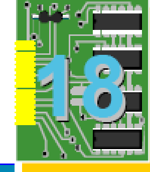
Photo Tools or Artwork

The gerber data or electronic data for the part is used to plot film that depicts the traces and pads of the board's design.

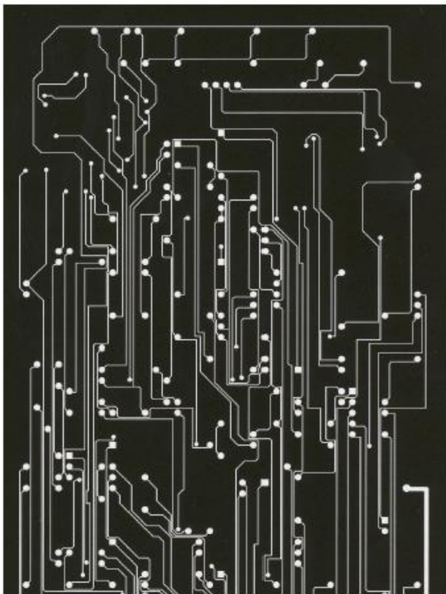
The photo tools or artwork Include solder mask and legend or nomenclature as well as the copper features. This film is used to place an image on the resist.

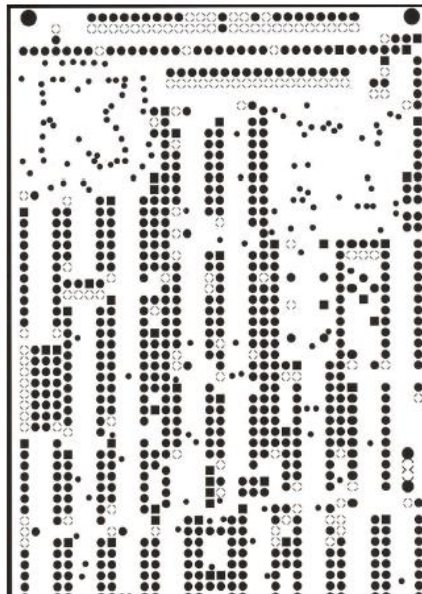


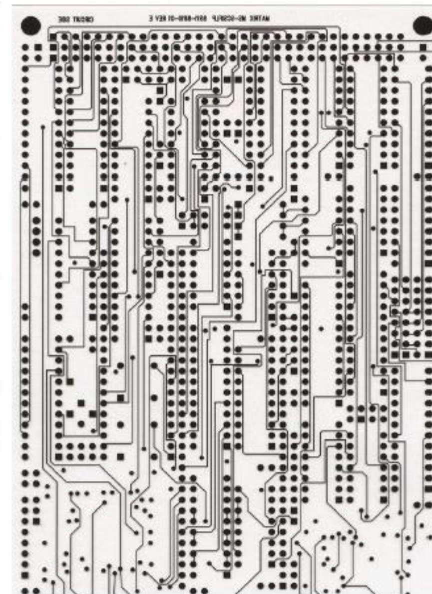
MULTILAYER BOARD WALK



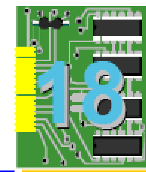
Each of the circuit and land patterns are unique to that part number and each layer has its own artwork pattern or piece of film.
Inner layer film is negative and outer layer film is positive.

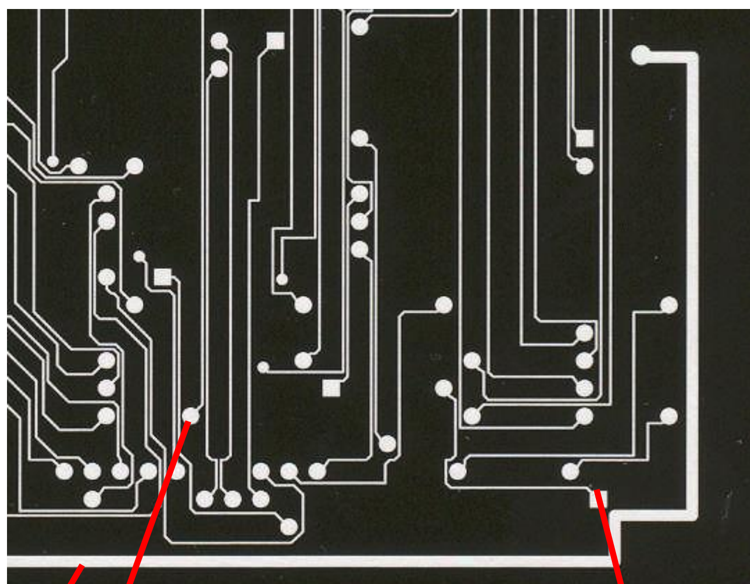




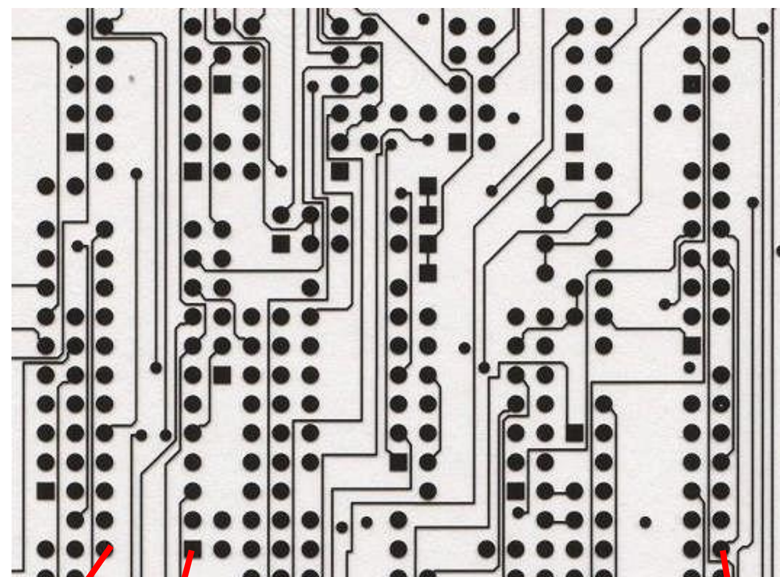


MULTILAYER BOARD WALK



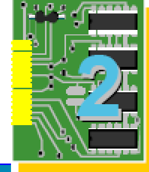


Inner layer film is “negative”. That means that the copper patterns left behind after processing the core are the “clear”areas on the film.



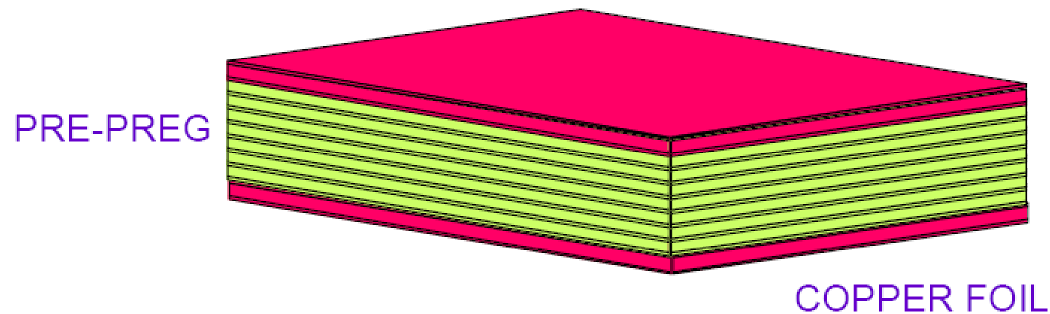
Outer layer film is “positive”. The traces and pads that are “opaque”on the film are copper on the outside of the board and the clear areas will be clear of copper.

RIGID LAMINATE IS MADE



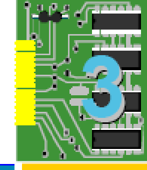
- Prepreg and Copper foil are bonded together to make the rigid laminate

After Bonding Process

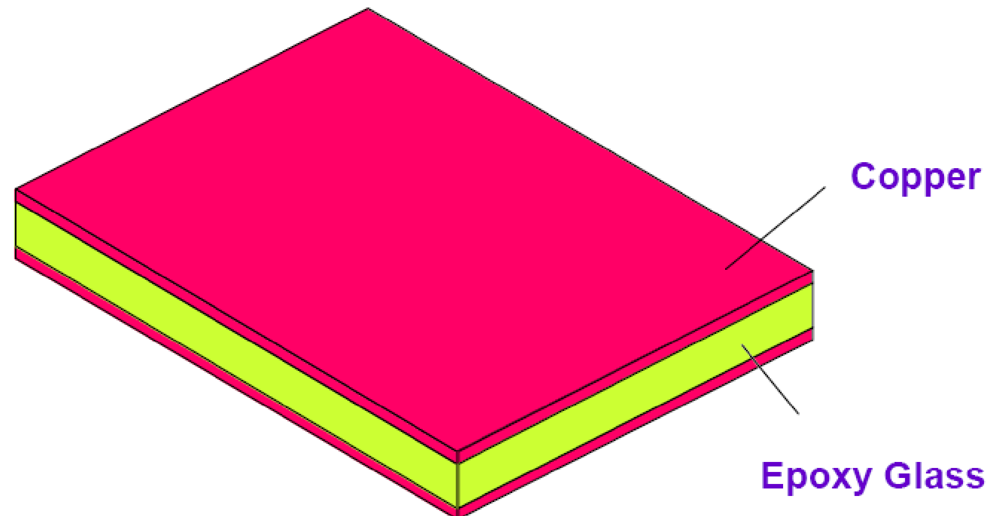


- Lay-up - Bonding - Trimming - Cut into panels ⇨

CUT INTO PANELS



- The Copper-clad epoxy glass (or similar) laminate is cut into panels ready for drilling.



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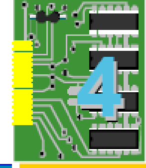
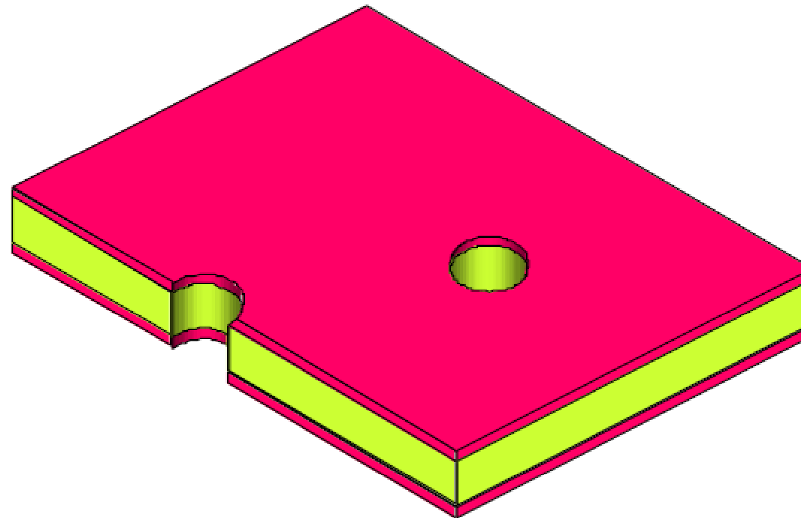
DRILLING



- Holes are drilled into the laminate.

  - When plated, the Holes will serve as a connection between the two sides of the board (PTH).

  - Other holes are for component mounting or board fixing.



- Boards stacked with entry/exit materials - Drilling - Deburring - Desmear - Electroless Copper plating ⇨

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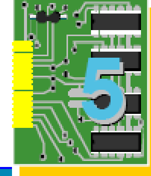
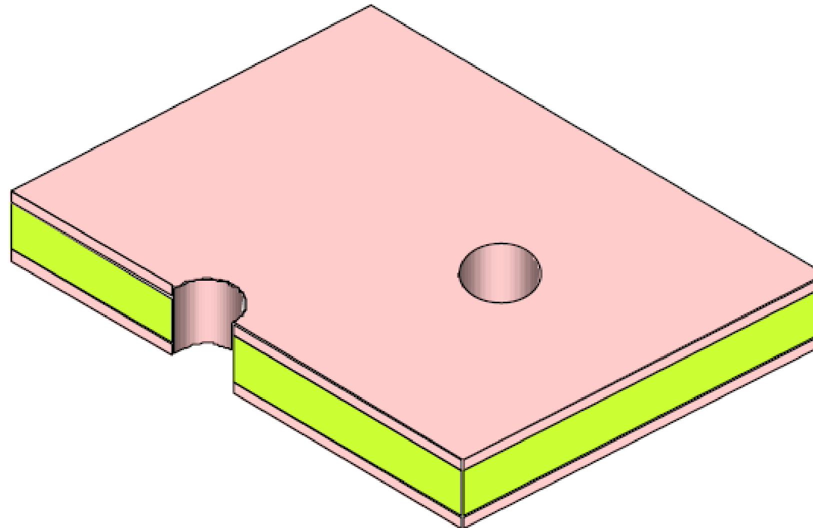
ELECTROLESS COPPER

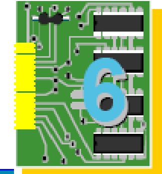


- **Drilled holes are coated with Electroless Copper Plating**

- **A thin deposit of Copper inside the holes provides electrical conductivity for the electroplating processes.**

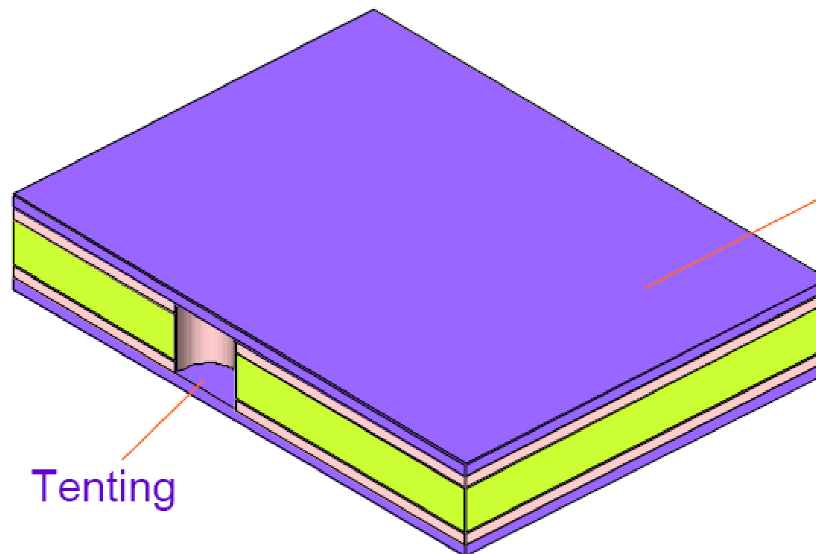


RESIST LAMINATION



- Plating Resist is applied to the boards ready for electroplating

- A light-sensitive Resist is applied to mask the areas of base Copper which do not require plating.



- The plating Resist is slightly thicker than the desired plating deposit.

Printing a circuit image onto the resist from artwork ⇨

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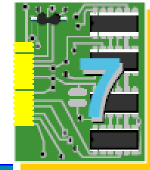
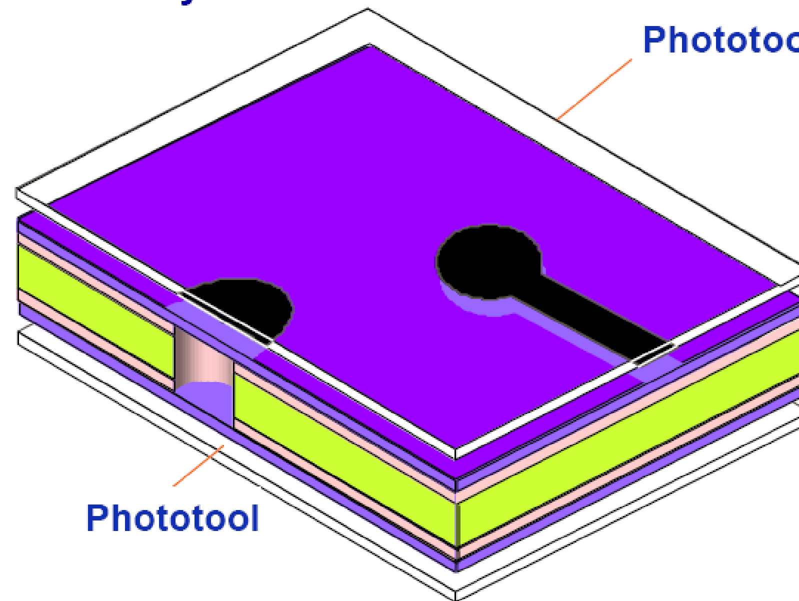
PRINTING



- An artwork which has the circuit Image (in black on phototool) is applied to the board ready for printing



- High intensity ultra-violet light passes through the clear areas of the artwork and hardens the Resist.

- U/v exposure - Polymersation - Developing ⇨

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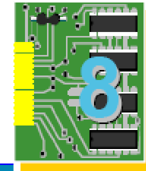
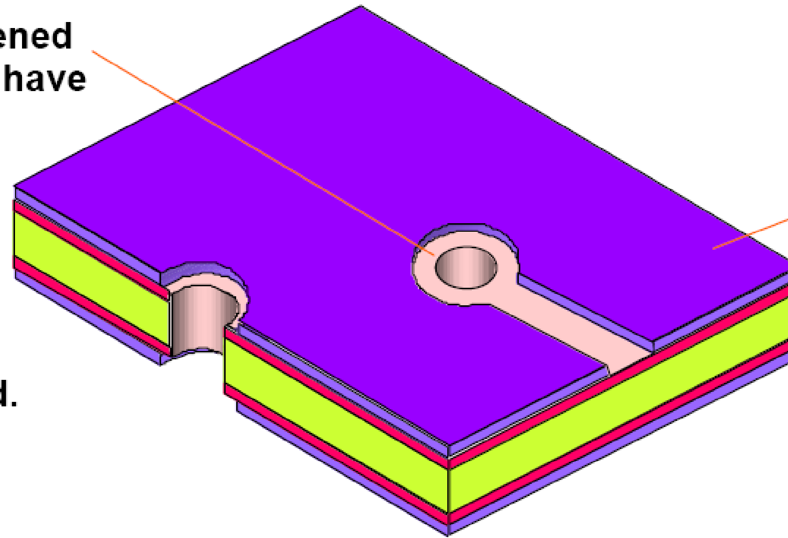
DEVELOPING



Technical
Training

- The boards are developed to reveal the Base Copper to be pattern plated

- The non light-hardened areas of the Resist have remained soft and become dissolved into the developing solution revealing the Copper to be plated.



Photoresist

- U/V light has penetrated the clear parts of the artwork and hardened the Resist

- The light-hardened areas of the Resist remain intact to prevent the unwanted base Copper from being plated.

Developing - Rinse - Dry - Inspection -Pattern Plating ⇨

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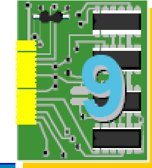
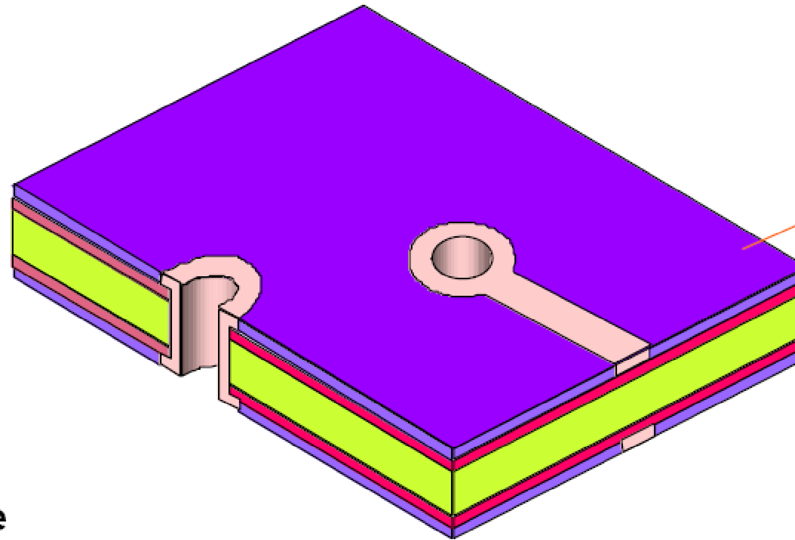
PATTERN PLATING COPPER.



- All of the exposed Copper areas of the board are Electroplated to form the circuit features.

- The holes, already made conductive with Electroless Copper,are plated up to a suitable thickness for carrying current through the finished board.



- The light hardened Resist prevents the unwanted parts of the board from becoming plated

- Acid clean - Microetch - Copper plate - Tin Lead plate ⇨

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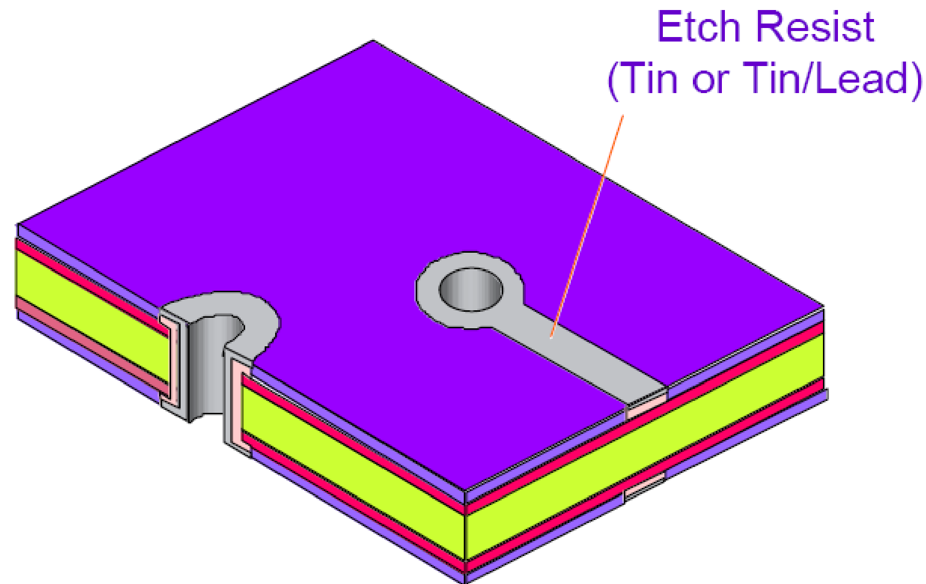
PATTERN PLATING TIN - LEAD

Technical Training

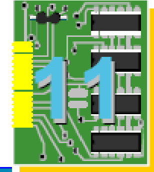
- Electroplate etching resist (Tin Lead)

- Tin Lead is plated onto the Copper plating as a protection during the etching process.

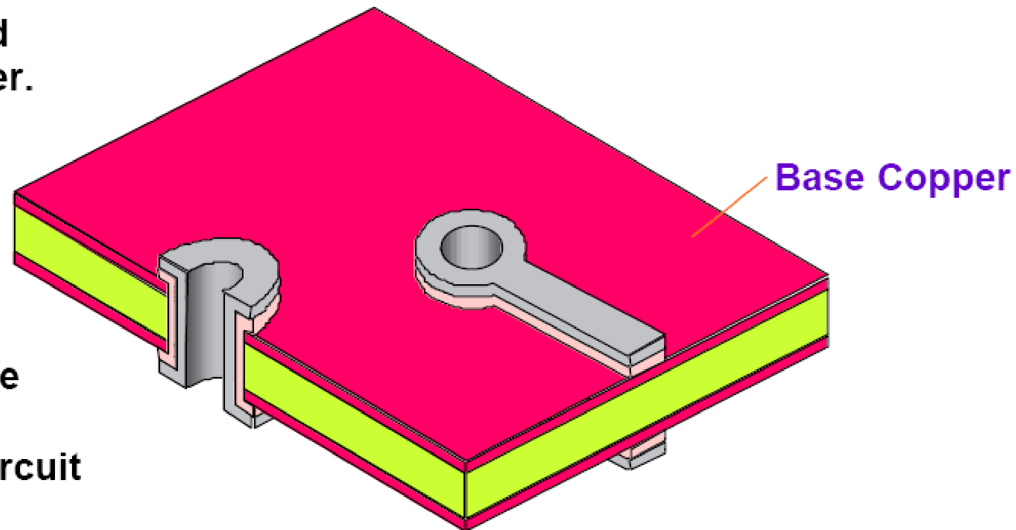


- Tin Lead plate - Dry - Strip Resist ⇨

STRIP RESIST

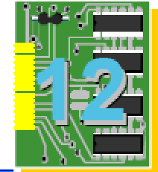


- **The Plating Resist is removed**
- **The circuit features can be seen raised on the base Copper.**
- **Being no longer required, the surplus base Copper can now be removed (etched) leaving only the circuit features protected with Tin Lead remaining as the electrical conductors.**



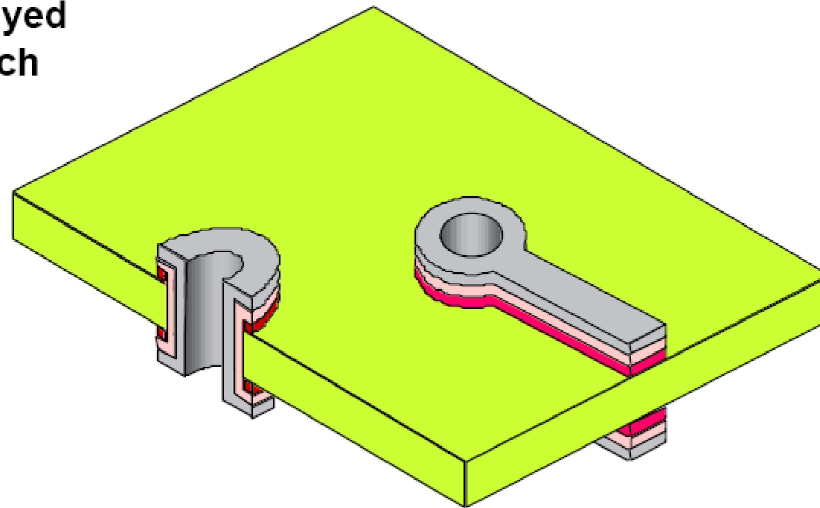
Strip Resist - Rinse - Dry - Etching ⇨

ETCHING



- **Unwanted base Copper is removed during the etching process**

- **Chemicals are sprayed onto the board which dissolve the unprotected base Copper.**



- **The Tin Lead plating has protected the Copper plated circuit features during this operation.**

Etching - Rinse - Dry - Strip Tin Lead ⇨

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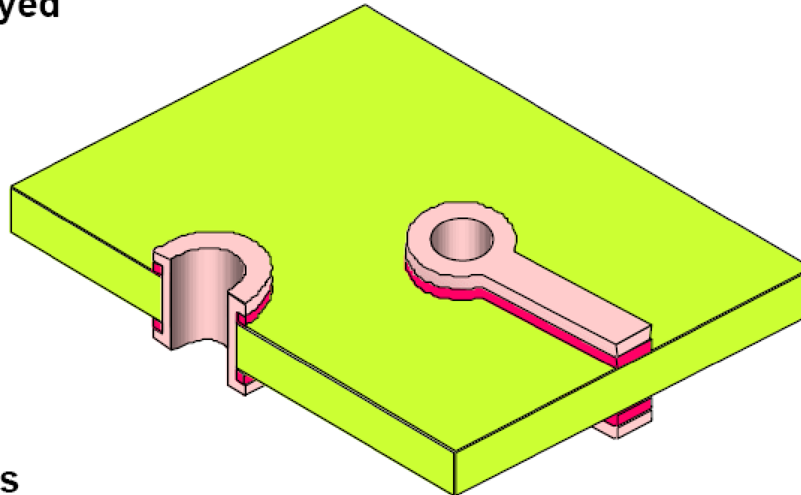
REMOVE TIN- LEAD PLATING

Technical Training

- **Strip etch Resist (Tin Lead)**

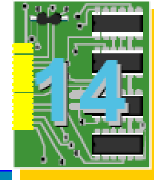
- **A chemical is sprayed onto the boards to dissolve the Tin Lead, which is no longer required.**



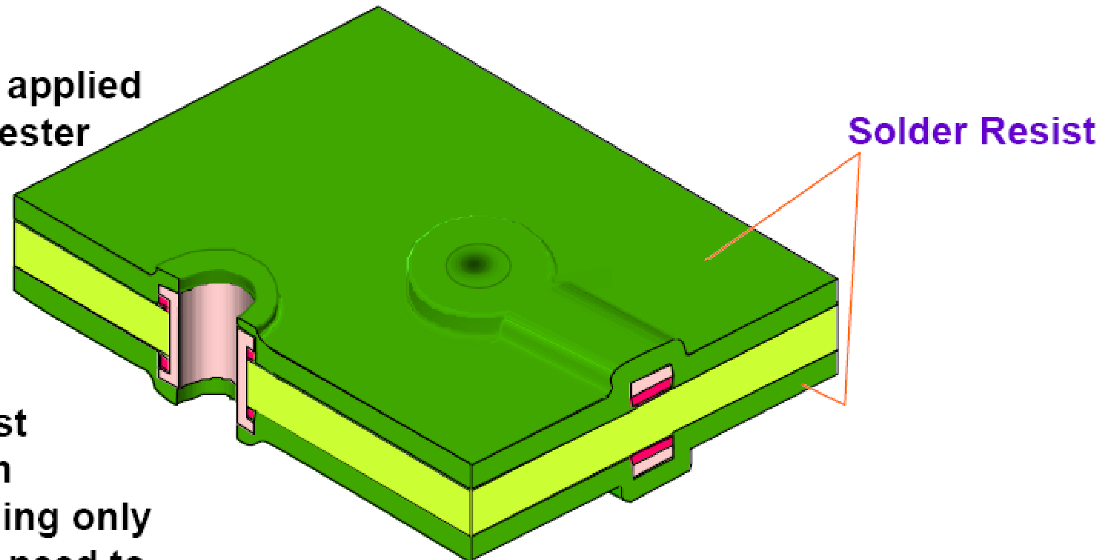
- **After the Tin Lead has been stripped, the Copper remains as the circuit features.**

- Tin Lead strip - rinse - dry - surface preparation - Apply solder Resist ⇨

APPLY SOLDER RESIST



- **Boards are cleaned and then coated with a photo-imageable solder resist.**
- **The liquid resist is applied using either a polyester mesh screen or curtain coating method**
- **When dry, the resist is then printed with an artwork containing only the features which need to remain exposed (pads etc.).**



- Printing - Developing - Curing - Solderable finish application ⇨

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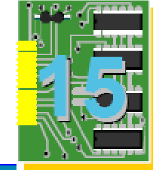
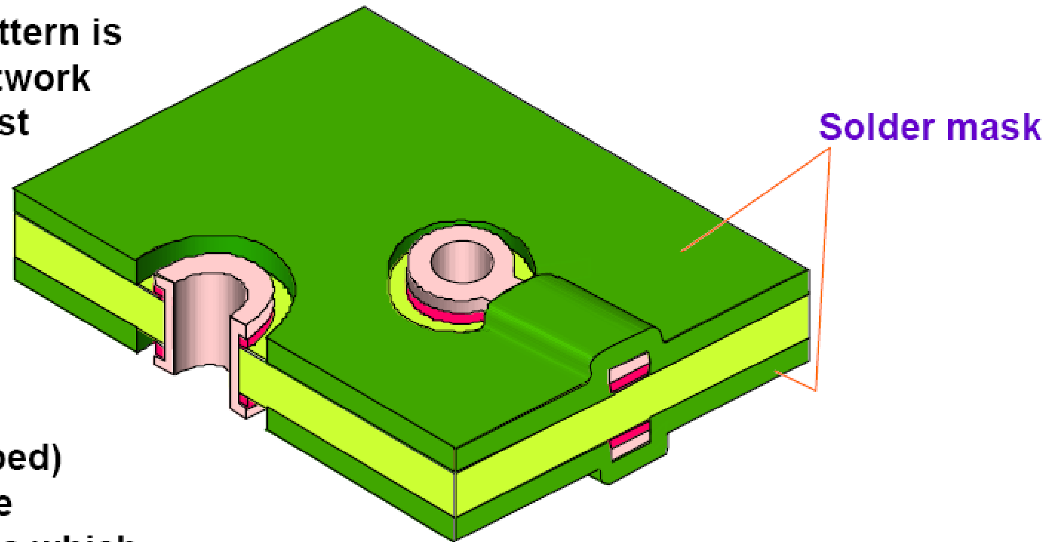
APPLY SOLDER RESIST



- **Using a similar process as for the plating resist (pages 6 to 8), the boards are printed and developed.**

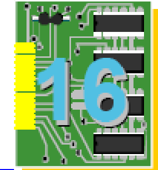
- **After coating, a pattern is printed from an artwork to harden the Resist background and leaving the solder pads area soft.**



- **The non-hardened areas (pads) are dissolved (developed) away to expose the Copper circuit pads which will later receive a suitable finish prior to being soldered by the customer.**

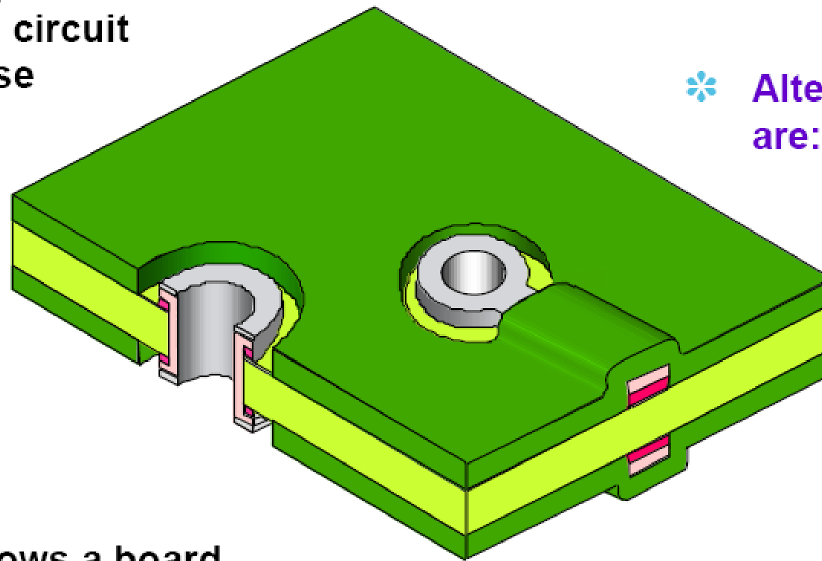
Oven curing - Solderable finish application ⇨

SOLDERABLE FINISH



- A choice of finishes may be applied.

- The solder Resist provides a mask which protects the circuit revealing only those features that require a solderable finish from becoming coated, soldered or plated.



- Alternative finishes are:
  - OSP
  - immersion ni/au
  - Immersion Tin
  - Silver
  - HASL

- The illustration shows a board which has been Hot Air Solder Levelled.

Solderable finish - Screenprint Annotation ⇨

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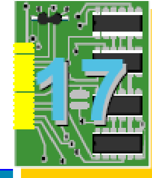
SCREEN PRINTING LEGEND

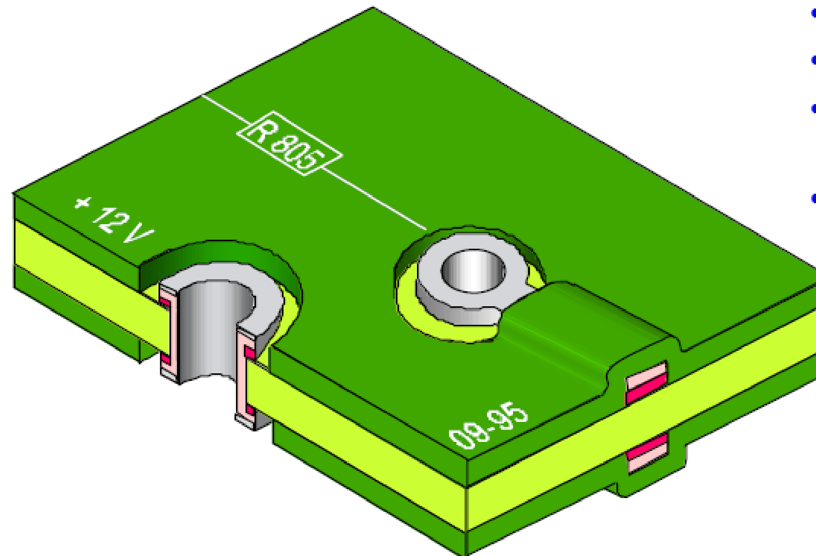


- Alpha-numeric references are screen printed.

➡ Other applications for screen printing include:

- *via plugging*
- *Carbon Printing*
- *Peelable soldermask*
- *Solder resist*

- **A photo-imaged stencil is used on a polyester mesh screen to reproduce an image onto the boards in coloured ink**



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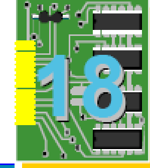
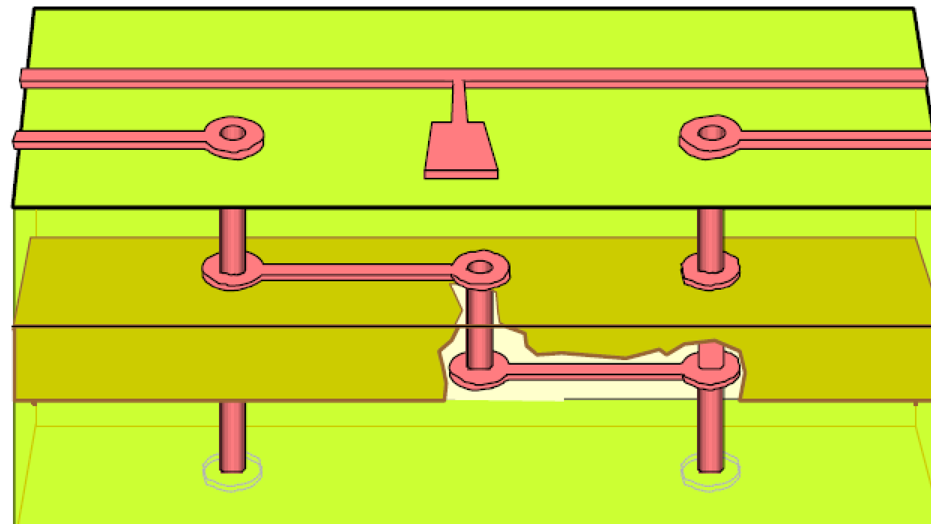
MULTILAYER BOARD WALK



- Due to miniaturisation and a higher complexity and density, the circuit route (tracking) is more diverse and has to pass between several layers of circuitry, which have been bonded together and inter-connected to each other via the plated through holes.

- Multilayer with a buried via inner layer to reduce overall size of the board



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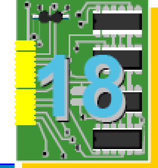
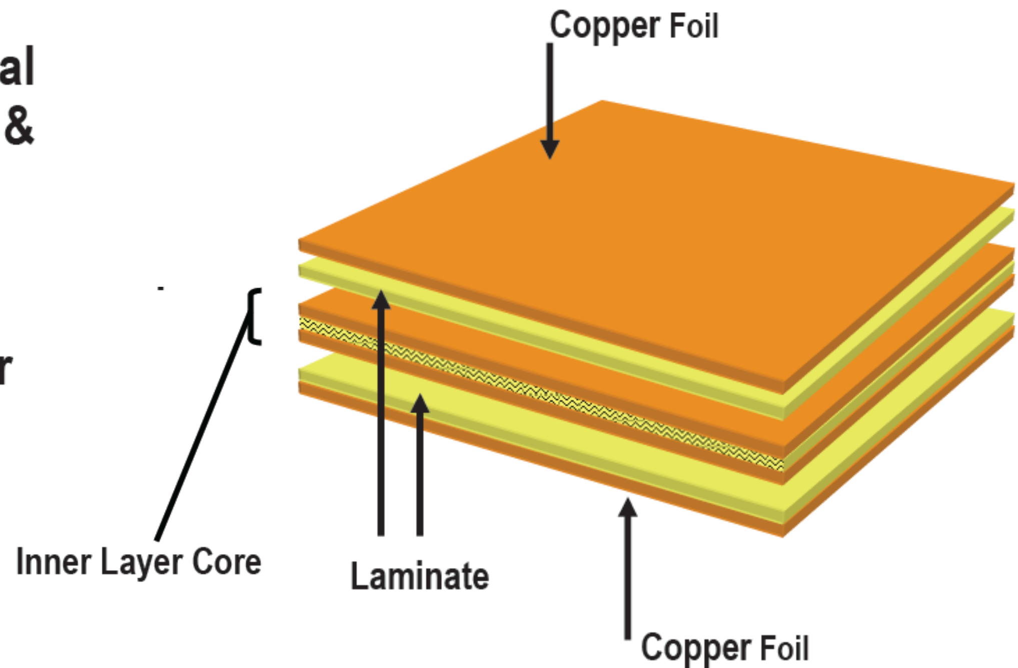
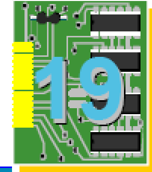
MULTILAYER BOARD WALK



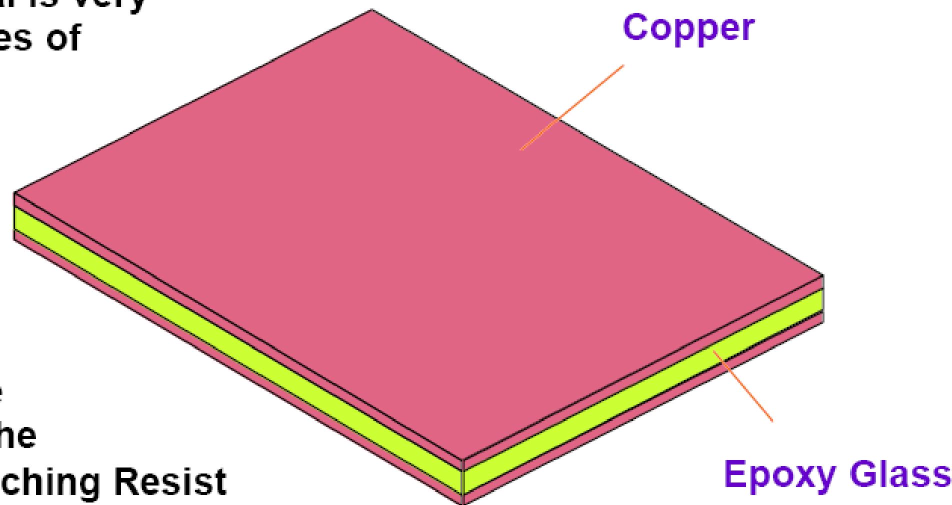
Multi-layer boards are made from the same base material with copper **foil** on the top & bottom and one or more **"inner layer" cores**. The number of "layers" corresponds to the number of copper foil layers.



INNER LAYER PREPARATION



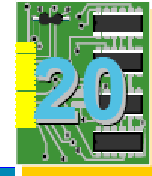
- Inner layer material is cut into panels.
- Inner Layer material is very similar to thin pieces of rigid material as is used for making double sided panels.



- The thin panels are cleaned ready for the application of an etching Resist on which to print a circuit pattern

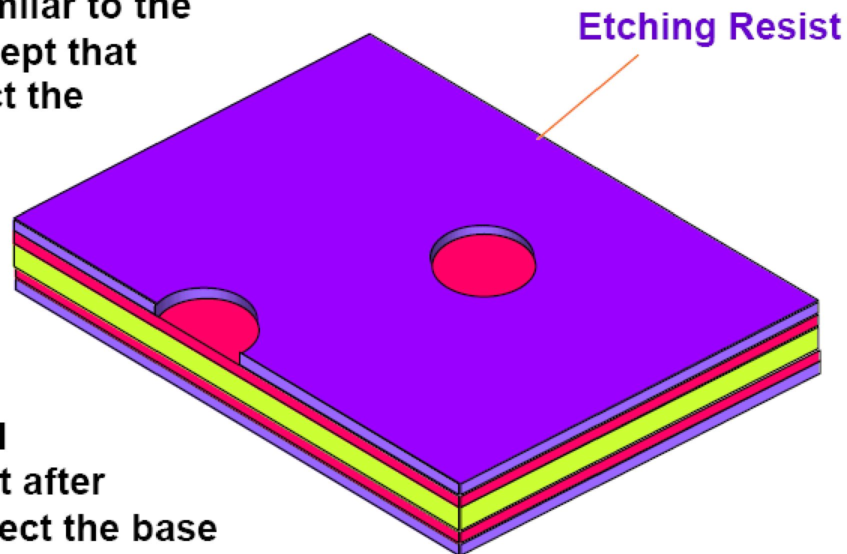
- Remove light soils - remove antitarnish - Coat with an Etching Resist ⇨

ETCHING RESIST



- A light-sensitive etching Resist is applied.

- This process is similar to the plating Resist, except that it is used to protect the base Copper from being etched.
- A negative artwork is used to print the inner layers.
- The light-hardened areas remain intact after developing to protect the base Copper which is not be etched.



Etching - Stripping - Post etch Punch -Adhesion Promoter (Black Oxide or similar)⇨

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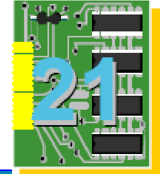
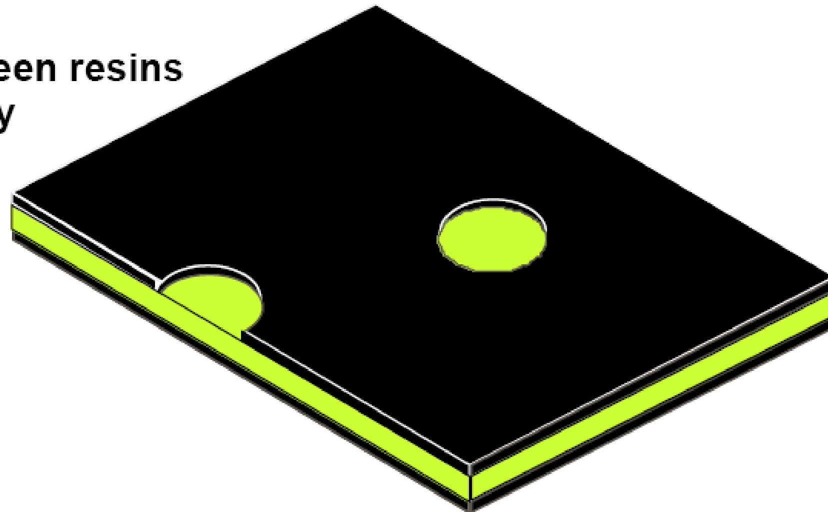
ADHESION PROMOTION



- The Copper is chemically treated to ensure good adhesion during bonding.

- The adhesion between resins and Copper are very low unless the Copper surface has been treated prior to bonding



- The Black Oxide process (or similar) is used to increase the surface roughness of the Copper.

- All materials are then placed together in a stack to be bonded - Lay-up ⇨

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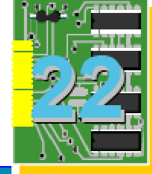
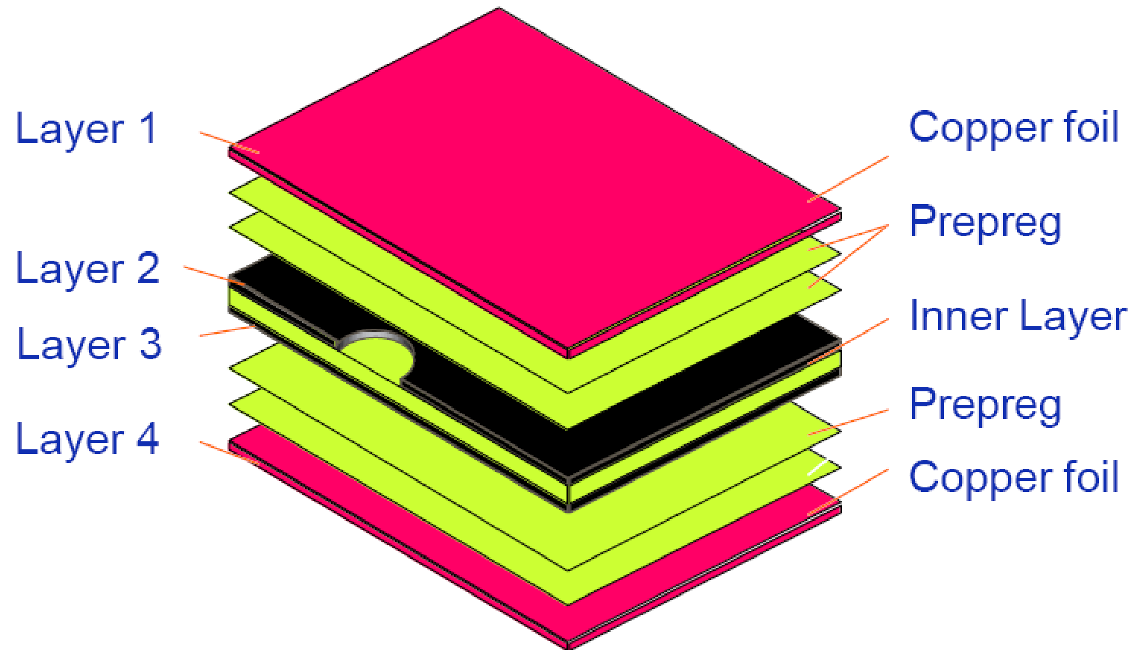
LAY - UP (4 Layer)

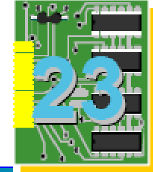


- **Inner Layers and Copper foil are interleaved with pre-preg for bonding together**



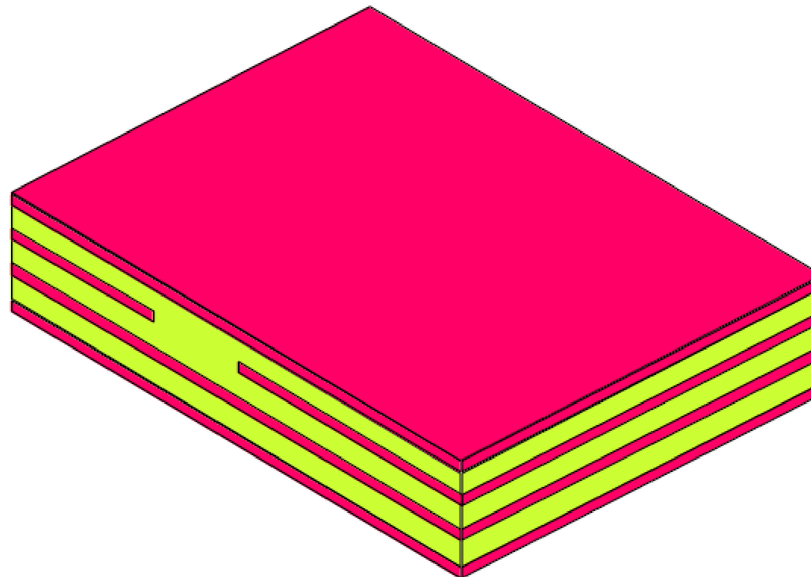
- The layed up stacks are placed into a press for bonding ⇨

BONDING



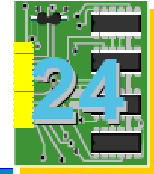
- The materials, layers and foil are bonded together under heat and pressure.

- The semi - cured resin contained within the prepreg melts, and flows before becoming hard and bonding all together as one.

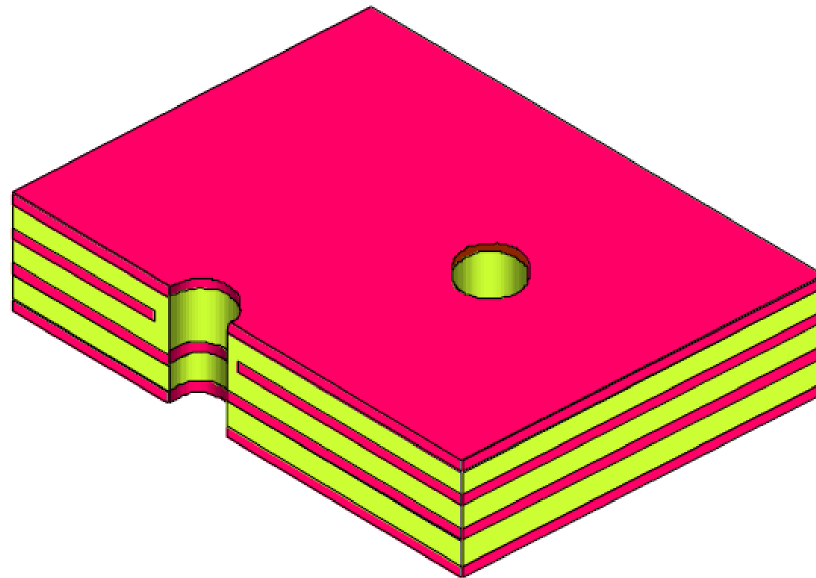


X-Ray Drill Tooling holes - Remove surplus resin from edges - Drilling ⇨

DRILLING



- The bonded panels are drilled, making sure that the inner layer circuit features are drilled centrally.



Deburring Brush - Desmear - Electroless Copper ⇨

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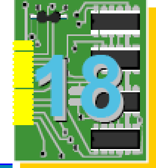
MULTILAYER BOARD WALK

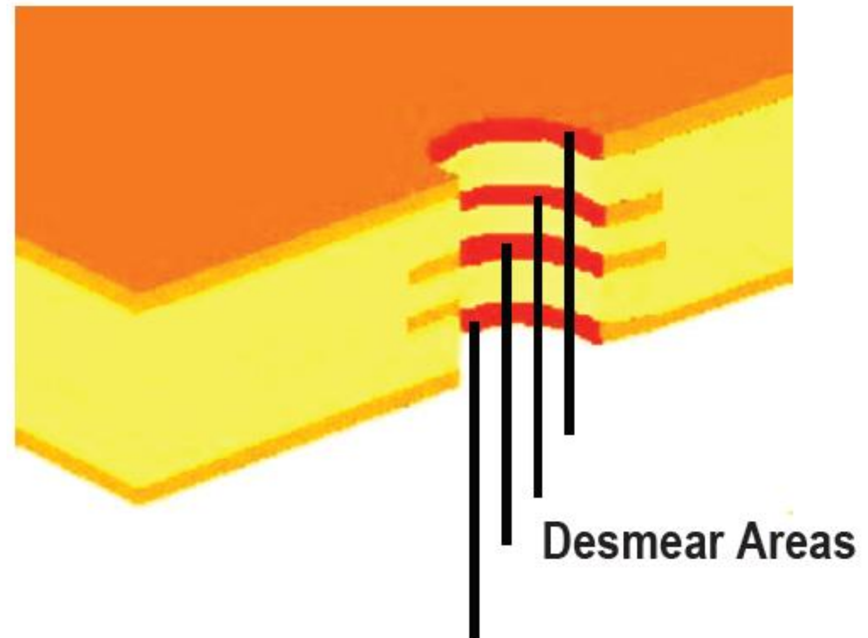


Desmear -

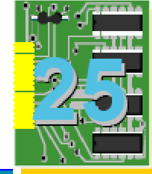
Multi-layer Boards Only

Desmear generally applies only to multilayer boards. It is a chemical process that removes the thin coating of resin from the inner layer connections that is produced by the heat and motion of the drill bits as they create the holes.

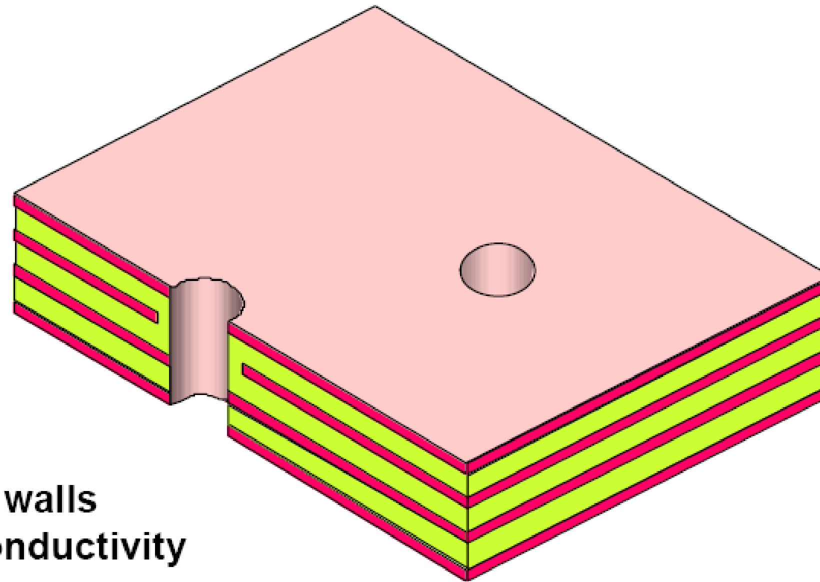
Removing the resin smear improves the electrical connectivity.



ELECTROLESS COPPER



- Electroless copper plating provides the electrical connection between the layers.



- A thin deposit of Copper on internal walls of holes provide conductivity for the electroplating processes.

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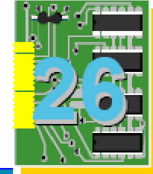
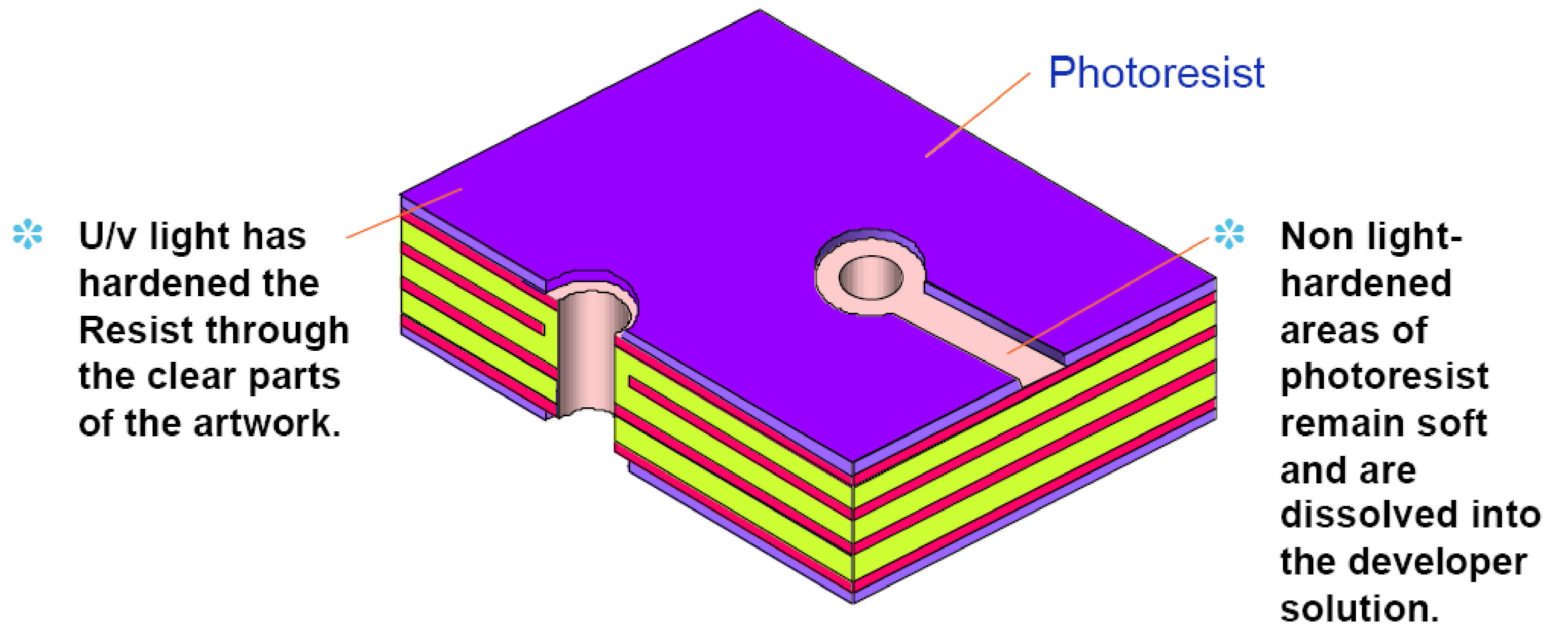
PLATING RESIST



- A plating Resist is applied as a mask to prevent unwanted Copper from becoming plated.



- U/v light has hardened the Resist through the clear parts of the artwork.

- Non light-hardened areas of photoresist remain soft and are dissolved into the developer solution.

- Laminate (50 micron) photoresist - expose - Develop
- Pattern Plating (Electroplating) to build up Copper thickness ⇨

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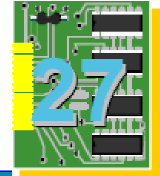
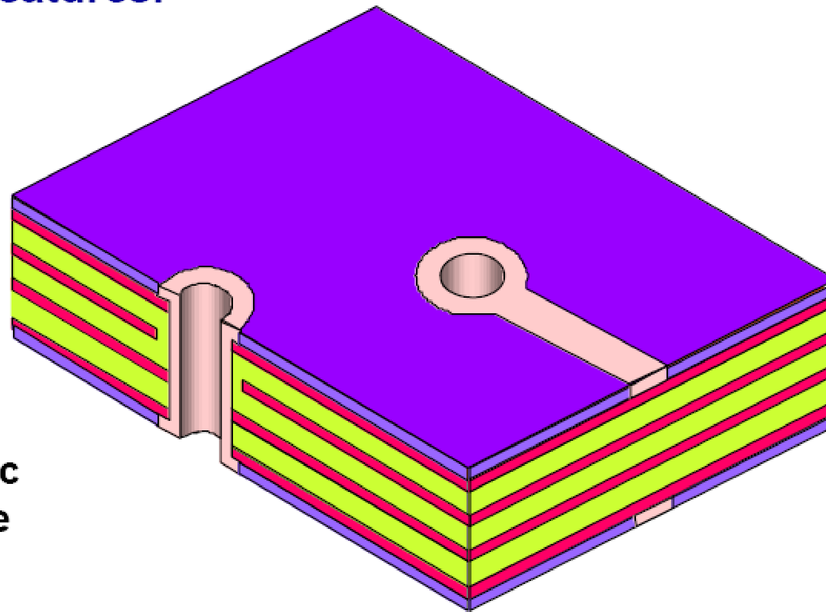
PATTERN PLATING



- All of the exposed areas of the board are Electroplated with Copper to form the circuit features.

- The holes, already made conductive with Electroless Copper, are plated up to a suitable thickness for carrying the electric current through the finished board.



- Acid Clean - Microetch - Copper plate -Tin Lead plate ⇨

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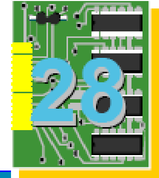
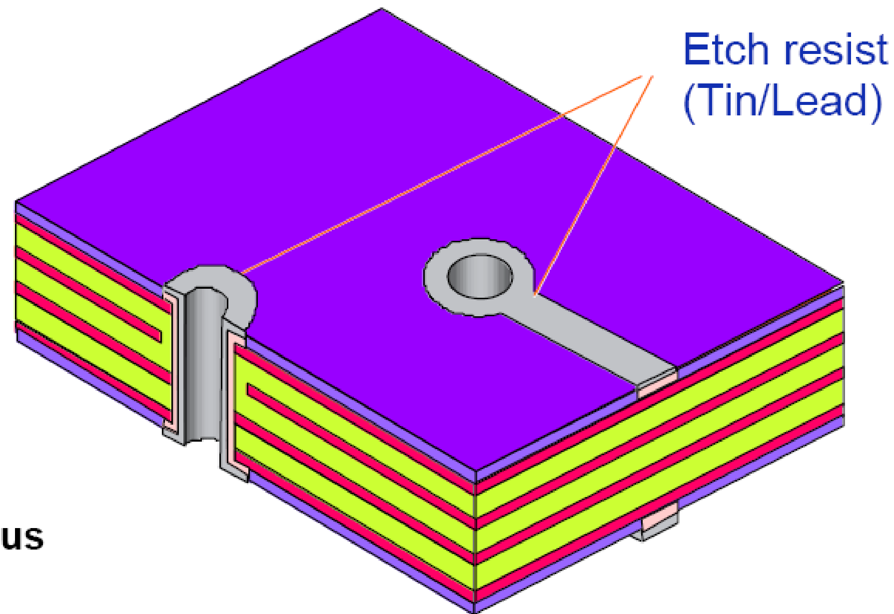
TIN LEAD PLATING



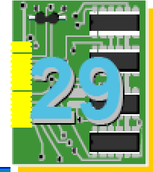
- **Electroplate Tin Lead as an etch Resist**

- **The Tin Lead plating will protect the Copper plated circuit features against the etching chemicals which will be used to dissolve the unwanted surplus base copper.**



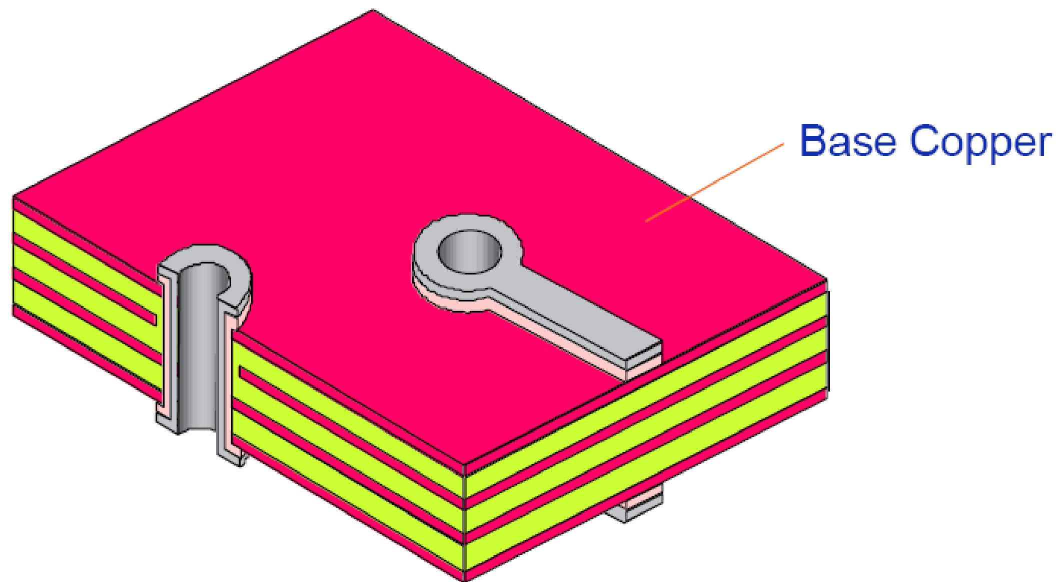
Strip Resist ⇨

STRIP PLATING RESIST



- Strip Photoresist after plating

- **The plating Resist has been removed to reveal the now "surplus" base Copper which is to be removed during the etching process, leaving only the Tin Lead plated circuit features.**



Etching ⇨

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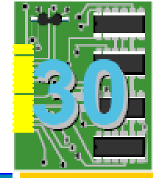
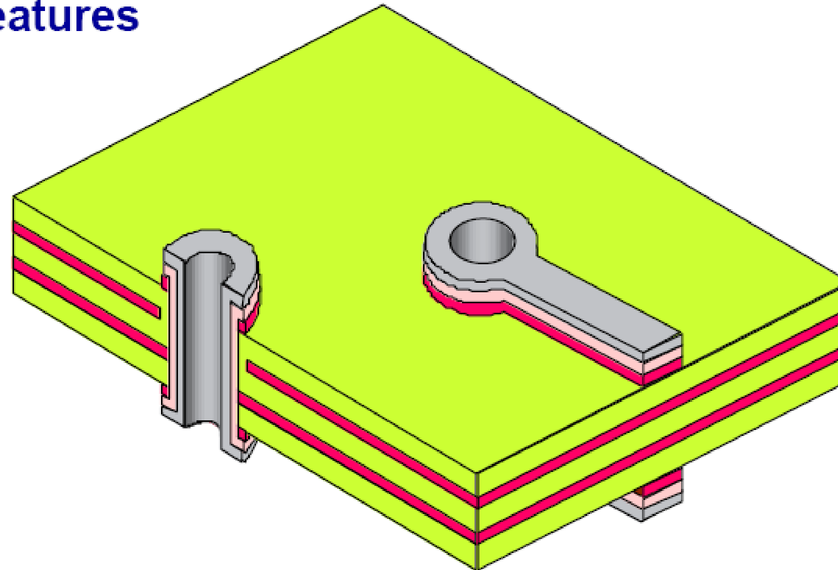
ETCHING



Technical
Training

- The unwanted Copper is now etched away leaving only the circuit features which were protected with Tin Lead.



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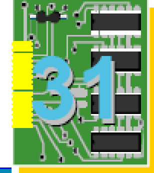
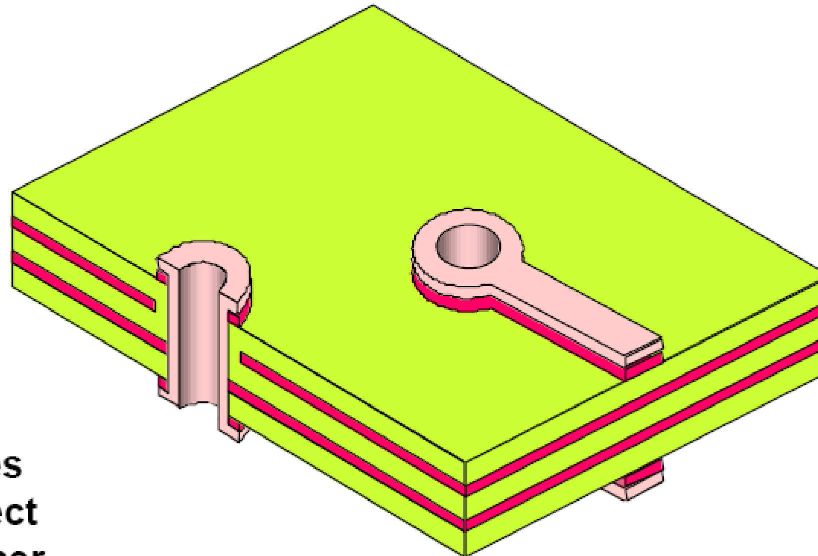
STRIP TIN LEAD



- **Remove Etch Resist leaving the circuit features in Copper**

- **Tin Lead plating is stripped from the circuit features.**



- **You can see how the Copper plating through the holes is used to connect the layers together and so to form the circuit networks.**

Surface preparation and clean ⇨

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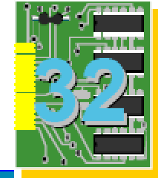
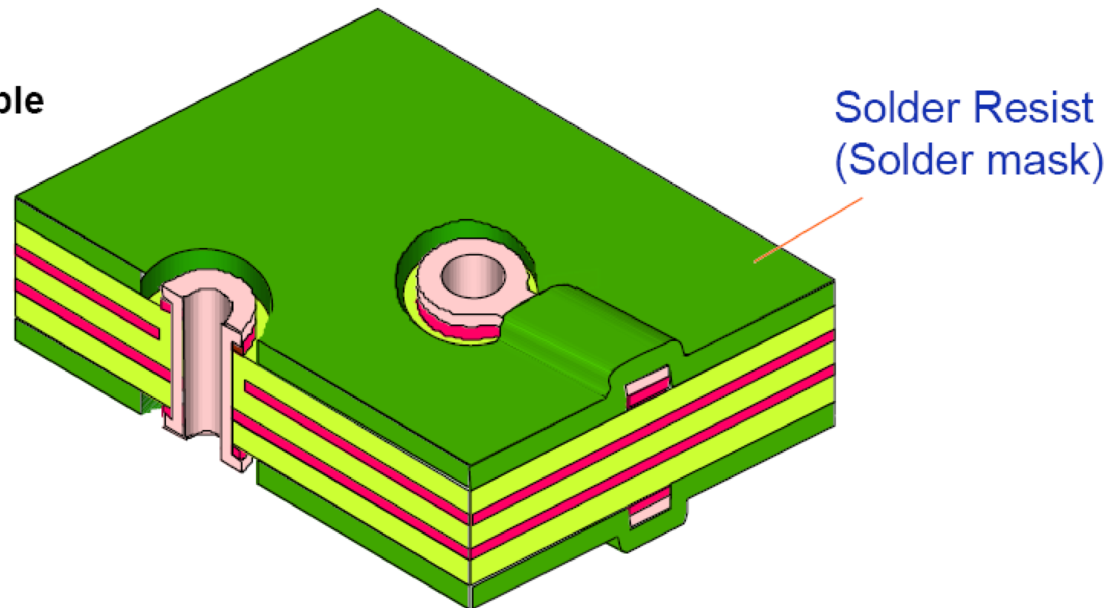
SOLDER RESIST



- **Solder mask (Probimer or similar)**

- **A photo-imageable coating is applied to protect the circuit during the application of soldering finishes and customer soldering**



- Coated - Exposed - Developed - Oven bake to cure - Apply a solderable finish ⇨

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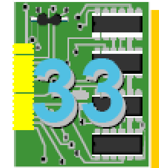
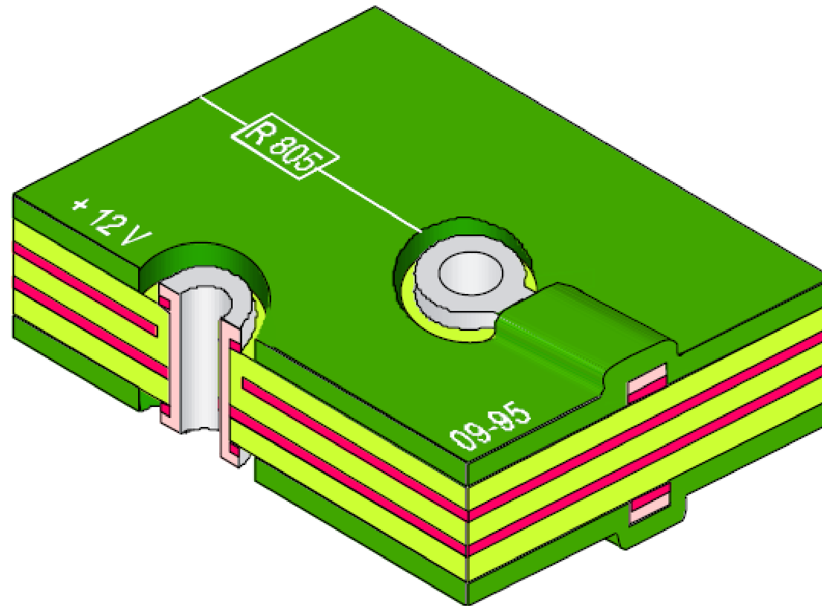
Solderable Finish



Technical
Training

- **A solderable finish is applied to the exposed Copper features and holes**

- **Annotation, and a choice of screen printed features may also be included at this stage**



Routing ⇨

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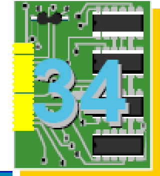
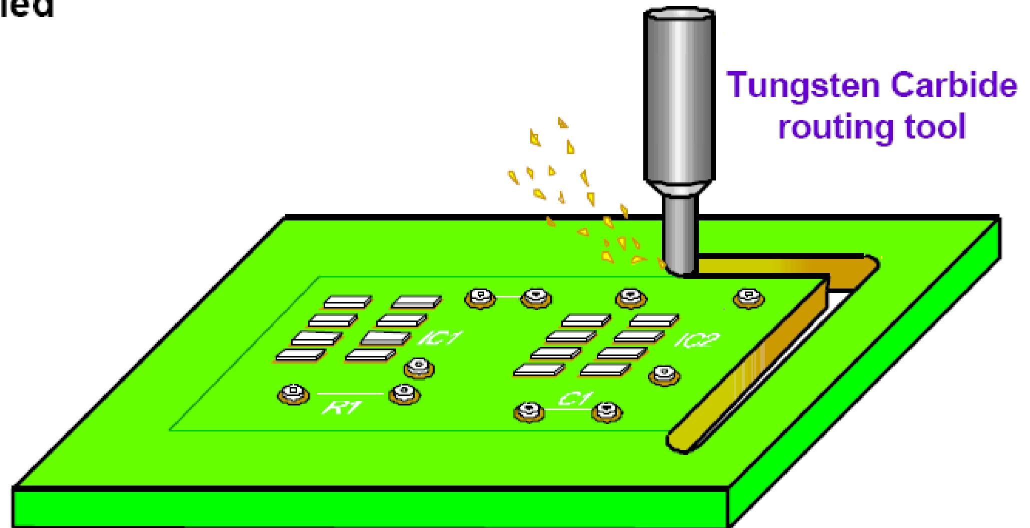
CNC Routing



- After completion of all major processes, the boards are routed to the final shape and size.

- A computer (CNC) controlled routing machine is used to cut individual circuits from the panels.

- A Tungsten Carbide cutter is used to overcome the abrasive nature of the PCB materials.



PCB scoring ⇨

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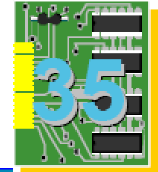
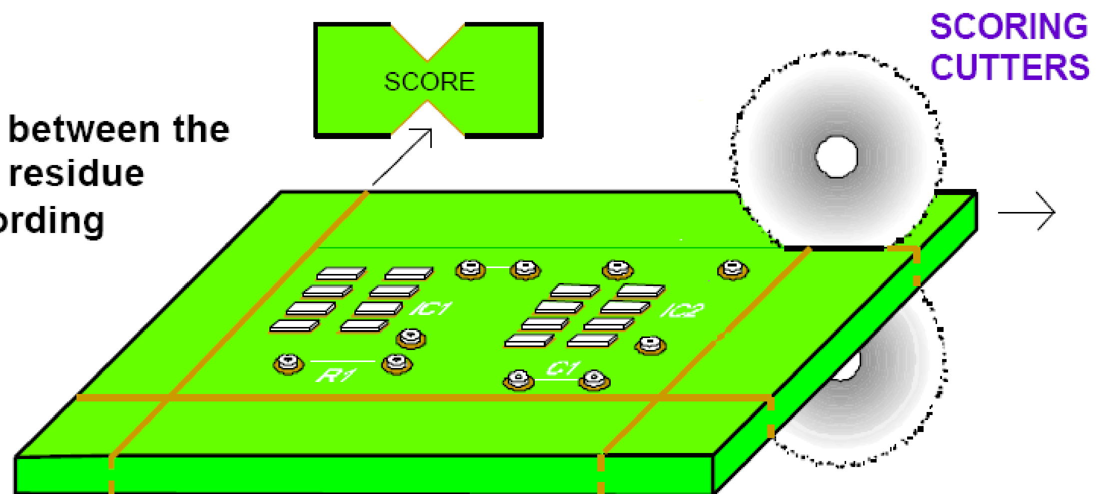
Scoring



- **Panels can be scored on both sides so that they can then be snapped into single circuits after assembly, reducing the handling.**

- **As the panels are passed between two rotating cutter blades which have been ground to a 30° cutting edge, aand a "V" is cut into each side.**
- **After scoring, the material has been weakened such that it can easily be snapped apart into individual circuits.**

- **The material remaining between the scores is known as the residue and may be varied according to the circuit size and customer requirement.**



Electrical testing ⇨

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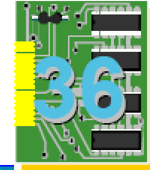
Bare Board Testing



Technical Training

- **Finished boards are tested with a DC voltage to verify the continuity of circuit networks and insulation properties.**

  A choice of methods is used for testing the boards :

- **BED OF NAILS**

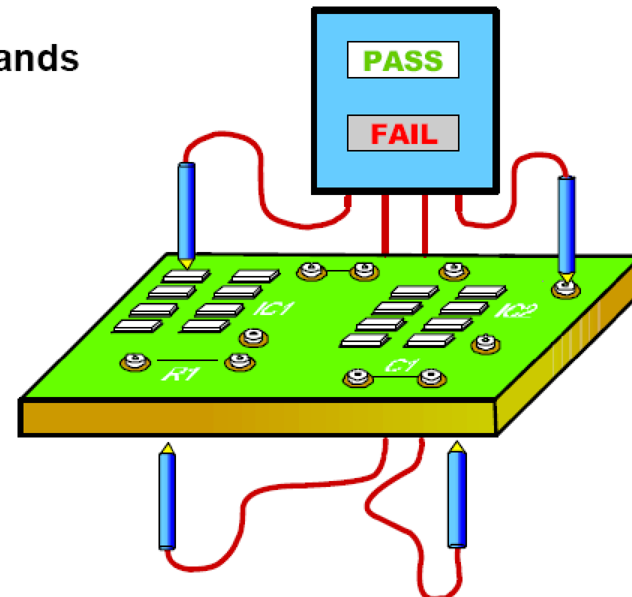
  Dedicated test jigs containing many thousands of pins are used to test the networks simultaneously

  -used for low density/ high volume work

- **FLYING PROBE**

  CNC controlled probes are used to test the networks individually, and therefore alleviate need for test jigs and several stages of testing

  -ideal for high density/fine pitch work



Final inspection and release verification ⇨

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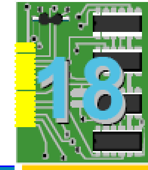
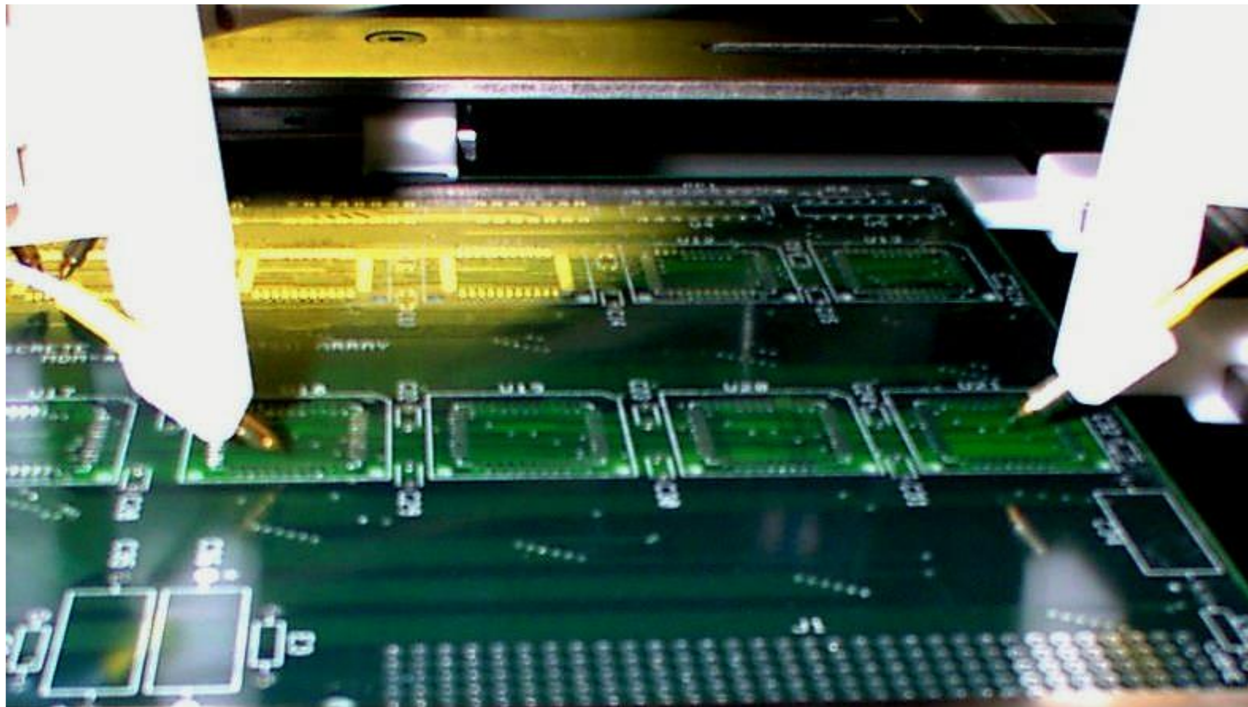
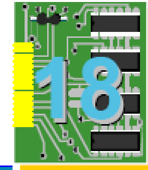
MULTILAYER BOARD WALK



Flying Probe test machine.



MULTILAYER BOARD WALK



Dedicated fixture on a universal grid test machine.

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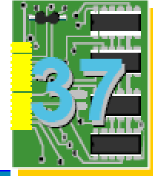
Final Inspection/Release

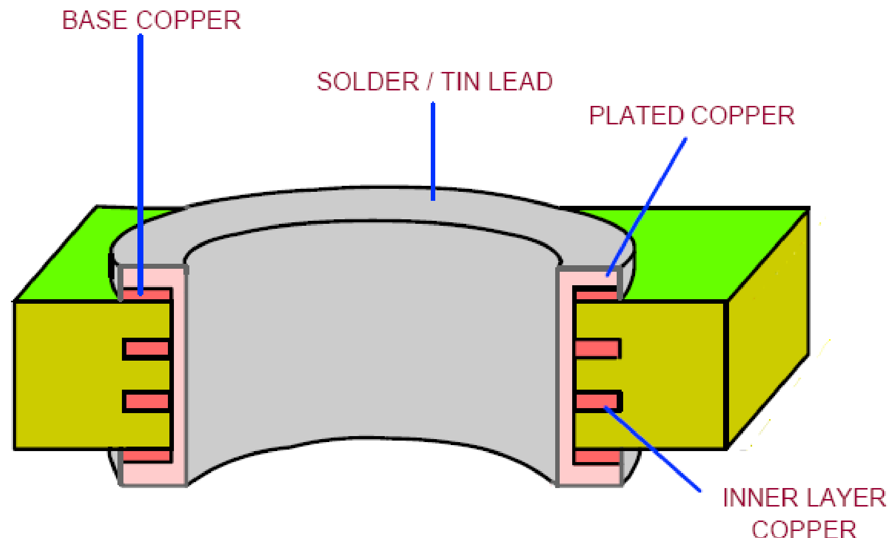


Technical Training

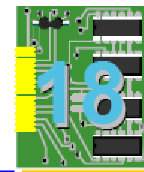
- **The completed PCB's are subjected to a final visual inspection, dimensional verification and release testing.**
- **A sample from the batch is subjected to thermal cycling in a solderbath.**
- **The sample is carefully ground across a plated through hole and then examined under a microscope.**

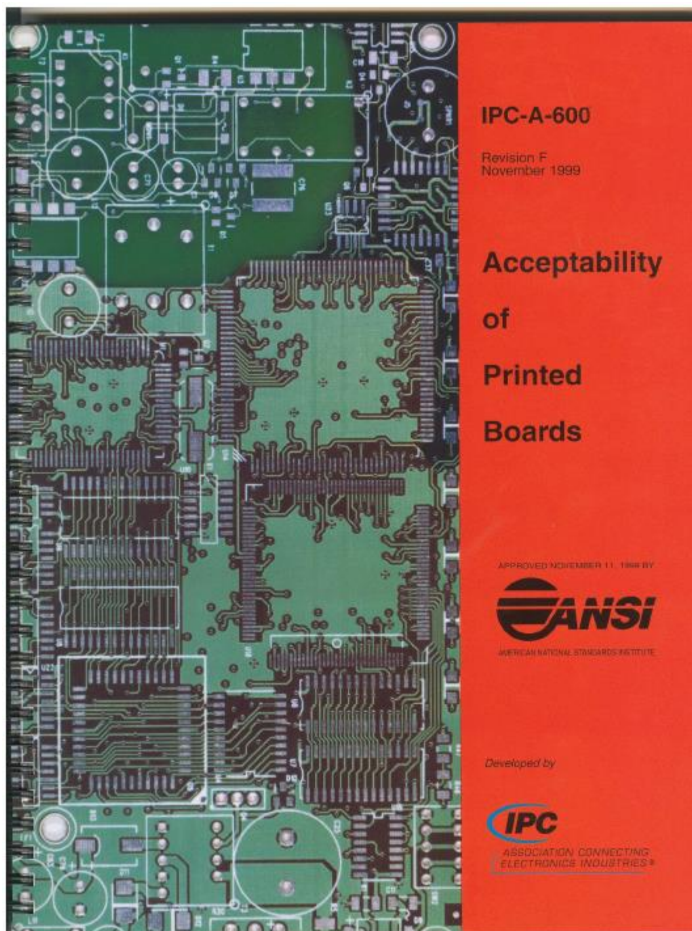
Checks include:

- plating thickness
- pad lift
- hole wall pullaway
- inner layer separation
- cracking
- voids
- outgassing



MULTILAYER BOARD WALK





higher complexity and density, the circuit

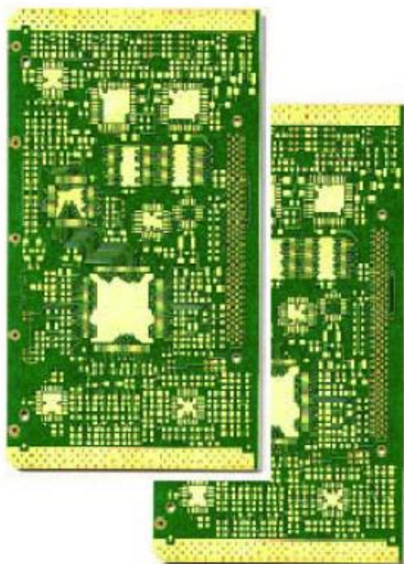
Final Inspection

Boards are visually inspected to assure they me
customers'requirements, industry specification
Advanced Circuits'standards,

as well as having the physical dimensions and l
sizes verified.

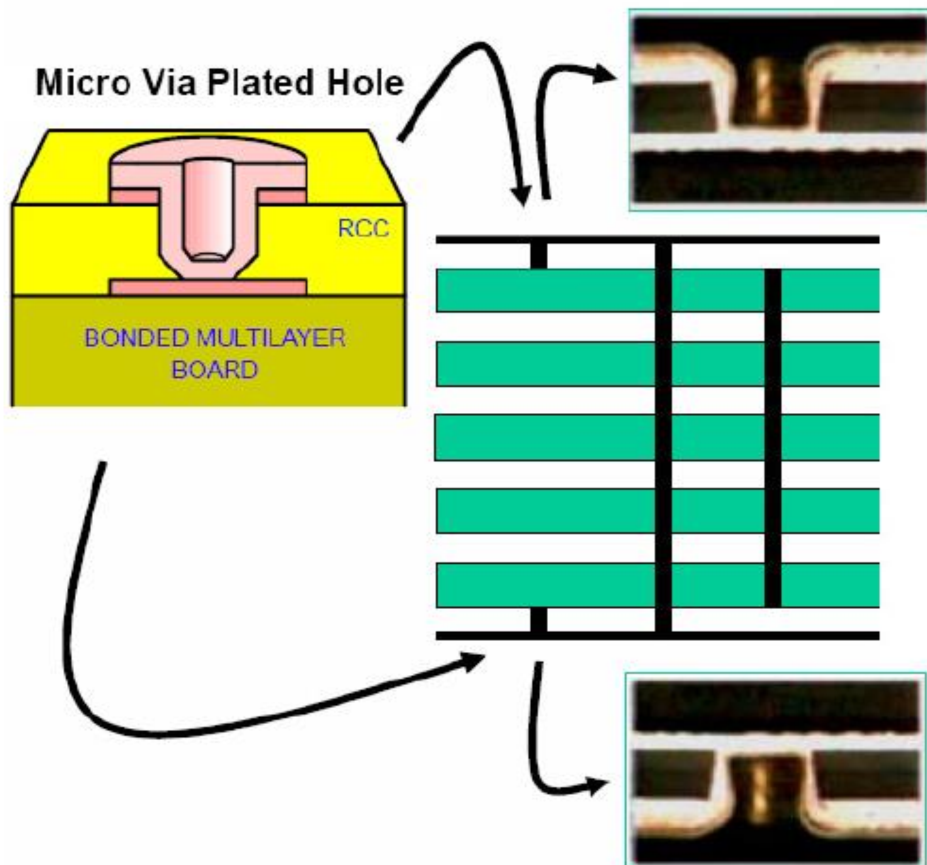
END OF PROCESS

- The finished boards are despatched to the customer



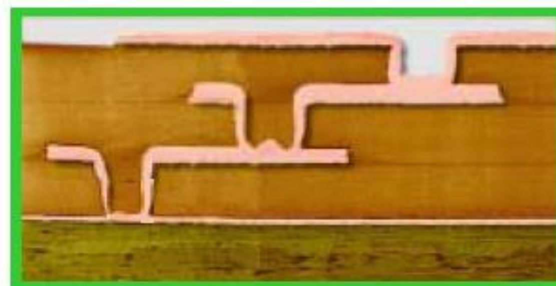
Thanks to

MICRO VIA TECHNOLOGY

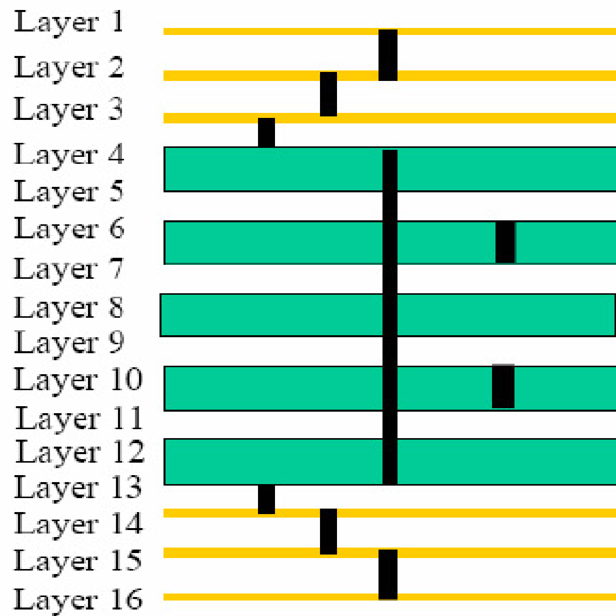


Higher complexity, denser circuitry and miniaturisation forces us to use smaller diameter holes for the interconnection of layers.

Using this technology enhances the success of further miniaturisation of electronic devices with higher I/O connections.



Sequential Microvia Constructions



How Do we construct it ?

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1. Manufacture double sided inner layer cores – Material issue, Coat, Dev, Etch, Strip, AOI, Multibond.

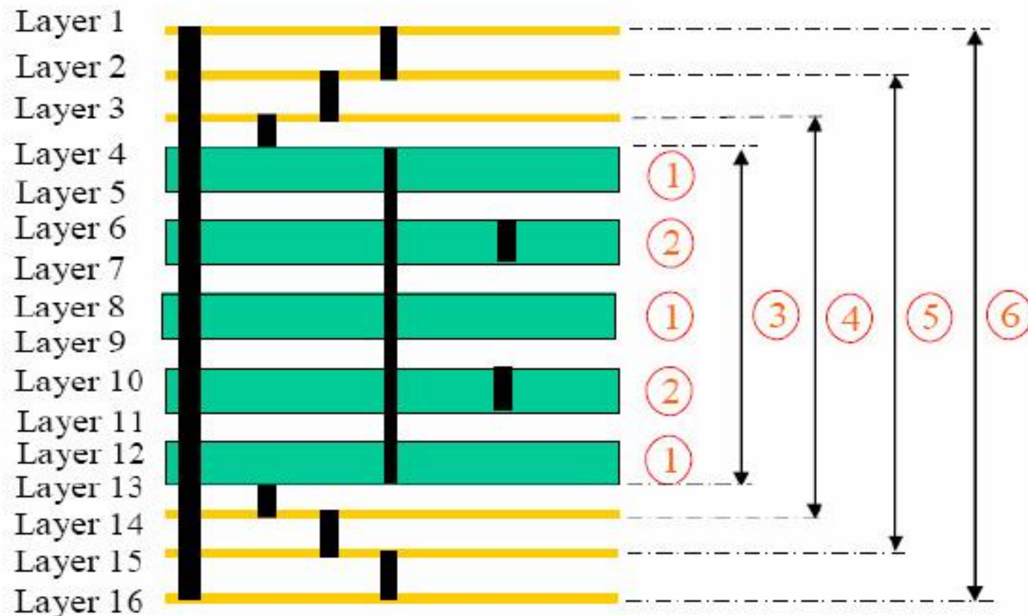
2. Manufacture double sided Buried Via inner layer cores – Material issue, Drill, Electroless, Lam, Exp, Dev, Pattern Plate, strip, Etch, Strip, AOI, Multibond.

3. Bond / Process Sub Assembly L4-13 – **BOND STAGE 1** – Bond, Mechanical Drill, Electroless, Lam, Exp, Dev, Pattern Plate, strip, Etch, Strip, AOI, Multibond.

4. Bond / Process Sub Assembly L3-14 – **BOND STAGE 2** – Bond, Laser Drill, Electroless, Lam, Exp, Dev, Pattern Plate, strip, Etch, Strip, AOI, Multibond.

5. Bond / Process Sub Assembly L2-15 – **BOND STAGE 3** – As per 4. above.

6. Bond / Process L1-16 – **BOND STAGE 4** – Bond, Mechanical Drill, Laser Drill, Electroless, Lam, Exp, Dev, Pattern Plate, strip, Etch, Strip, Apply Soldermask, Apply Legend, Rout, Test, Inspect.



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END OF PROCESS

Technical training

- The finished boards are despatched to the customer

END OF Mini Board Walk