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Fysisk institutt, Universitetet i Oslo

Lille Fysiske Auditorium

10. and 17. Mars 2014

John Steinar Johnsen

Senior Application Engineer

PCB

-Printed Circuit Board-

www.elmatica.com

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Program for 10. and 17. Mars 2014

Time, 12:15 – 14:00 both days.

- Mini BoardWalk, Schematic Simplified Tour of the PCB Manufacturing Processes
- A view on different PCB build up's, EMC considerations, PWR , GND and signals.
- Build in capasitance (BC Core), de-coupling
- Some stuff on PCB Materials, copper structure, glass and epoxy.
  Specify according to IPC 4101C/xxx
- Advanced HDI PCBs, microvia holes, buried vias, stacked and staggered microvia holes, buried holes.
- Design Rules, design aspects, errors seen.
- Introduction to Flexible and FlexRigid PCBs
- Introduction to MBPCB Metal Back PCB's. Aluminium for Power and LED applications.

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A view on different PCB build up's, EMC considerations, PWR , GND and signals

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DESIGN RULES

Layer stack-up (Balanced build):

- In order to review for the balanced build, consider an imaginary line in the middle of the board. This will divide the board into **upper** and **lower** half.

- **The copper layers** in the top half of the board should match with the bottom half of the circuit board.

- **The layer to layer** spacing in the top half of the board should match with the bottom half of the board.

- **The material used** in the upper and lower half of the board should be the same to avoid warpage.

- The stack-up for hybrid circuits should be reviewed by design to design basis.

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4 layer Standard 1.6mm foil build

UNITS: um | ICD STACKUP PLANNER FX – www.icd.com.au | 27/8/2013 | Total Board Thickness: 1539.24 um

Differential Pairs > Pair 1

Layer No.	Via	Description	Layer Name	Material Type	Dielectric Constant	Dielectric Thickness	Copper Thickness	Trace Clearance	Trace Width	Current (Amps)	Characteristic Impedance (Zo)	Edge Coupled Differential (Zdiff)	Broadside Coupled Differential (Zdbs)	Notes
		Soldermask		Dielectric	3.3	12.7								
1	203	Signal	Top	Conductive			35.56	304.8	304.8	0.69	54.44	96.82		
		Prepreg		Dielectric	4.3	203.2								
2		Plane	GND	Conductive			35.56							
		Core		Dielectric	4.3	990.6								
3		Plane	VCC	Conductive			35.56							
		Prepreg		Dielectric	4.3	203.2								
4		Signal	Bottom	Conductive			35.56	304.8	304.8	0.69	54.44	96.82		
		Soldermask		Dielectric	3.3	12.7								

It is common to see four layer boards stacked as above. 2 layer core with 2 foil layers.
That is, four evenly spaced layers with the planes in the centre. Although, this certainly makes the board symmetrical it doesn't help the EMC.

To put the power planes closer in the middle certainly creates good inter plane capacitance, but it doesn't help with signal integrity, crosstalk or EMC

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6 layer Standard 1.6mm foil build

UNITS: um | ICD STACKUP PLANNER FX – www.icd.com.au | 27/8/2013 | Total Board Thickness: 1564.64 um

Differential Pairs > Pair 1

Layer No.	Via	Description	Layer Name	Material Type	Dielectric Constant	Dielectric Thickness	Copper Thickness	Trace Clearance	Trace Width	Current (Amps)	Characteristic Impedance (Zo)	Edge Coupled Differential (Zdiff)	Broadside Coupled Differential (Zdbs)	Notes
		Soldermask		Dielectric	3.3	12.7								
1	200	Signal	Top	Conductive			35.56	203.2	304.8	0.69	54.44	90.52		
		Prepreg		Dielectric	4.3	203.2								
2		Plane	GND	Conductive			35.56							
		Core		Dielectric	4.3	355.6								
3		Signal	Inner 3	Conductive			35.56	203.2	304.8	0.69	55.5	83.94	66.1	
		Prepreg		Dielectric	4.3	304.8								
4		Signal	Inner 4	Conductive			35.56	203.2	304.8	0.69	55.5	83.94	66.1	
		Core		Dielectric	4.3	355.6								
5		Plane	VCC	Conductive			35.56							
		Prepreg		Dielectric	4.3	203.2								
6		Signal	Bottom	Conductive			35.56	203.2	304.8	0.69	54.44	90.52		
		Soldermask		Dielectric	3.3	12.7								

A six layer board is basically a four layer board with two extra signal layers added between the planes.
This improves the EMI dramatically as it provides two buried layers for high-speed signals and two surface layers for routing low speed signals.

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8 layer Standard 1.6mm foil build

UNITS: um | ICD STACKUP PLANNER FX – www.icd.com.au | 27/8/2013 | Total Board Thickness: 1564.64 um

Differential Pairs > Pair 1

Layer No.	Via	Description	Layer Name	Material Type	Dielectric Constant	Dielectric Thickness	Copper Thickness	Trace Clearance	Trace Width	Current (Amps)	Characteristic Impedance (Zo)	Edge Coupled Differential (Zdiff)	Broadside Coupled Differential (Zdbs)	Notes
		Soldermask		Dielectric	3.3	12.7								
1	203	Signal	Top	Conductive			35.56	254	127	0.37	48.55	92.37		
		Prepreg		Dielectric	4.3	76.2								
2		Plane	GND	Conductive			17.78							
		Core		Dielectric	4.3	203.2								
3		Signal	Inner 3	Conductive			17.78	254	127	0.22	54.7	102.59		
		Prepreg		Dielectric	4.3	203.2								
4		Plane	VDD	Conductive			17.78							
		Core		Dielectric	4.3	457.2								
5		Plane	GND	Conductive			17.78							
		Prepreg		Dielectric	4.3	203.2								
6		Signal	Inner 6	Conductive			17.78	254	127	0.22	54.7	102.59		
		Core		Dielectric	4.3	203.2								
7		Plane	VCC	Conductive			17.78							
		Prepreg		Dielectric	4.3	76.2								
8		Signal	Bottom	Conductive			35.56	254	127	0.37	48.55	92.37		
		Soldermask		Dielectric	3.3	12.7								

To improve EMC performance, add two more planes to the six layer stackup.
In the case below, two plane layers are added to the centre of the substrate.
This allows tight coupling between the centre planes and isolates each signal plane reducing coupling hence crosstalk dramatically.
This configuration is commonly used for high speed signals of DDR2 and DDR3 designs where crosstalk due to tight routing is an issue.

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10 layer Standard 1.6mm foil build

UNITS: um | ICD STACKUP PLANNER FX – www.icd.com.au | 27/8/2013 | Total Board Thickness: 1584.96 um

Differential Pairs > Pair 1

Layer No.	Via Span & Hole Diameter	Description	Layer Name	Material Type	Dielectric Constant	Dielectric Thickness	Copper Thickness	Trace Clearance	Trace Width	Current (Amps)	Characteristic Impedance (Zo)	Edge Coupled Differential (Zdiff)	Broadside Coupled Differential (Zdbs)	Notes
		Soldermask		Dielectric	3.3	12.7								
1	203 102 102	Signal	Top	Conductive			35.56	203.2	101.6	0.31	53.9	100.34		
		Prepreg		Dielectric	4.3	76.2								
2		Plane	GND	Conductive			35.56							
		Core		Dielectric	4.3	127								
3		Signal	Inner 3	Conductive			35.56	304.8	101.6	0.31	51.58	97.2	51.07	
		Prepreg		Dielectric	4.3	127								
4		Signal	Inner 4	Conductive			35.56	304.8	101.6	0.31	51.58	97.2	51.07	
		Core		Dielectric	4.3	127								
5		Plane	VDD	Conductive			35.56							
		Prepreg		Dielectric	4.3	457.2								
6		Plane	GND	Conductive			35.56							
		Core		Dielectric	4.3	127								
7		Signal	Inner 7	Conductive			35.56	304.8	101.6	0.31	51.58	97.2	51.07	
		Prepreg		Dielectric	4.3	127								
8		Signal	Inner 8	Conductive			35.56	304.8	101.6	0.31	51.58	97.2	51.07	
		Core		Dielectric	4.3	127								
9		Plane	VCC	Conductive			35.56							
		Prepreg		Dielectric	4.3	76.2								
10		Signal	Bottom	Conductive			35.56	203.2	101.6	0.31	53.9	100.34		
		Soldermask		Dielectric	3.3	12.7								

A ten layer board should be used when six routing layers and four planes are required and EMC is of concern. This stackup is ideal because of the tight coupling of the signal and return planes, the shielding of the high speed signal layers, the existence of multiple ground planes, as well as a tightly coupled power/ground plane.

"Prepared for mVia use"

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12 layer Standard 1.6mm foil build

UNITS: um | ICD STACKUP PLANNER FX – www.icd.com.au | 27/8/2013 | Total Board Thickness: 1559.56 um

Differential Pairs > Pair 1

Layer No.	Via Span & Hole Diameter			Description	Layer Name	Material Type	Dielectric Constant	Dielectric Thickness	Copper Thickness	Trace Clearance	Trace Width	Current (Amps)	Characteristic Impedance (Zo)	Edge Coupled Differential (Zdiff)	Broadside Coupled Differential (Zdbs)	Notes
				Soldermask		Dielectric	3.3	12.7								
1	203	102	102	Signal	Top	Conductive			35.56	203.2	101.6	0.31	53.9	100.34		
				Prepreg		Dielectric	4.3	76.2								
2				Plane	GND	Conductive			35.56							
				Core		Dielectric	4.3	127								
3				Signal	Inner 3	Conductive			35.56	304.8	101.6	0.31	51.58	97.2	51.07	
				Prepreg		Dielectric	4.3	127								
4				Signal	Inner 4	Conductive			35.56	304.8	101.6	0.31	51.58	97.2	51.07	
				Core		Dielectric	4.3	127								
5				Plane	VDD	Conductive			35.56							
				Prepreg		Dielectric	4.3	152.4								
6				Signal	Inner 6	Conductive			35.56	304.8	101.6	0.31	51.43	98.56	72.03	
				Core		Dielectric	4.3	127								
7				Signal	Inner 7	Conductive			35.56	304.8	101.6	0.31	51.43	98.56	72.03	
				Prepreg		Dielectric	4.3	152.4								
8				Plane	GND	Conductive			35.56							
				Core		Dielectric	4.3	127								
9				Signal	Inner 9	Conductive			35.56	304.8	101.6	0.31	51.58	97.2	51.07	
				Prepreg		Dielectric	4.3	127								
10				Signal	Inner 10	Conductive			35.56	304.8	101.6	0.31	51.58	97.2	51.07	
				Core		Dielectric	4.3	127								
11				Plane	VCC	Conductive			35.56							
				Prepreg		Dielectric	4.3	76.2								
12				Signal	Bottom	Conductive			35.56	203.2	101.6	0.31	53.9	100.34		
				Soldermask		Dielectric	3.3	12.7								

The above twelve layer, 2 signal layers are added in the middle, and stackup provides shielding on six of the internal layers. "Prepared for mVia use"

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The fourteen layer stackup below is used when eight routing (signal) layers are required plus special shield of critical nets is required. Layers 6 and 9 provide isolation for sensitive signals while layers 3 & 4 and 11 & 12 provide shielding for high speed signals.

14 layer Standard 1.8mm foil build

UNITS: um | ICD STACKUP PLANNER FX – www.icd.com.au | 27/8/2013 | Total Board Thickness: 1986.28 um

Differential Pairs > Pair 1

Layer No.	Via Span & Hole Diameter	Description	Layer Name	Material Type	Dielectric Constant	Dielectric Thickness	Copper Thickness	Trace Clearance	Trace Width	Current (Amps)	Characteristic Impedance (Zo)	Edge Coupled Differential (Zdiff)	Broadside Coupled Differential (Zdbs)	Notes
		Soldermask		Dielectric	3.3	12.7								
1	203 102 102	Signal	Top	Conductive			35.56	203.2	101.6	0.31	53.9	100.34		
		Prepreg		Dielectric	4.3	76.2								
2		Plane	GND	Conductive			35.56							
		Core		Dielectric	4.3	152.4								
3		Signal	Inner 3	Conductive			35.56	304.8	101.6	0.31	48.42	90.08	7.04	
		Prepreg		Dielectric	4.3	76.2								
4		Signal	Inner 4	Conductive			35.56	304.8	101.6	0.31	48.42	90.08	7.04	
		Core		Dielectric	4.3	152.4								
5		Plane	VDD	Conductive			35.56							
		Prepreg		Dielectric	4.3	177.8								
6		Signal	Inner 6	Conductive			35.56	152.4	101.6	0.31	50.65	87.99		
		Core		Dielectric	4.3	177.8								
7		Plane	VCC	Conductive			35.56							
		Prepreg		Dielectric	4.3	76.2								
8		Plane	GND	Conductive			35.56							
		Core		Dielectric	4.3	177.8								
9		Signal	Inner 9	Conductive			35.56	152.4	101.6	0.31	50.65	87.99		
		Prepreg		Dielectric	4.3	177.8								
10		Plane	VSS	Conductive			35.56							
		Core		Dielectric	4.3	152.4								
11		Signal	Inner 11	Conductive			35.56	304.8	101.6	0.31	48.42	90.08	7.04	
		Prepreg		Dielectric	4.3	76.2								
12		Signal	Inner 12	Conductive			35.56	304.8	101.6	0.31	48.42	90.08	7.04	
		Core		Dielectric	4.3	152.4								
13		Plane	VCC	Conductive			35.56							
		Prepreg		Dielectric	4.3	76.2								
14		Signal	Bottom	Conductive			35.56	203.2	101.6	0.31	53.9	100.34		
		Soldermask		Dielectric	3.3	12.7								

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A sixteen layer PCB provides ten layers of routing and is normally used for very dense designs. Repeated arguments from 14 – 12 layer sstackups.

16 layer Standard 1.8mm foil build

UNITS: um | ICD STACKUP PLANNER FX – www.icd.com.au | 27/8/2013 | Total Board Thickness: 1752.6 um

Differential Pairs > Pair 1

Layer No	Via	Description	Layer Name	Material Type	Dielectric Constant	Dielectric Thickness	Copper Thickness	Trace Clearance	Trace Width	Current (Amps)	Characteristic Impedance (Zo)	Edge Coupled Differential (Zdiff)	Broadside Coupled Differential (Zdbs)	Notes
		Soldermask		Dielectric	3.3	12.7								
1	203	Signal	Top	Conductive			35.56	152.4	101.6	0.31	53.9	96.71		
		Prepreg		Dielectric	4.3	76.2								
2		Plane	GND	Conductive			17.78							
		Core		Dielectric	4.3	127								
3		Signal	Inner 3	Conductive			17.78	203.2	101.6	0.19	53.63	97.88	43.24	
		Prepreg		Dielectric	4.3	76.2								
4		Signal	Inner 4	Conductive			17.78	203.2	101.6	0.19	53.63	97.88	43.24	
		Core		Dielectric	4.3	127								
5		Plane	VDD	Conductive			17.78							
		Prepreg		Dielectric	4.3	127								
6		Signal	Inner 6	Conductive			17.78	254	101.6	0.19	50.99	98.5	59.52	
		Core		Dielectric	4.3	76.2								
7		Signal	Inner 7	Conductive			17.78	254	101.6	0.19	50.99	98.5	59.52	
		Prepreg		Dielectric	4.3	127								
8		Plane	VCC	Conductive			17.78							
		Core		Dielectric	4.3	101.6								
9		Plane	GND	Conductive			17.78							
		Prepreg		Dielectric	4.3	127								
10		Signal	Inner 10	Conductive			17.78	254	101.6	0.19	50.99	98.5	59.52	
		Core		Dielectric	4.3	76.2								
11		Signal	Inner 11	Conductive			17.78	254	101.6	0.19	50.99	98.5	59.52	
		Prepreg		Dielectric	4.3	127								
12		Plane	VSS	Conductive			17.78							
		Core		Dielectric	4.3	127								
13		Signal	Inner 13	Conductive			17.78	203.2	101.6	0.19	53.63	97.88	43.24	
		Prepreg		Dielectric	4.3	76.2								
14		Signal	Inner 14	Conductive			17.78	203.2	101.6	0.19	53.63	97.88	43.24	
		Core		Dielectric	4.3	127								
15		Plane	VCC	Conductive			17.78							
		Prepreg		Dielectric	4.3	76.2								
16		Signal	Bottom	Conductive			35.56	152.4	101.6	0.31	53.9	96.71		
		Soldermask		Dielectric	3.3	12.7								

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A sixteen layer 1.6mm based on only 3 cores. This build is adapted for 5 microvias stacked or staggered. (1-2 / 2-3 / 3-4 / 4-5 / 5-6) and indentical (16----11)

16 layer 1.6mm foil build, microvia via

UNITS: um | ICD STACKUP PLANNER FX – www.icd.com.au | 27/8/2013 | Total Board Thickness: 1569.72 um

Differential Pairs > Pair 1

Layer No	Via Span & Hole Diameter	ion	Layer Name	Material Type	Dielectric Constant	Dielectric Thickness	Copper Thickness	Trace Clearance	Trace Width	Current (Amps)	Characteristic Impedance (Zo)	Edge Coupled Differential (Zdiff)	Broadside Coupled Differential (Zdbs)	Notes	idside Coupled erential (Zdbs)	Notes
		Soldermask		Dielectric	3.3	12.7										
1	203 102 203 203 203 102	Signal	Top	Conductive			35.56	152.4	101.6	0.31	53.9	96.71				
		Prepreg		Dielectric	4.3	76.2										
2		Plane	GND	Conductive			35.56									
		Prepreg		Dielectric	4.3	76.2										
3		Signal	Inner 3	Conductive			35.56	203.2	101.6	0.31	29.55	58.24	43.98		43.98	
		Prepreg		Dielectric	4.3	76.2										
4		Signal	Inner 4	Conductive			35.56	203.2	101.6	0.31	29.55	58.24	43.98		43.98	
		Prepreg		Dielectric	4.3	76.2										
5		Plane	VDD	Conductive			35.56									
		Prepreg		Dielectric	4.3	76.2										
6		Signal	Inner 6	Conductive			17.78	254	101.6	0.19	39.4	77.7	56.38		56.38	
		Core		Dielectric	4.3	76.2										
7		Signal	Inner 7	Conductive			17.78	254	101.6	0.19	48.11	94.06	56.38		56.38	
		Prepreg		Dielectric	4.3	127										
8		Plane	VCC	Conductive			17.78									
		Core		Dielectric	4.3	101.6										
9		Plane	GND	Conductive			17.78									
		Prepreg		Dielectric	4.3	127										
10		Signal	Inner 10	Conductive			17.78	254	101.6	0.19	50.99	98.5	59.52		59.52	
		Core		Dielectric	4.3	76.2										
11		Signal	Inner 11	Conductive			17.78	254	101.6	0.19	50.99	98.5	59.52		59.52	
		Prepreg		Dielectric	4.3	127										
12		Plane	VSS	Conductive			35.56									
		Prepreg		Dielectric	4.3	76.2										
13		Signal	Inner 13	Conductive			35.56	203.2	101.6	0.31	29.55	58.24	43.98		43.98	
		Prepreg		Dielectric	4.3	76.2										
14		Signal	Inner 14	Conductive			35.56	203.2	101.6	0.31	29.55	58.24	43.98		43.98	
		Prepreg		Dielectric	4.3	76.2										
15		Plane	VCC	Conductive			35.56									
		Prepreg		Dielectric	4.3	76.2										
16		Signal	Bottom	Conductive			35.56	152.4	101.6	0.31	53.9	96.71				
		Soldermask		Dielectric	3.3	12.7										


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- Build in capasitance
- (BC Core), de-coupling

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Buried Capacitance®

--BC--

Product Family

will improve your
- **Power Distribution System (PDS)**
- **Noise margin**

and improve
- **EMC levels**.

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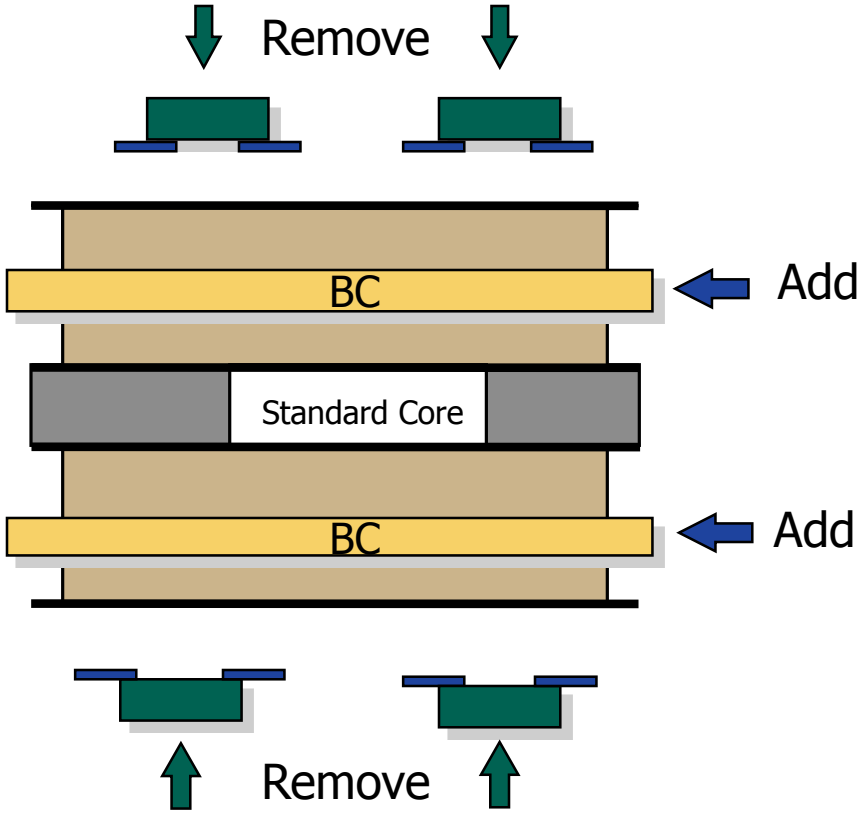
A Very Simple Idea

Use the Power and Ground Planes to Form Buried Capacitance™ (BC) Planes Within the PCB, and Remove Most of the Bypass Capacitors



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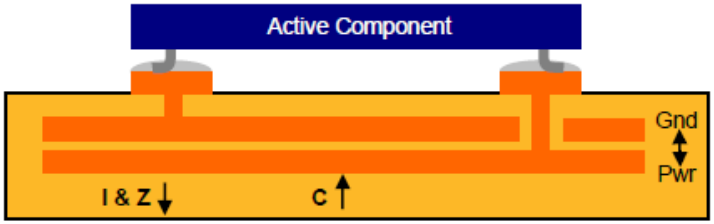
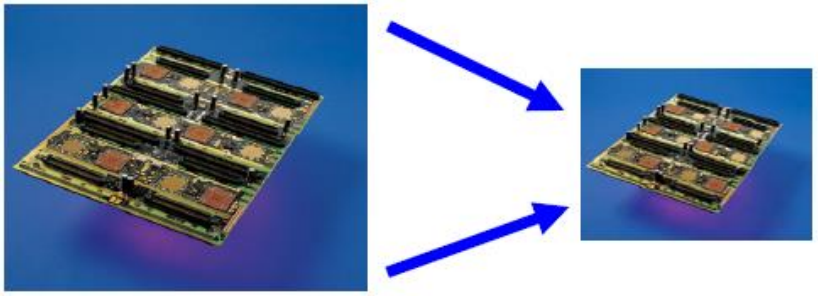
Buried Capacitance ® Drivers

Decrease Plane Inductances &
Broad Band Impedance

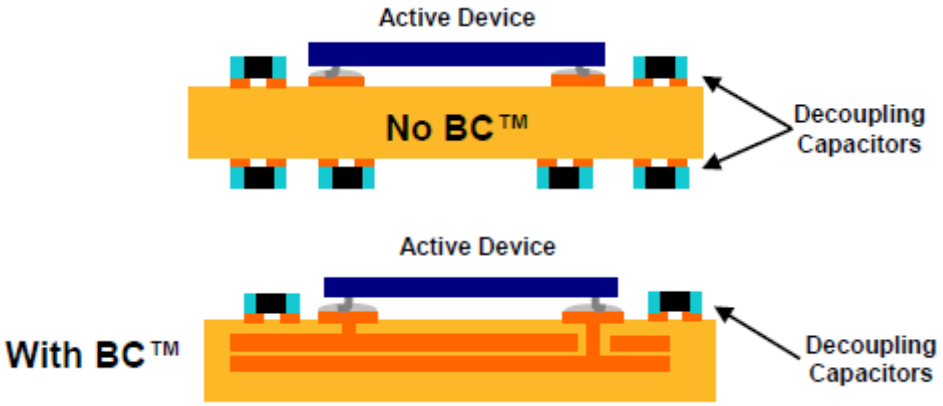


Reduced size or increased functionality
at same size



Lower assembly cost &
higher reliability

- Fewer components= Less solder joints



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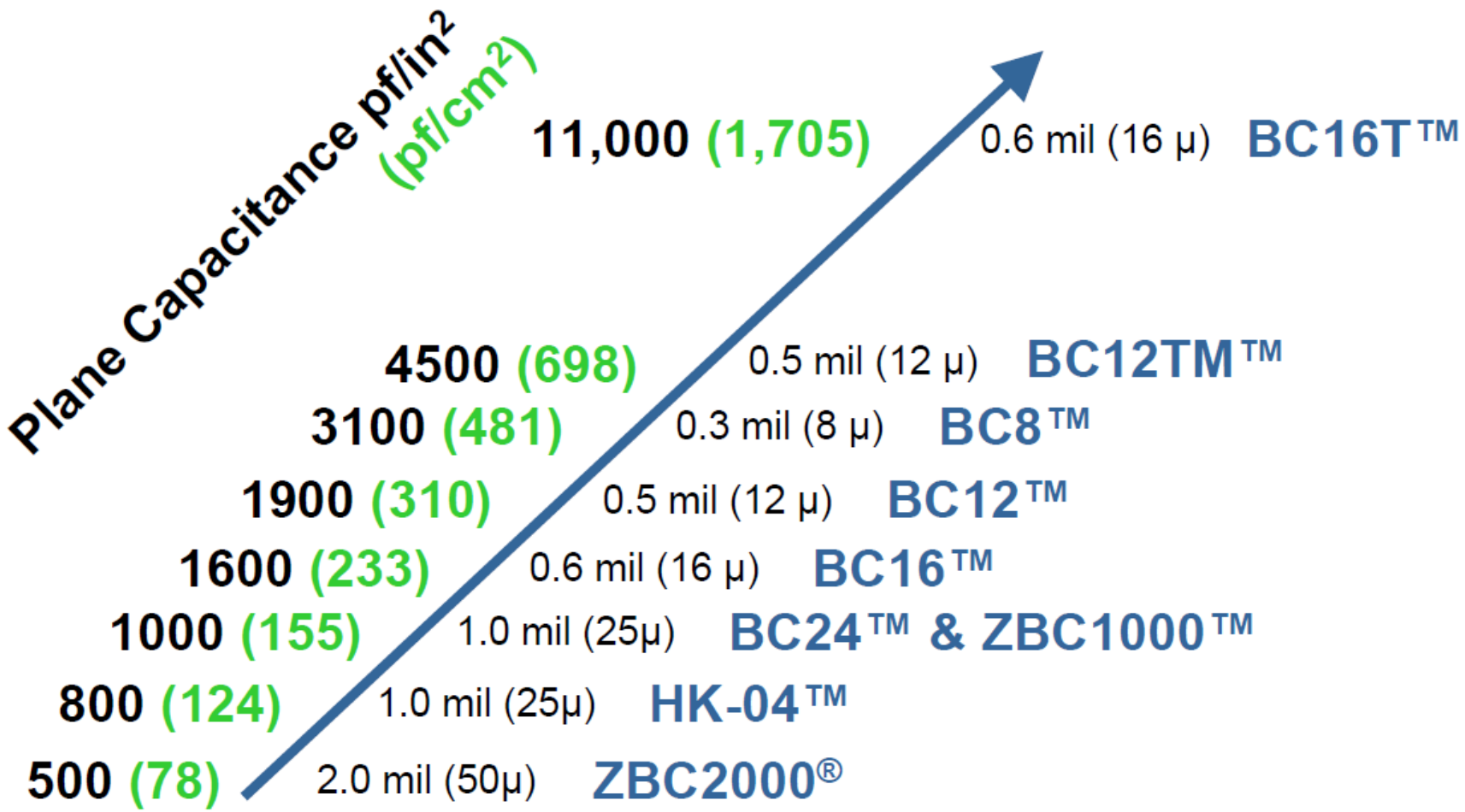
Buried Capacitance® Overview



BC12, BC16, BC8, BC16T, BC12T are all trademarks of Oak Mitsui Technologies
HK-04 is a trademark of DuPont Electronic Materials

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Buried Capacitance® Technical

					FaradFlex™						Interra™
Property	Condition	Unit	ZBC-2000	ZBC-1000	BC-24	BC-16	BC-12	BC-8	BC-12TM	BC-16T	HK-04
Dielectric Thickness	Nominal	Mils (µm)	2.0 (50)	1.0 (25)	0.94 (24)	0.63 (16)	0.47 (12)	0.31 (8)	0.47 (12)	0.63 (16)	25
Dielectric Type	N/A	N/A	FR-4	FR-4	Modified FR-4	Modified FR-4	Modified FR-4	Modified FR-4	Modified FR-4	Modified FR-4	Polyimide
Tg	DSC/ DMA	°C	170	170	200	200	200	200	200	200	195
Capacitance	DC-1 MHz	nf/in.^{2}	0.5	0.9	1.0	1.5	2.0	3.1	4.5	11.0	0.8
Capacitance	DC-1 MHz	pF/cm^2	78	140	155	233	310	481	698	1705	124
Plane self-Inductance	1 GHz	pH	49	38	35	29	23	18	23	29	Pending
Dk	1 MHz	N/A	4.2	4.2	4.6	4.6	4.6	4.4	10	30	3.5
Df	1 MHz	N/A	0.015	0.015	0.015	0.015	0.015	0.016	0.019	0.019	0.003
Peel Strength	As received	lb/in.^{2}	>6.0	>6.0	>8.0	>8.0	>8.0	8.0	6.0	6.0	9
Hi-Pot Test Pass	DC volts	Volts	500	500	500	500	500	500	500	100	500
Dielectric Breakdown	1kV/mil	Volts (DC)	>2.5	>2.5	5.3	7.3	5.0	5.0	6.2	2.8	6-7
UL Rating	N/A	N/A	94-V0	94-V0	94-V0	94-V0	94-V0	94-V0	In progress	In progress	94-V0

High Dk value is positive for the capacitance, will ”not” affect signal- impedance values

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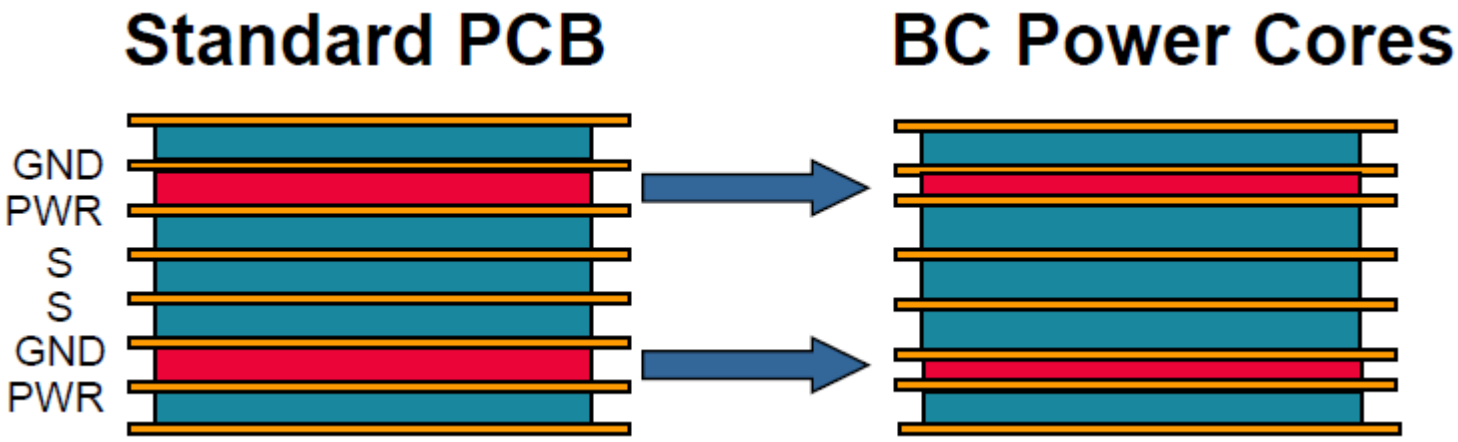
Buried Capacitance ® Conversion



Decrease power plane spacing below 100um
Dramatically improves high frequency capacitance
Closer adjacent power/ground planes reduces plane ΔV due to:
- Increased capacitance at lower frequencies
- Decreased inductance at higher frequencies

Provides additional Z-axis room to increase signal impedances

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Representative ZBC Design Example

(Capasitor Elimination)

# Caps Before	Product	# Caps After	% Eliminated
48	ZBC 2000	17	64 %
48	BC 24	13	72 %
48	BC 16	12	74 %
48	BC 12	11	75 %
48	BC 8	10	77 %

Based on a 1156 Pin BGA, 3.3V power distribution, 603 Style Bypass Caps

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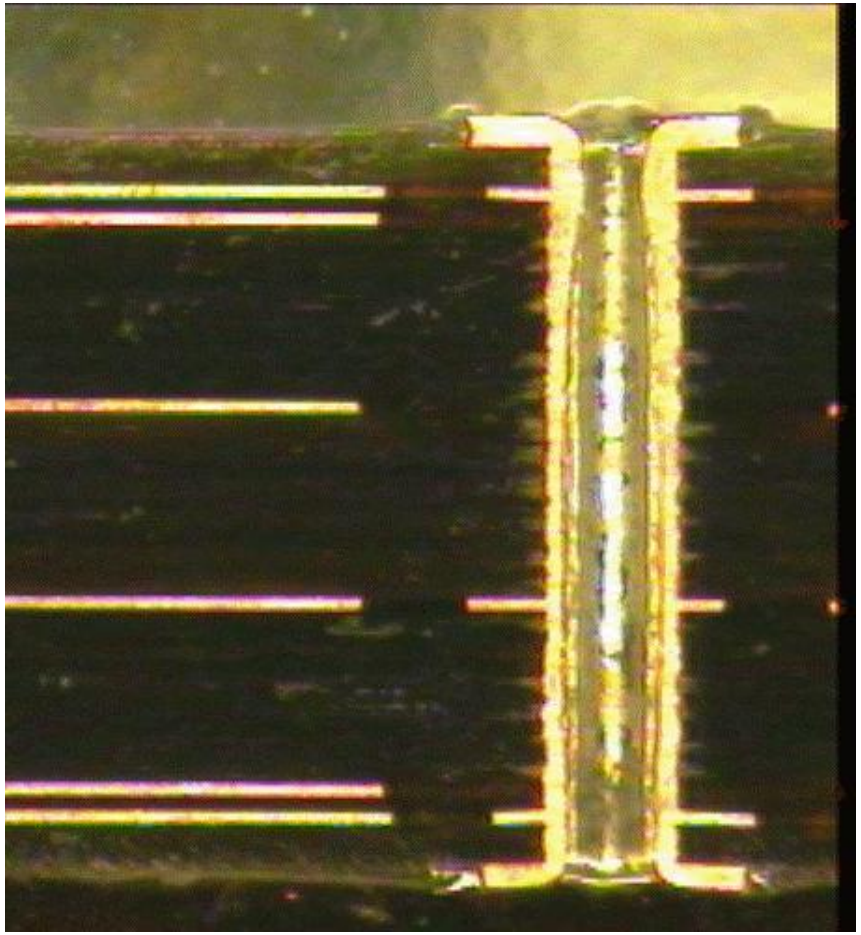
BC Photomicrograph



1 Top
2 Gnd
3 Pwr

4 Sig

5 Sig

6 Pwr
7 Gnd
8 Bot

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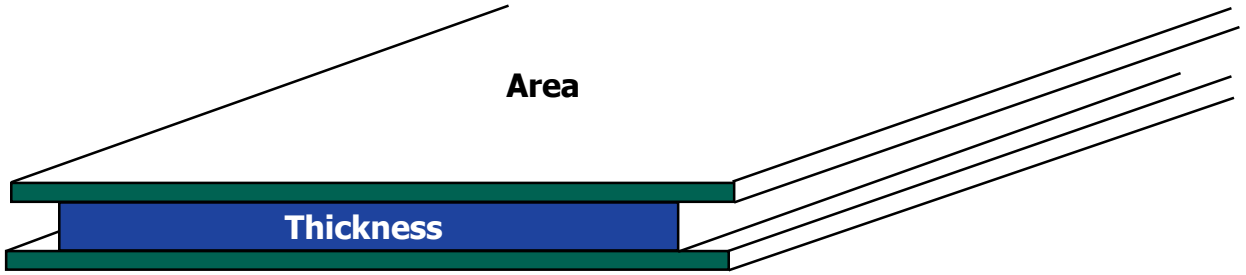
Capacitance Calculation



C = AεD/t where
C - is total capacitance
A - is the area per sq. inch of the plane (or split plane) attached to the active devices
ε - is the dielectric constant of the dielectric material
D - is a constant (225)
t - is the thickness of the dielectric material in mils

Example: (10" x 10" PCB)*2 Planes*4.5*225/2

= 101,250 Picofarads, or **.1 uF**

May not be applicable on small area parts

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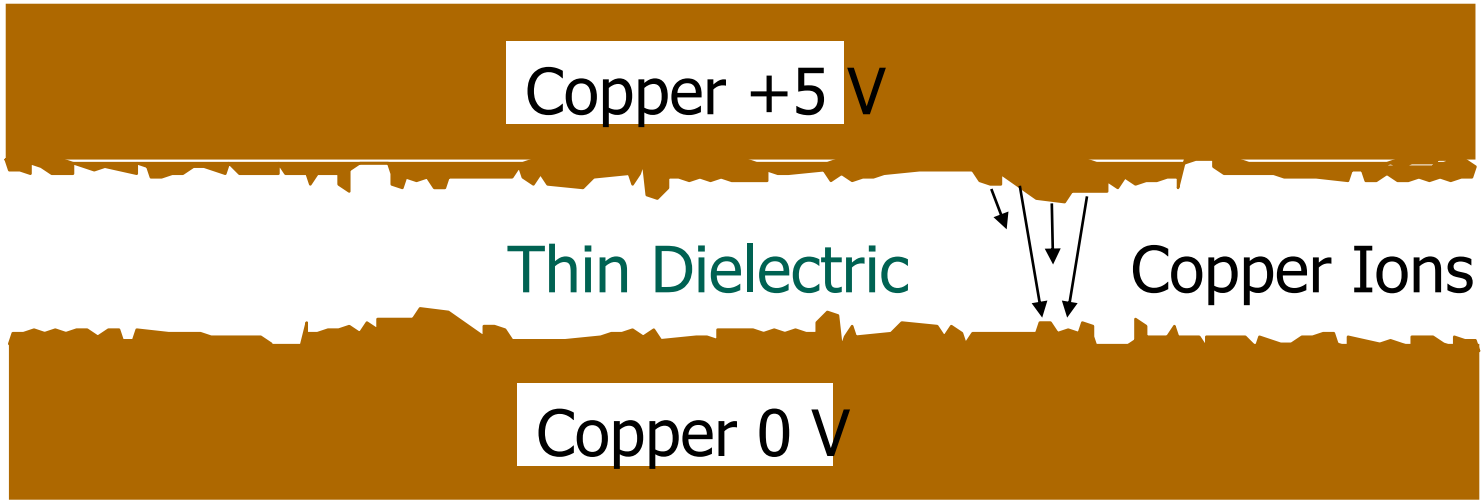
Electromigration of Copper Due to Temperature and Humidity



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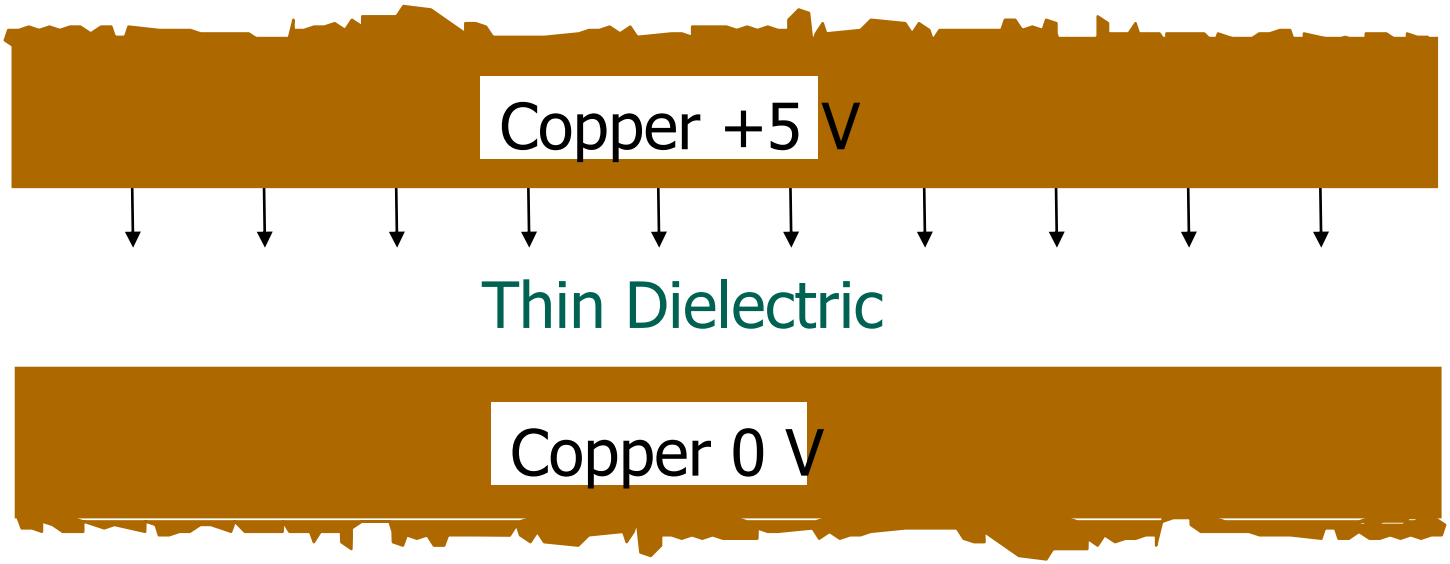
BC Has Flat Internal Surfaces to Distribute the Voltage...and is Tested at 500 VDC



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Full workshop / test report available

3M™ Embedded Capacitor Material Key Properties

Attribute	Value
Capacitance /area	6.4 nF/in² (1.0 nF/cm²)
Dielectric Constant	16
Dielectric Thickness	0.55 mil (14 um)
Dielectric loss @ 1GHz	0.03
Resin system	Epoxy, ceramic filler
Freq., Voltage, Temperature	Meets X7R
Dielectric Strength	~3300 V/mil (130V/um)
Breakdown Voltage	>100V
Copper Thickness	1.4 mil (35 um)
Flammability Rating	94V-0

High Dk value is positive for the capacitance, will not affect signals and impedance value

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The end of BC

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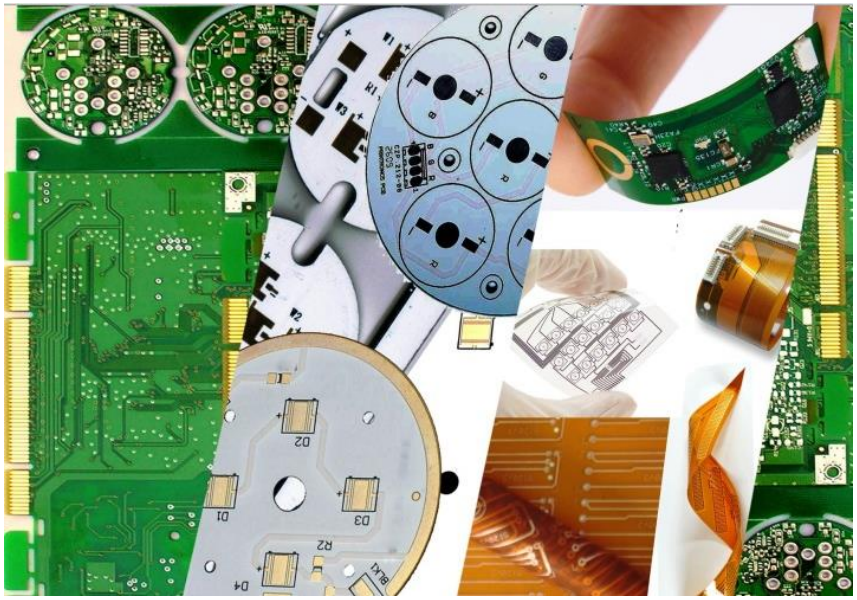

Some stuff on PCB Materials,

- copper structure,

- glass and epoxy.

Specify according to IPC 4101C/xxx

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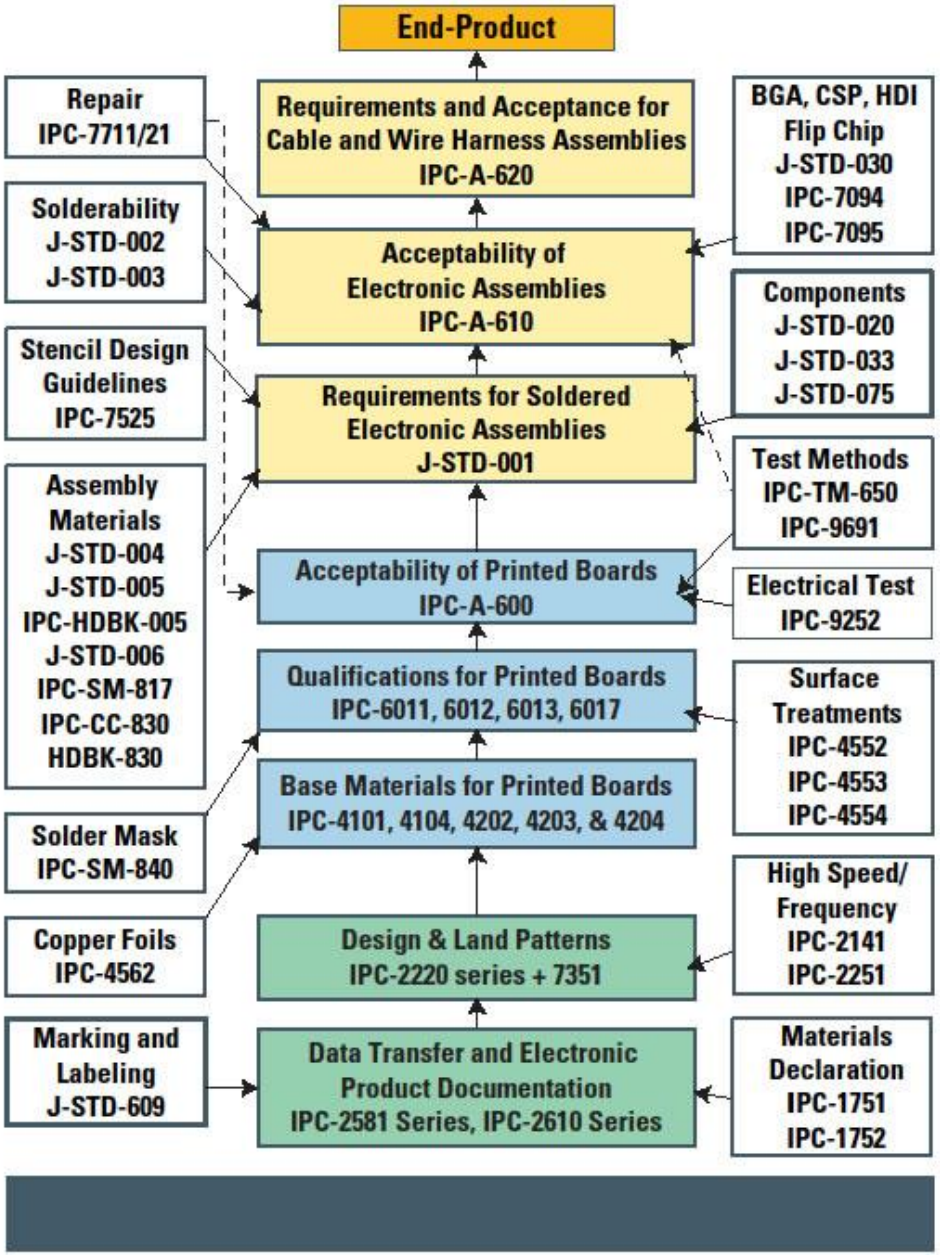
IPC STANDARDS —
EVERYTHING YOU NEED FROM START TO FINISH



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Laminate & Prepreg Manufacturing

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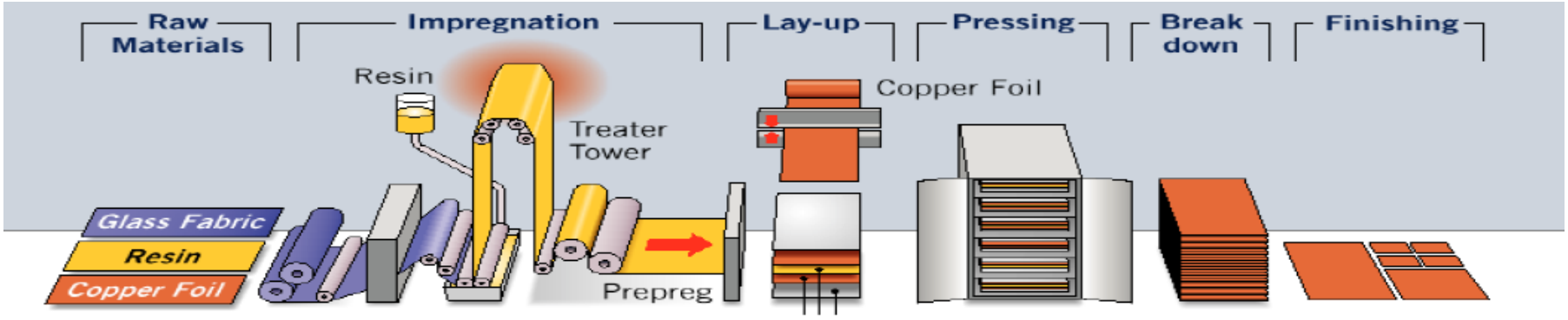
Manufacturing Technology Focus



- **Treating**
  - Gauges for Resin content control
  - On line DCM's, MMV's, FTIR's
  - High Shear mixing equipment, Dedicated lines, Filtration systems
- **Lay up**
  - Sandwich copper concept, separate rooms.
  - Controlled Clean room environment with Humidity and static control.
- **Press**
  - High temperature pressing capability
- **Finishing**
  - High Speed and precise finishing capability.

Manufacturing Focus - Internal contamination Reduction - Controlled environment, Treating technology, handling and lay up technology.
- Prepreg Consistency -Resin content control, On Line cure monitoring, Redundancy with FTIR, Melt viscosity and Gelation - Surface quality -Lay up Technology
- Controlled thickness.

Cost - Productivity enhancement through lean manufacturing, Re-engineered Processes

QTA - Fast turn around capability through cycle time reduction, sophisticated scheduling and equipment capability

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Laminate Material Building Blocks

Glass

- Glass fabric is available in different roll widths, styles and thicknesses
- Some glass fabrics are different between North America, Asia Pacific and Europe
- Core constructions are different depending on the region and OEM specification.

Resin

- The resin is determined by what properties are needed to make a particular MLB design function. ie. Tg, Dk, Df etc.
- The resin must be compatible with the glass fabric
- The resin must be compatible with the copper foil

Copper

- Copper is designated by weight and foil type i.e. Reverse Treat (RTF), HVLP or eHVLP, HTE, Double Treat or std ED copper foil
- The copper used must be able to achieve good peel strengths so the copper does not pull away from the base laminate during mlb processing.

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Woven Glass Fabric

OEM designs are calling out the number of plies of glass to be used per core layer and even calling out the glass fabric style when controlled impedance is critical.

It is important that we understand the effect of the glass used in the construction of the core material we give to an OEM. A 2 ply construction vs. 1 ply will give you a different Dk and Df based on the retained resin % of the core.

When programs move from one Region to the other please be aware of the constructions used in the other Regions. For critical OEM's and designs we need to try and keep the electrical properties of the material the same ie. the same construction of core material and prepreg. Isola has a set of Global Constructions for their High Speed Digital Product Line.

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GlassFabric

Common Glass Fabrics

Glass Style	Weave	Warp Count	Fill Count	Warp Yarn	Fill Yarn	Fabric Thickness inches	Fabric Thickness mm	Fabric Nominal Weight OSY	Fabric Nominal Weight g/m2
1035	Plain	66	68	ECD 900-1/0	ECD 900-1/0	0.0011	0.030	0.88	30
1037	Plain	70	73	ECC 1200-1/0	ECC 1200-1/0	0.0011	0.030	0.68	23
1067	Plain	70	70	ECD 900-1/0	ECD 900-1/0	0.0013	0.032	0.91	31
106	Plain	56	56	ECD 900-1/0	ECD 900-1/0	0.0015	0.038	0.73	25
1078	Plain	54	54	ECD 450 1/0	ECD 450 1/0	0.0017	0.040	1.41	48
1086	Plain	60	60	ECD 450 1/0	ECD 450 1/0	0.0020	0.050	1.60	54
1080	Plain	60	47	ECD 450-1/0	ECD 450-1/0	0.0025	0.064	1.45	49
2113	Plain	60	56	ECE 225-1/0	ECD 450-1/0	0.0029	0.074	2.31	78
2313	Plain	60	64	ECE 225- 1/0	ECD 450-1/0	0.0032	0.080	2.38	81
3313	Plain	61	62	ECDE 300-1/0	ECDE 300-1/0	0.0032	0.081	2.43	82
3070	Plain	70	70	ECDE 300-1/0	ECDE 300-1/0	0.0034	0.086	2.74	93
2116	Plain	60	58	ECE 225-1/0	ECE 225-1/0	0.0038	0.097	3.22	109
1506	Plain	46	45	ECE110-1/1	ECE 110-1/0	0.0056	0.140	4.89	165
1652	Plain	52	52	ECG 150-1/0	ECG 150-1/0	0.0045	0.114	4.09	142
7628	Plain	44	31	ECG 75-1/0	ECG 75-1/0	0.0068	0.173	6.00	203

Fiberglass Yarn Nomenclature

1 st Letter	E = E-glass (electrical grade)
2 nd Letter	C = Continuous Filaments
3 rd Letter	Filament Diameter C, D, E, DE, G
1 Ist number	Yardage in one pound (length)
2 nd number	Number of strands in a yarn/ strands plied or twisted

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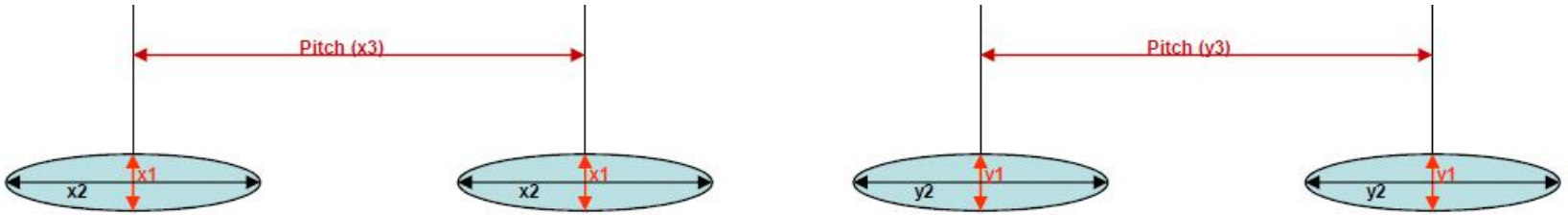
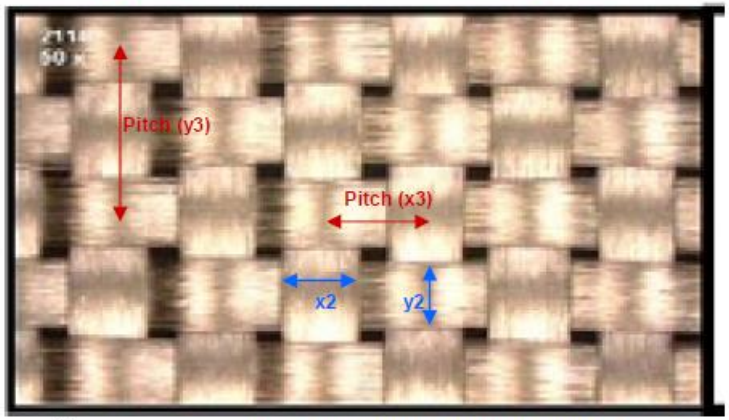
Glass Dimensions





	Measurement Results (mils)					
Glass Fabric	X1	X2	X3	Y1	Y2	Y3
106	1.00	4.80	18.50	0.60	10.20	20.60
1067	0.82	8.85	14.30	0.78	12.40	13.70
1080	1.60	8.20	17.00	1.10	12.10	22.40
1086	1.44	10.80	16.60	1.00	14.70	17.10
2113 / 2313	2.40	10.50	17.00	1.00	15.30	18.20
3313	1.90	13.10	16.20	1.50	11.00	16.30
3070	1.70	12.70	14.80	1.70	12.60	14.20
2116	2.20	14.10	17.20	2.00	14.50	17.30
1652	2.40	15.30	17.50	2.90	15.90	18.80

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Glass Language Terms

Common Terms:

- Expanded Weave
- Open Weave
- Open Filament
- Spread Glass
- Flat Glass
- Mechanically Spread
- Square Weave

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Isola's Glass Definitions

Definitions:

- **Expanded Weave** – Glass Spread More than Standard in one Direction
- **Open Weave** – Same as Expanded
- **Open Filament** – Same as Expanded
- **Spread Glass** – Glass Spread by a # of Different Ways
- **Mechanically Spread (MS) Glass**
  – Glass is Mechanically Spread in both the warp and fill directions.
- **Square Weave** – Glass that has a Balanced Density and/or Yarn Counts in Warp and Fill Directions.
- **Flat Glass** – Glass is made from fibers with little or no twist. Isola does not offer Flat Glass. Spread Glass is "Flatter", but not truly a Flat Glass.

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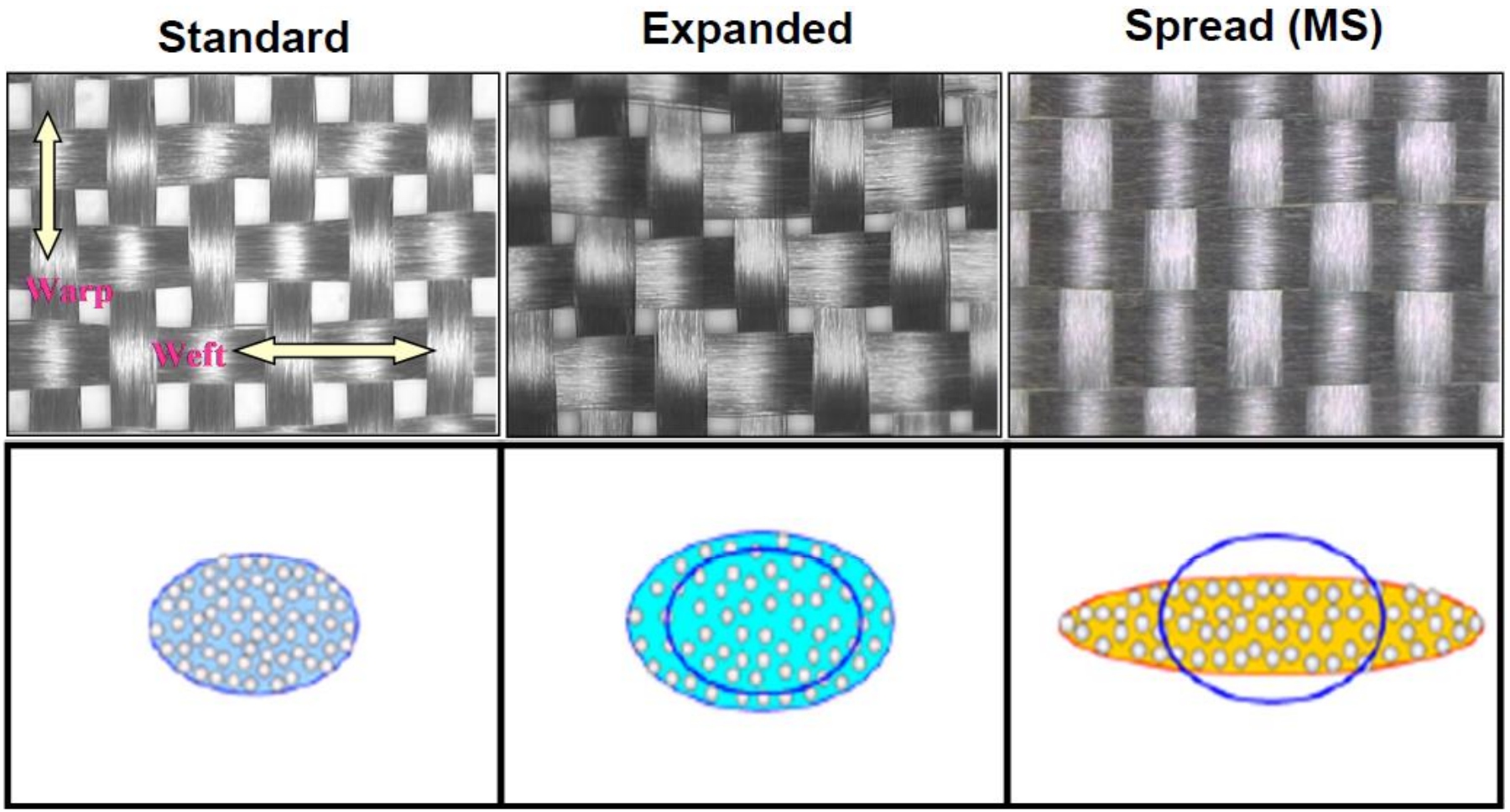
Explanation Glass Spreading Terminology



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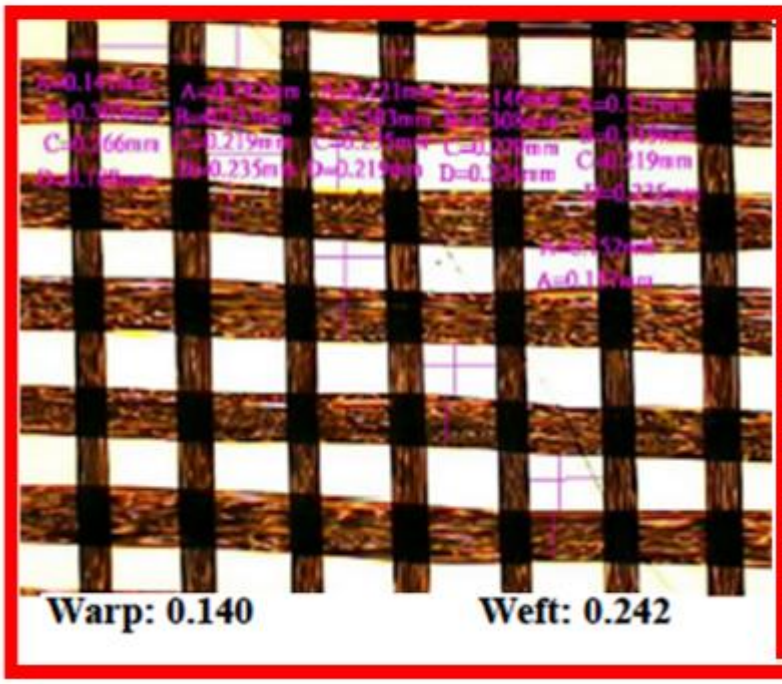
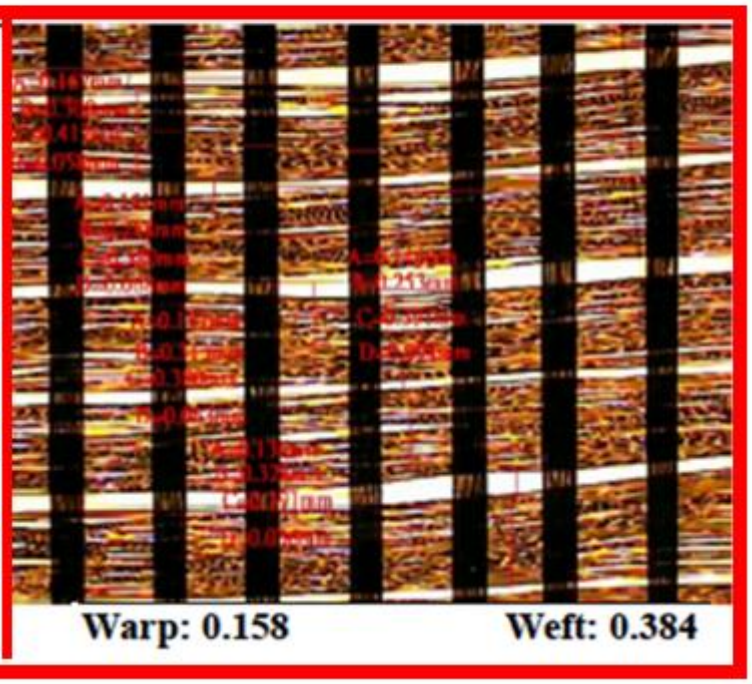
Standard Weave Versus Expanded Weave

106 Standard



106 Expanded



Note: Most of the spreading occurs in the fill direction on the expanded glass

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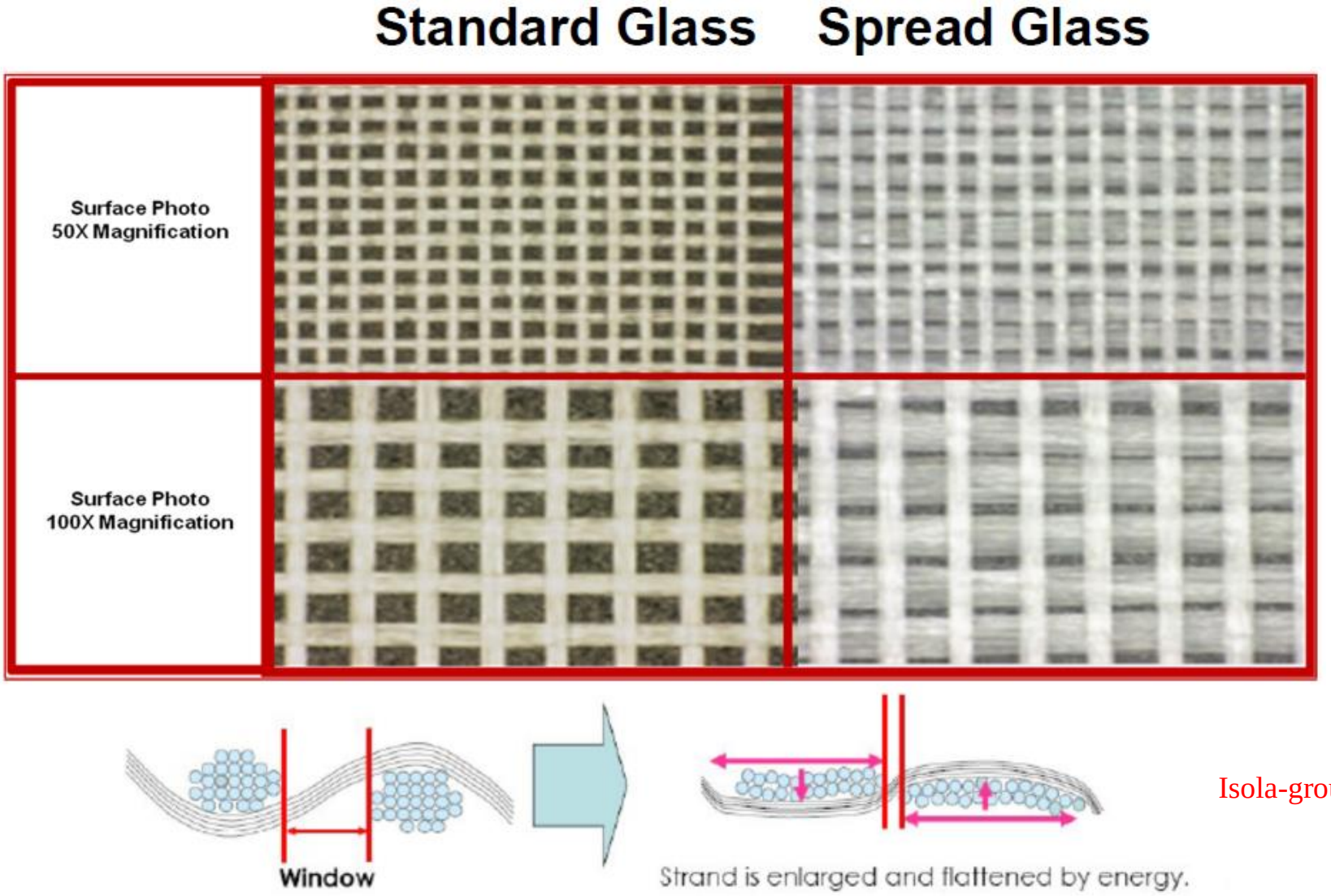
106 Glass Examples



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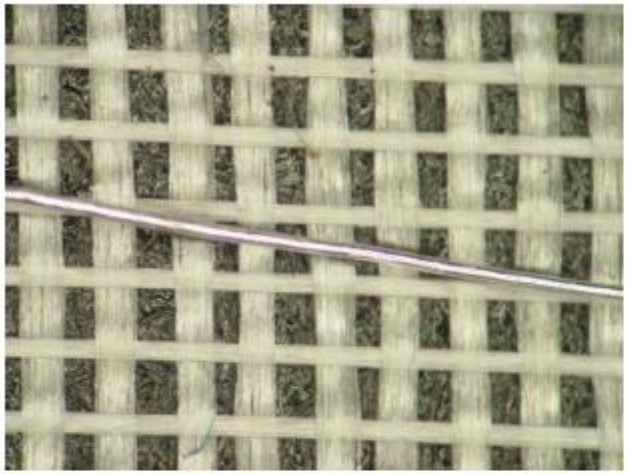
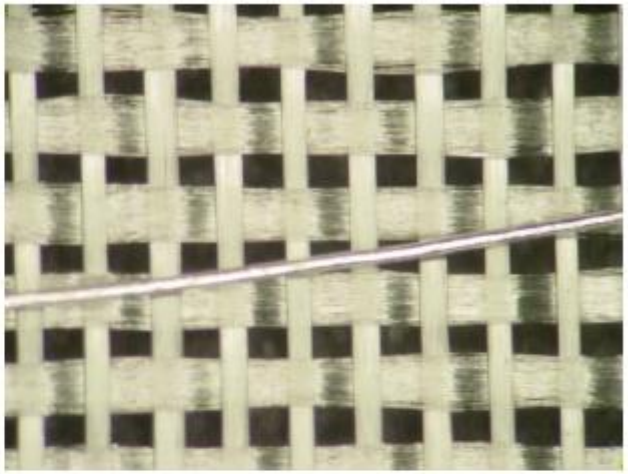
SOME REPRESENTATIVE GLASS STYLES

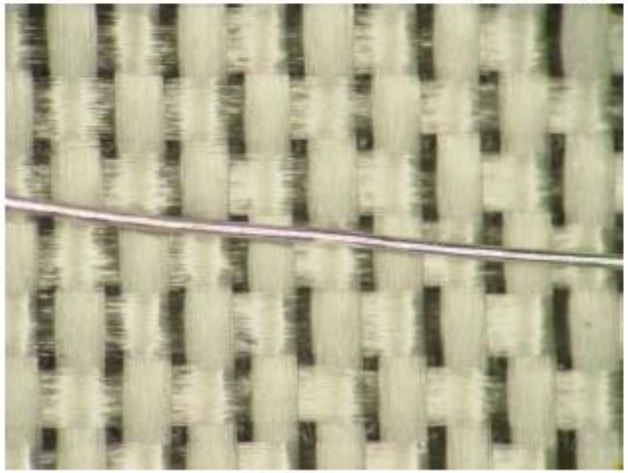


106

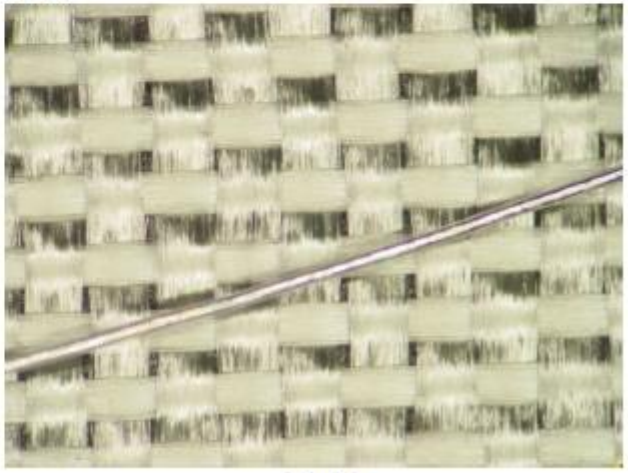
WIRE IS 3.5 MILS IN DIAMETER



1080



2113



3313

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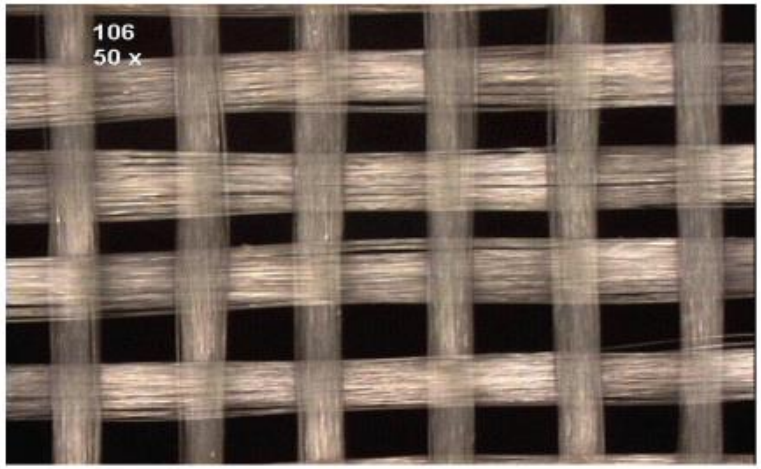
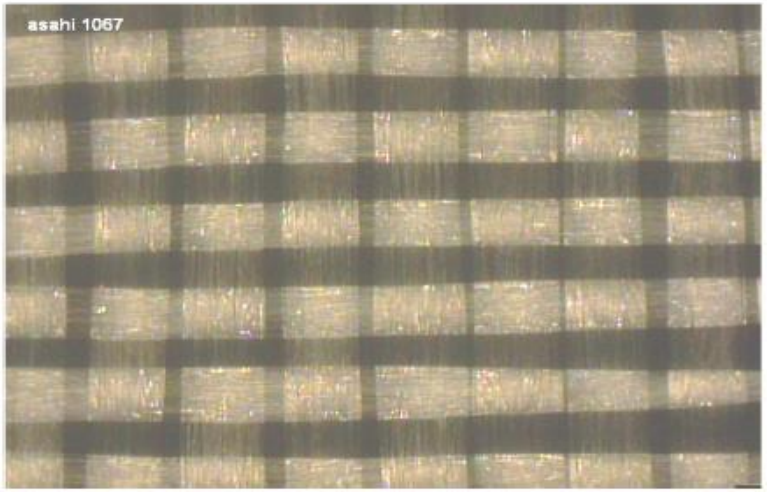
Glass Fabric Photos, Woven Glass Fabric



106
Warp & Fill Count: 56 x 56 (ends/in)
Thickness: 0.0015” / 0.038 mm



1067
Warp & Fill Count: 70 x 70 (ends/in)
Thickness: 0.0013” / 0.032 mm

Photos courtesy of Isola R & D Laboratories

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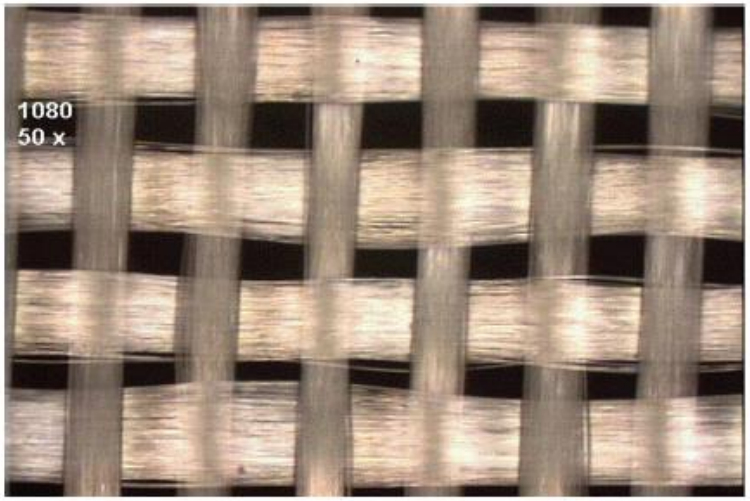
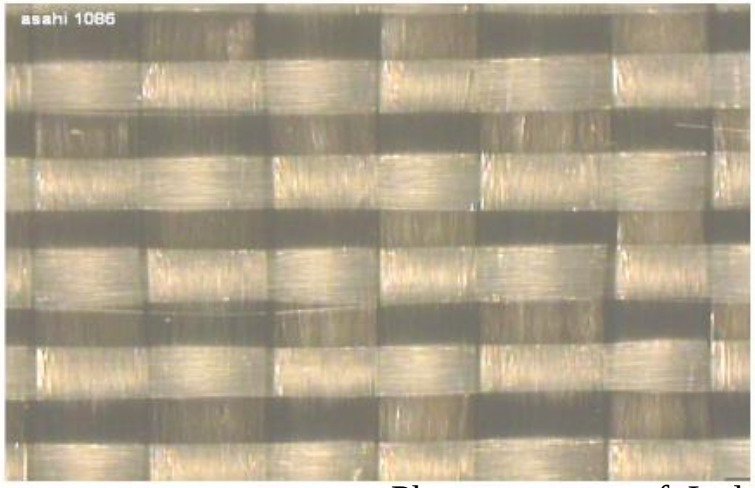
Glass Fabric Photos, Woven Glass Fabric



1080
Warp & Fill Count: 60 x 47 (ends/in)
Thickness: 0.0025” / 0.064 mm



1086
Warp & Fill Count: 60 x 60 (ends/in)
Thickness: 0.002” / 0.050 mm

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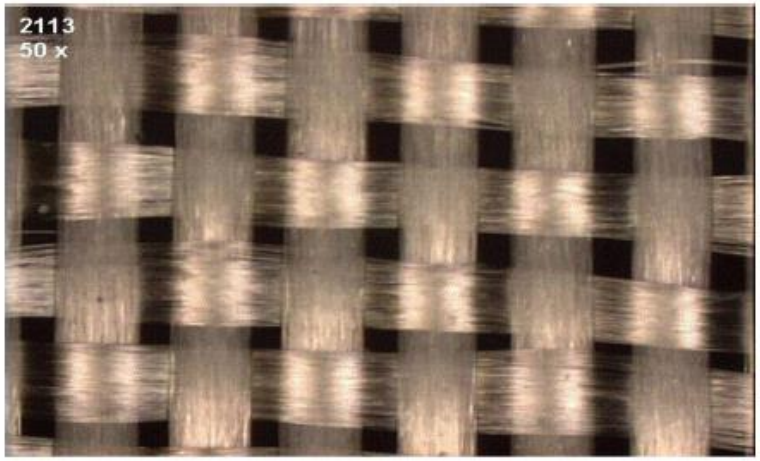
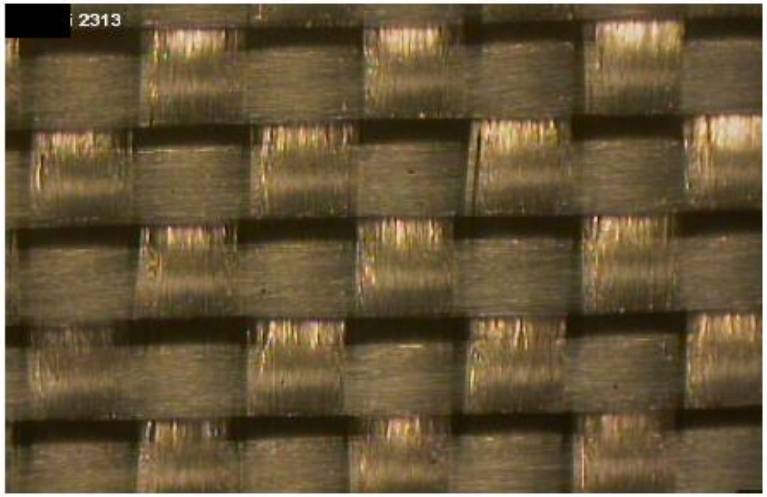
Glass Fabric Photos, Woven Glass Fabric



2113
Warp & Fill Count: 60 x 56 (ends/in)
Thickness: 0.0029” / 0.074 mm



2313
Warp & Fill Count: 60 x 64 (ends/in)
Thickness: 0.0032” / 0.080 mm

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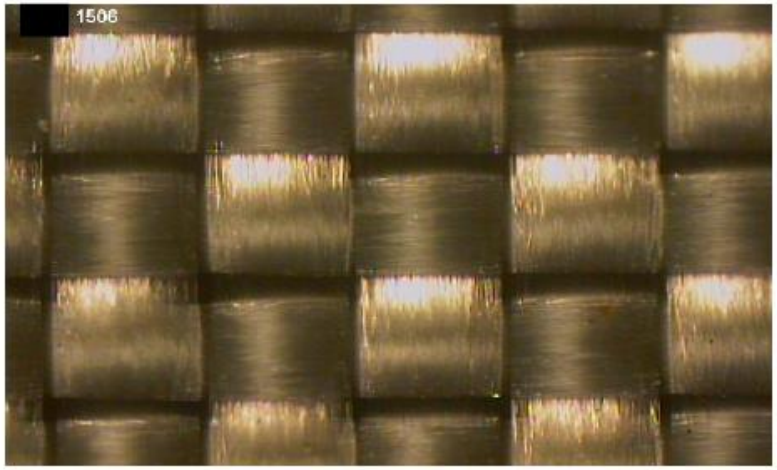
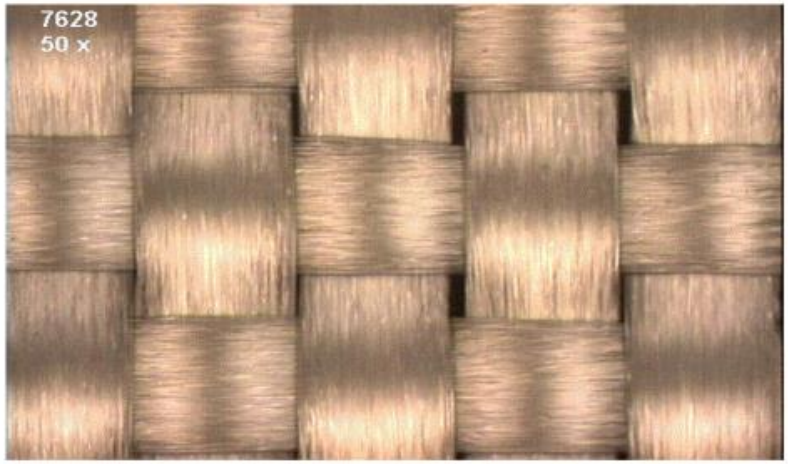
Glass Fabric Photos, Woven Glass Fabric



1506
Warp & Fill Count: 46 x 45 (ends/in)
Thickness: 0.0056” / 0.140 mm



7628

Warp & Fill Count: 44 x 32 (ends/in)
Thickness: 0.0068” / 0.173 mm

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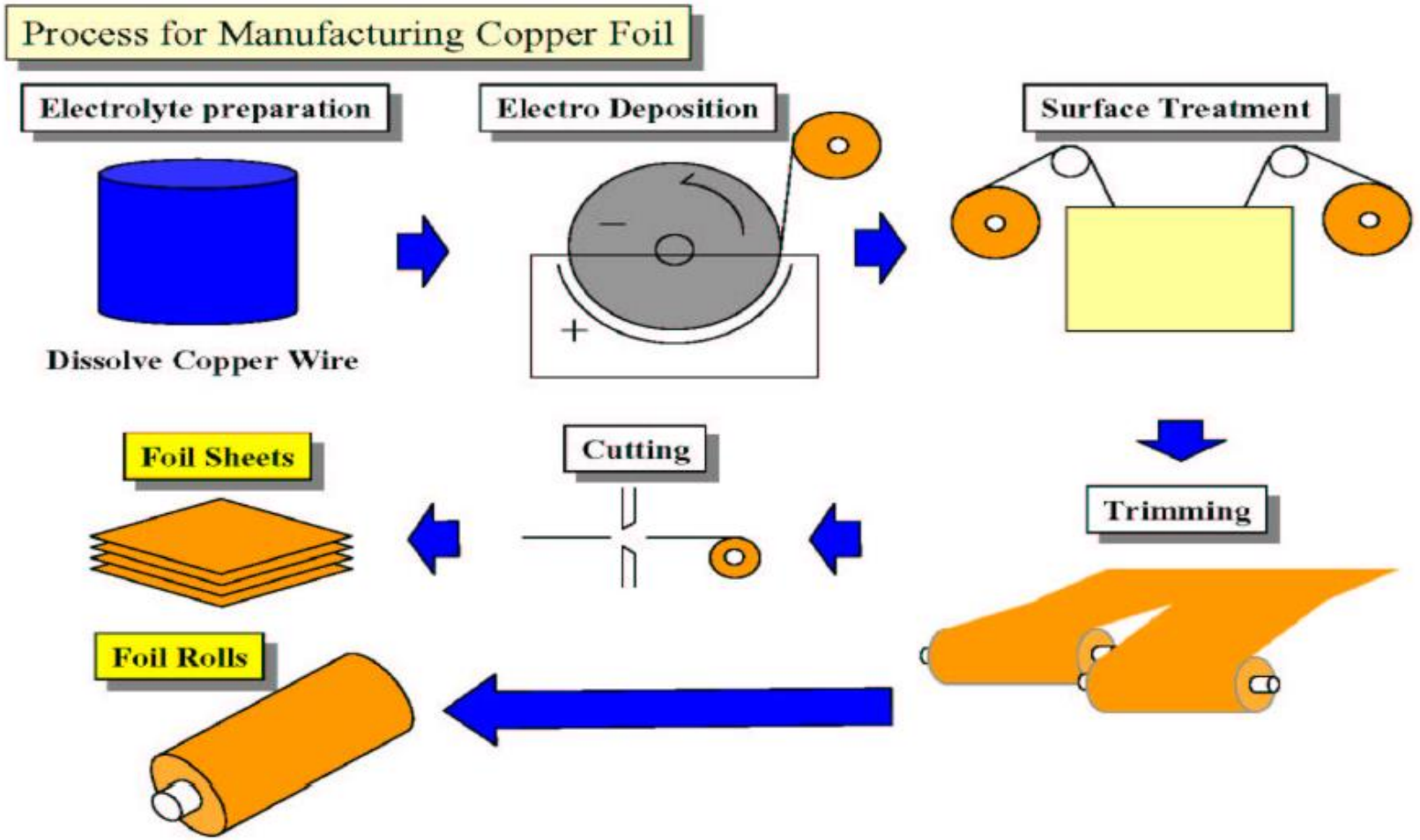
Copper Process Introduction



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Copper Foil Acronyms

- ED – Standard Shiny Copper
- HTE– High Tensile of Elongation, Standard Shiny Copper
- DSTF ® – Drum Side Treated Foil*
- RTF – Reverse Treated Foil
- VLP – Very Low Profile
- e-VLP – Extra(?) Very Low Profile*
- H-VLP – H (?) Very Low Profile*

  - *** Not IPC Designations**

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Copper Foil Types

ED = Standard Shiny Copper, Copper Tooth
HTE = High Temp Elongation Shiny Copper, Copper Tooth
DSTF/RTF = Reverse Treat, Low Profile Copper Tooth
DT = Double Treat Copper, No Black Oxide Needed

- The RTF Copper Foils Offer Benefits To The Fabricator During Processing – More Defined Etched Line, Ability For Thinner Lines And Lower Copper Tooth Profile.

- **VLP/e-VLP/H-VLP** Foils Are Used For Better Impedance Control & Improved Signal Integrity

- 95+ % Of NA Is RTF Foil. Very Small Percentage = DT

- RTF Foil Use Increasing In Asia-Pacific Region

- Thicker Cores Still Use Some HTE Or ED Foil.

Copper Weights

18 micron = H oz
35 micron = 1 oz
70 micron = 2 oz

Heavier Copper Such As 3, 4 And 5 Oz Foil Used For Power Supply Designs Or Ground Planes In MLB Designs

5 and 6 oz Cu for Automotive 4 – L designs

12 oz Cu used for Automotive 2 – L designs

DSTF*=Drum Side Treat Foil*

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Electrodeposited Copper Foil

- ED Foil is “Industry Standard”
- Many Thicknesses Available
- Grade 3 is Industry Standard Inner-layer Foil

Grade	Foil Description
1	**Standard Electrodeposited**
2	High Ductility Electrodeposited
3	**High Temperature Elongation Electrodeposited**
4	Annealed Electrodeposited
5	As Rolled-Wrought
6	Light Cold Rolled-Wrought
7	Annealed-Wrought
8	As Rolled-Wrought Low-Temperature Annealable

Foil Profile Type	Max. Foil Profile (Microns)	Max. Foil Profile (µ Inches)
S – Standard	N/A	N/A
L – Low Profile	10.2	400
V – Very Low Profile	5.1	200
X – No Treatment or Roughness	N/A	N/A

Foil Designator	Common Industry Terminology	Area Weight (g/m^2)	Nominal Thickness (µm)	Area Weight (oz/ft^2)	Area Weight ($g/254\ in^2$)	Nominal Thickness (mils)
E	5 µm	45.1	5.0	0.148	7.4	0.20
Q	9 µm	75.9	9.0	0.249	12.5	0.34
T	12 µm	106.8	12.0	0.350	17.5	0.47
H	**½ oz**	**152.5**	**17.2**	**0.500**	**25.0**	**0.68**
M	¾ oz	228.8	25.7	0.750	37.5	1.01
1	**1 oz**	**305.0**	**34.3**	**1**	**50.0**	**1.35**
2	**2 oz**	**610.0**	**68.6**	**2**	**100.0**	**2.70**
3	3 oz	915.0	103.0	3	150.0	4.05
4	4 oz	1220.0	137.0	4	200.0	5.40
5	5 oz	1525.0	172.0	5	250.0	6.75
6	6 oz	1830.0	206.0	6	300.0	8.10
7	7 oz	2135.0	240.0	7	350.0	9.45
10	10 oz	3050.0	343.0	10	500.0	13.50
14	14 oz	4270.0	480.0	14	700.0	18.90

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Copper Foil Definitions

- STD HTE (Standard Shiny Copper) Adhesion Treatment is Applied to Matte Side
- DSTF ® (Drum Side Treated Foil) – Adhesion Treatment is Applied to Shiny/Drum Side
- RTF (Reverse Treated Foil) Same as DSTF ®
- LP –Low Profile Foil with Tooth 5.1-9.9 Microns
- VLP – Very Low Profile Foil with Tooth < 5 Microns
- HVLP/ e-VLP - Very Low Profile Foils

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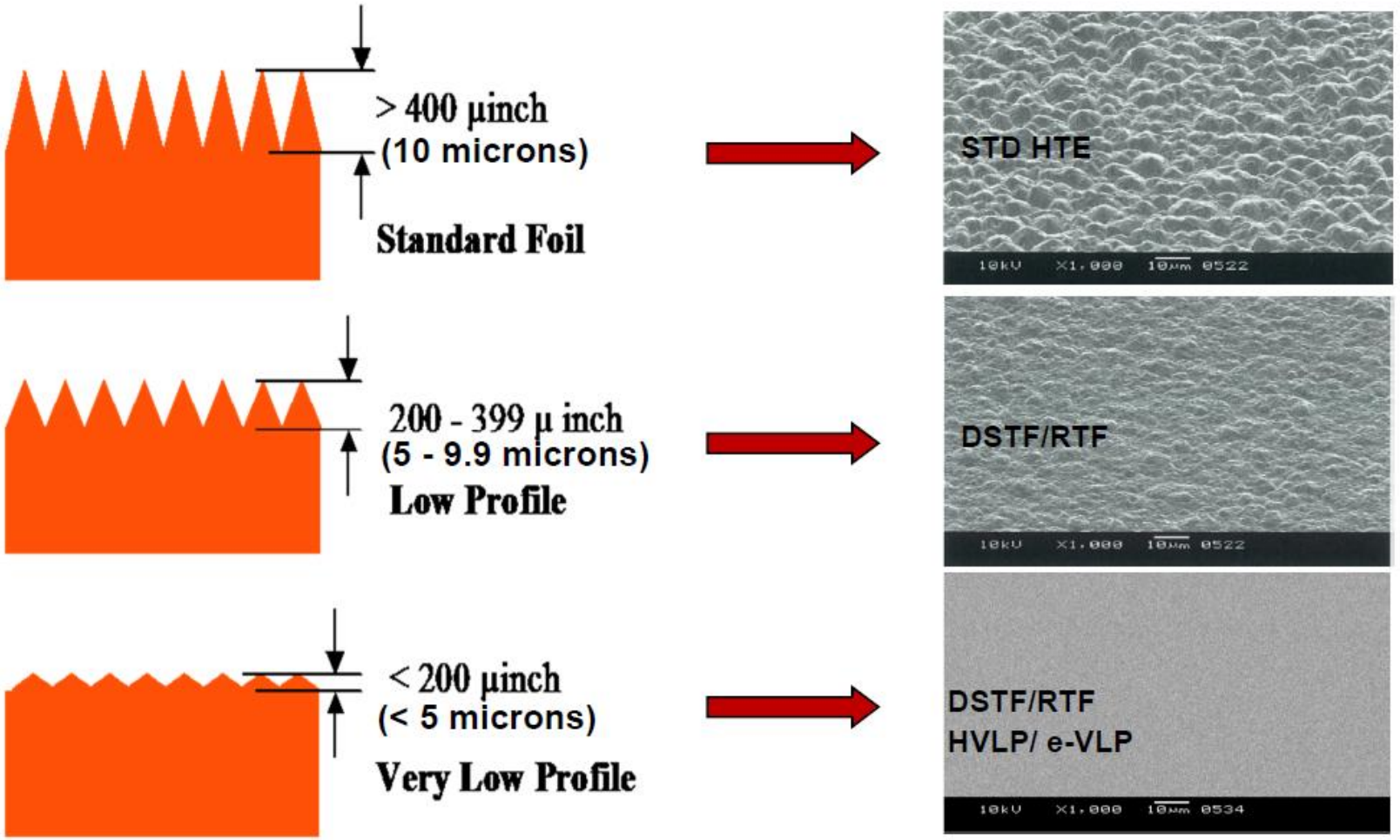
Copper Roughness Specifications



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Copper Foil Roughness Parameters

Ra:

- Ra Is The Average Roughness of The Surface. It Is The Area Between The Roughness Profile And Its Mean Line, Or The Integral Of The Absolute Value Of Roughness Profile Height Over The Evaluation Length

Rz:

- Rz Is The Average Difference Between The "Peaks" And The "Valleys" In The Surface.

Rq/RMS :

- Root Mean Square Is An Average Of The Peaks And Valleys On A Surface. Tends To Give 11% Lower Result Than Ra On Same Surface.

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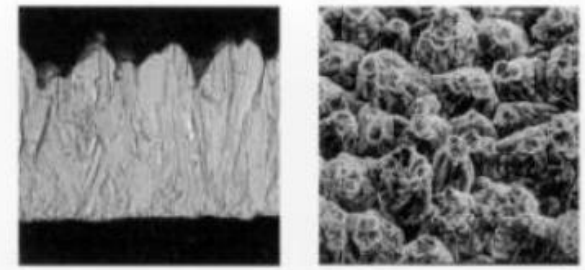
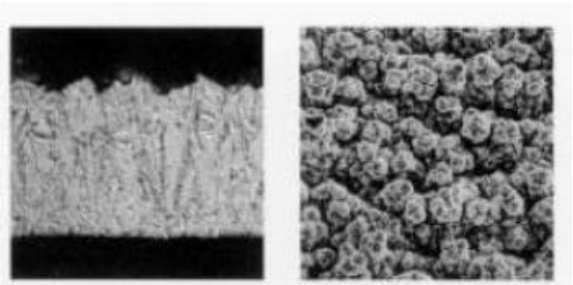
Copper Surface Profiles

Matte Side Surface Profile



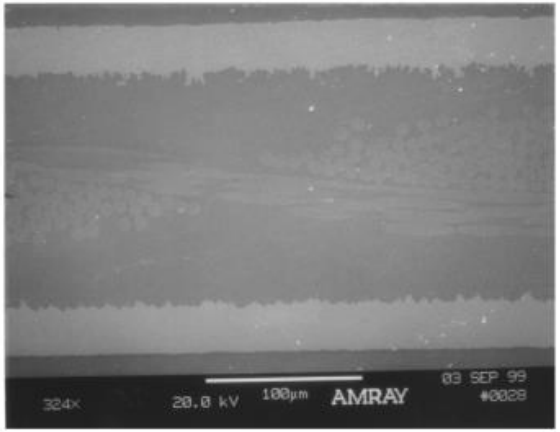
Matte Side of Standard Grade 1 Foil

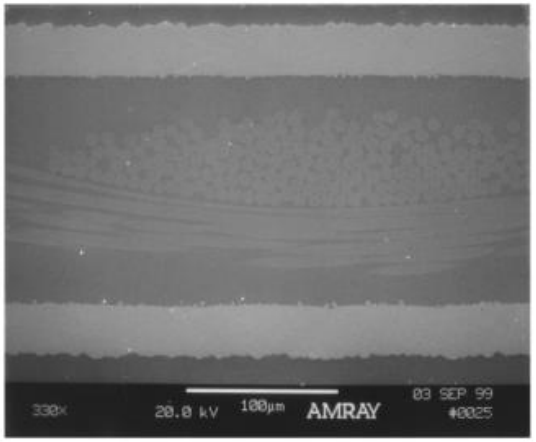


Matte Side of Low Profile Grade 1 Foil

• Standard vs Drum Side Treated Foil (DSTFoil)

Laminate With Standard Copper Foil





Laminate With DSTFoil® Copper Foil

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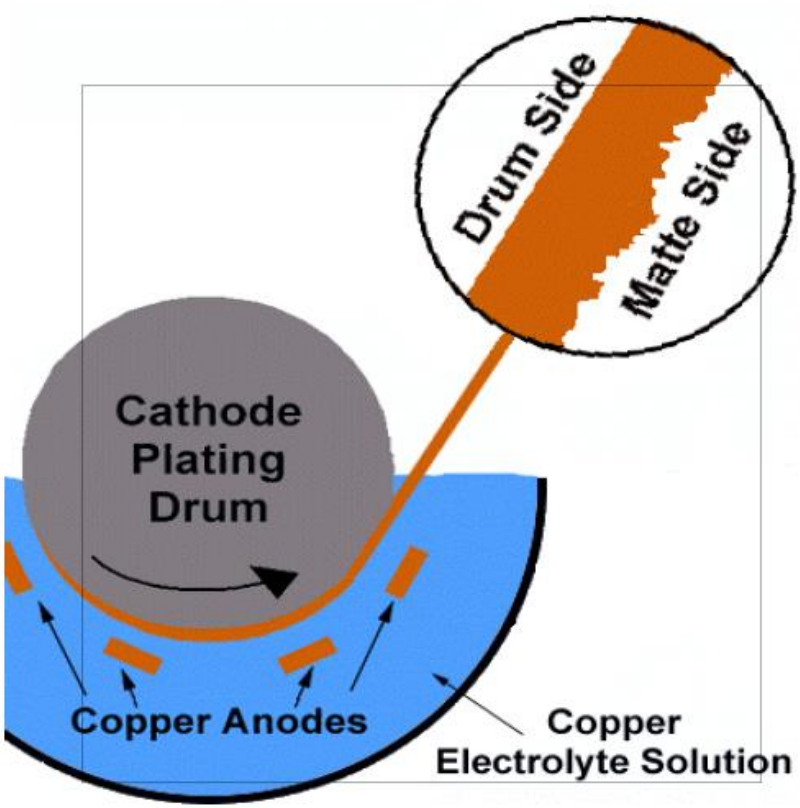
THE PCB REFERENCE

DSTF®& RTF Process Introduction

Copper Foil Manufacturing Process



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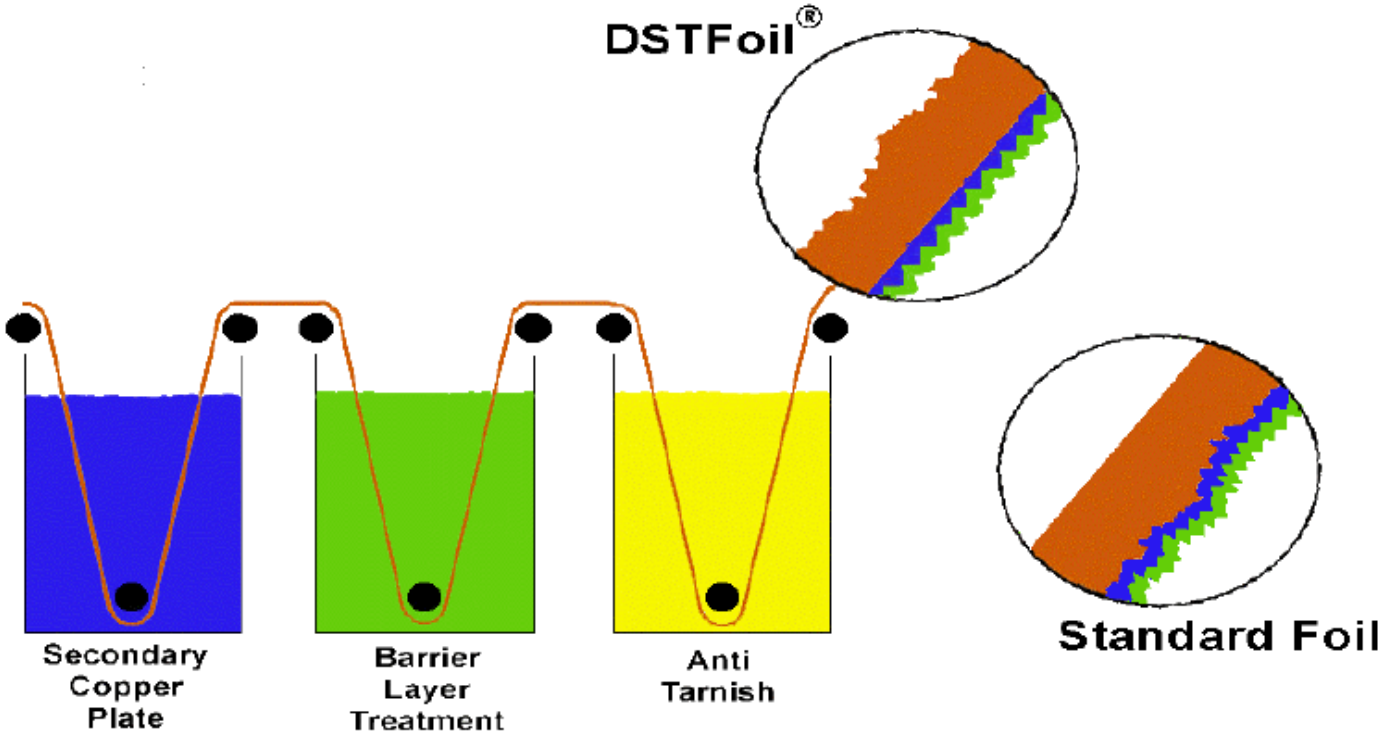
DSTF®& RTF Process Introduction

Copper Foil Treatment



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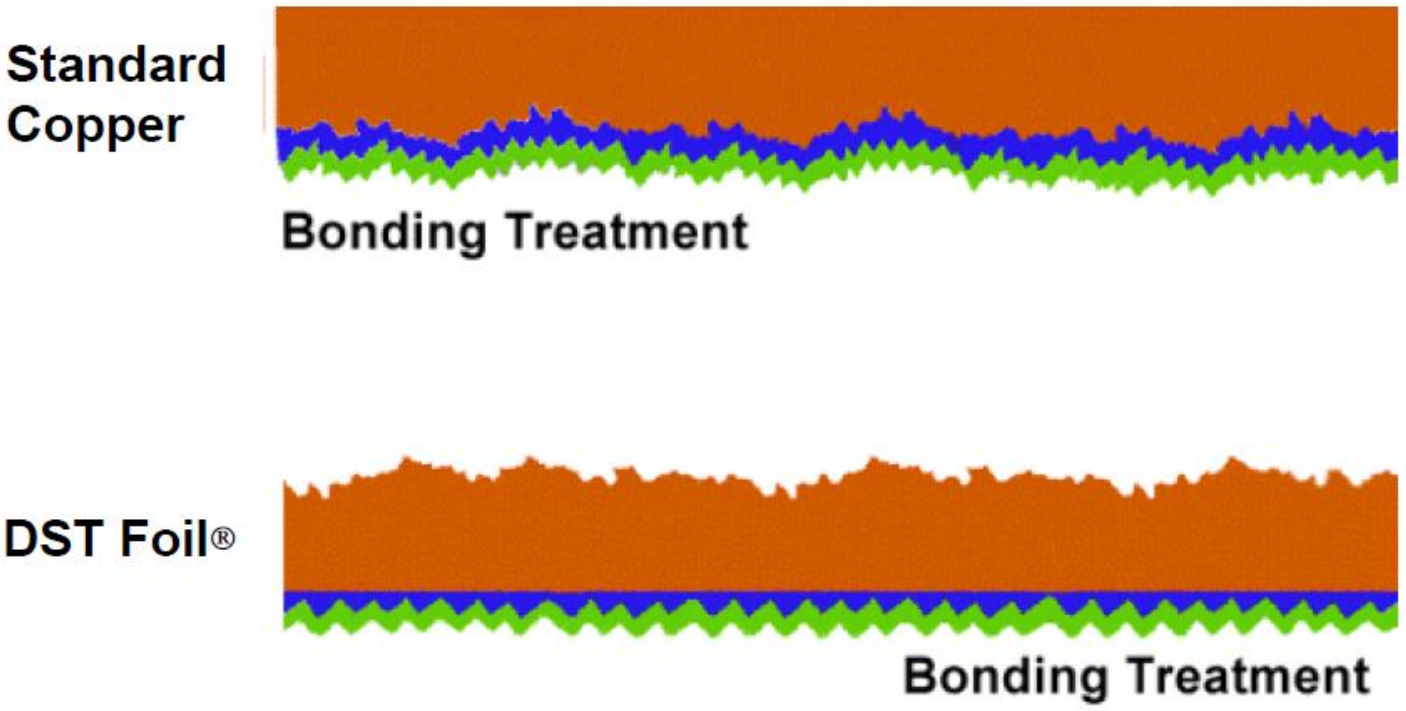
DSTF®& RTF Process Introduction

DSTFoil® Comparison to Standard Copper Foil



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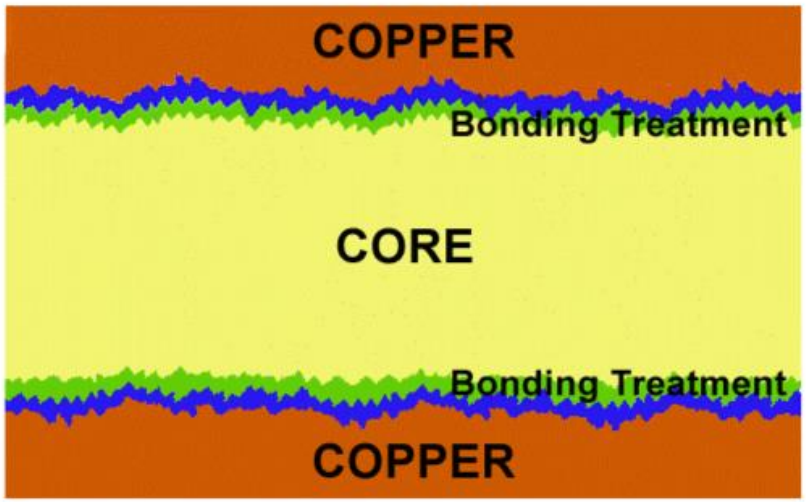
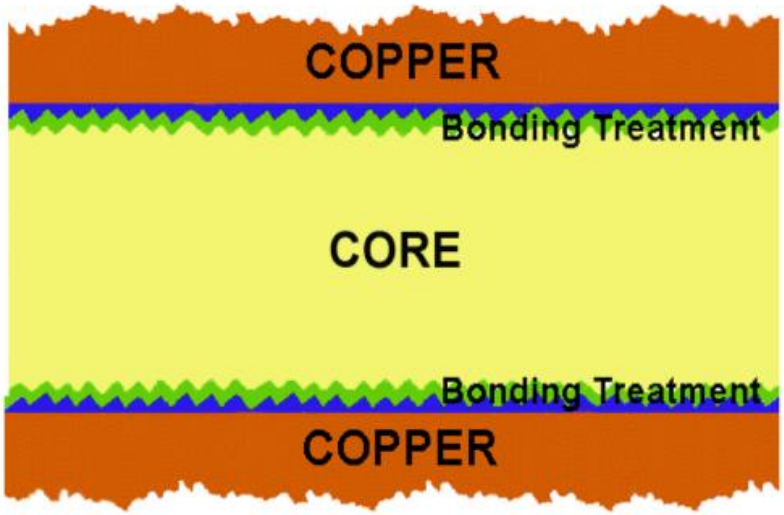
DSTF®& RTF Process Introduction

Standard Foil Clad Laminate



DSTFoil ® Clad Laminate



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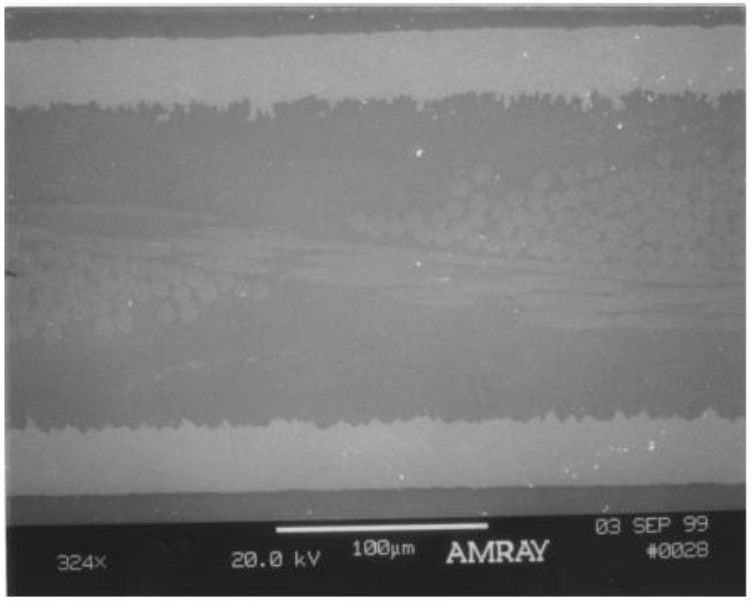
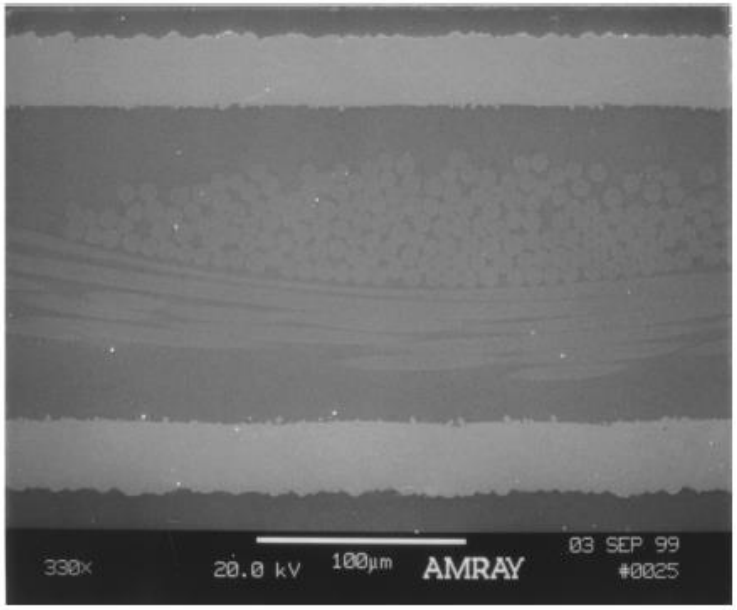
DSTF®& RTF Process Introduction



Laminate clad with traditional copper foil



Laminate clad with DSTFoil®

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Which Copper Should You Specify ?

- STD HTE -At high frequencies, middle and high profile copper foil may present problems concerning their matte side (such as signal attenuation and signal delay owing to increased propagation distance.

- DSTF, RTF & VLP -Will provide improved quality on high frequency transmission Lines. Will also provide smaller deviations on characteristic impedance due to improved etching capabilities.

- HVLP & e-VLP-Since these foils are usually smooth on the resist side and have lower roughness than the DSTF and RTF foils, they will provide additional signal improvement. This is especially true at the higher frequencies because the signal is now travelling closer to the surface of the foil.

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What Are the Tradeoffs?

Copper Types	Peels Strength	I/L Yields	Impedance	Signal Integrity	Costs
STD HTE					
DSTF/RTF/VLP					
e-VLP/H-VLP					

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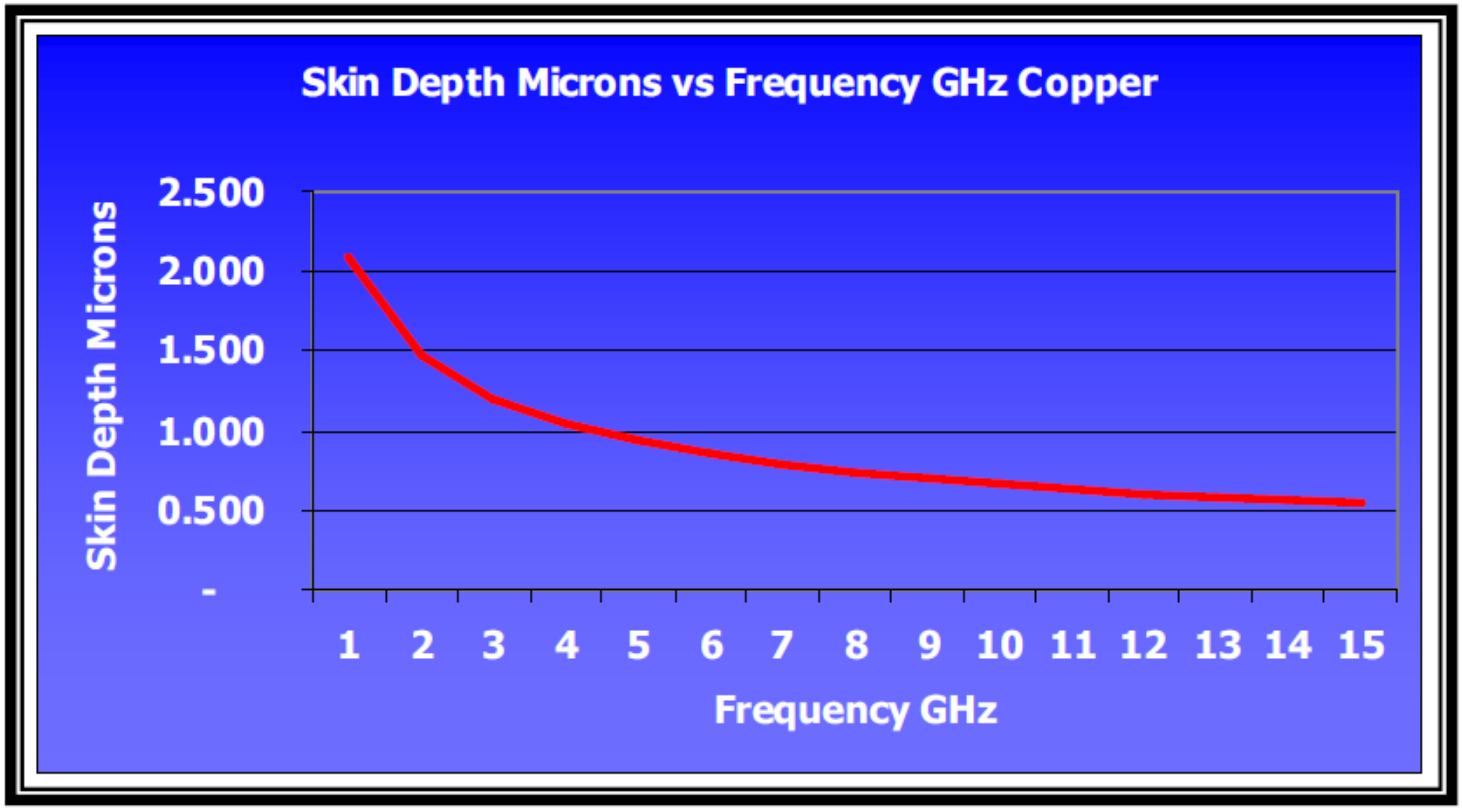
Skin Effect



Skin effect: The tendency of alternating current to flow near the surface of a conductor. The skin effect is caused by the self-inductance of the conductor, which causes an increase in the inductive reactance at high frequencies, thus forcing the carriers, i.e.,electrons, toward the surface of the conductor.

$\Delta = 2.5 \sqrt{1/f}$= Skin depth in microns

Where f is the frequency in GHz

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PROBLEMS WITH ROUGHNESS SPECIFICATIONS

- At the present time, there are no standards for specifying copper roughness.
- There are several designators such as low profile, but each copper supplier uses the term differently.
- It appears there is no activity underway to develop a reliable roughness standard.
- At present, the only reliable way to control copper roughness is to determine the minimum copper roughness required to assure delamination does not occur and put this requirement on the fabrication drawing.
- The proper place to obtain the copper roughness spec. is the laminate manufacturer.

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High Speed

Selecting the Right Material

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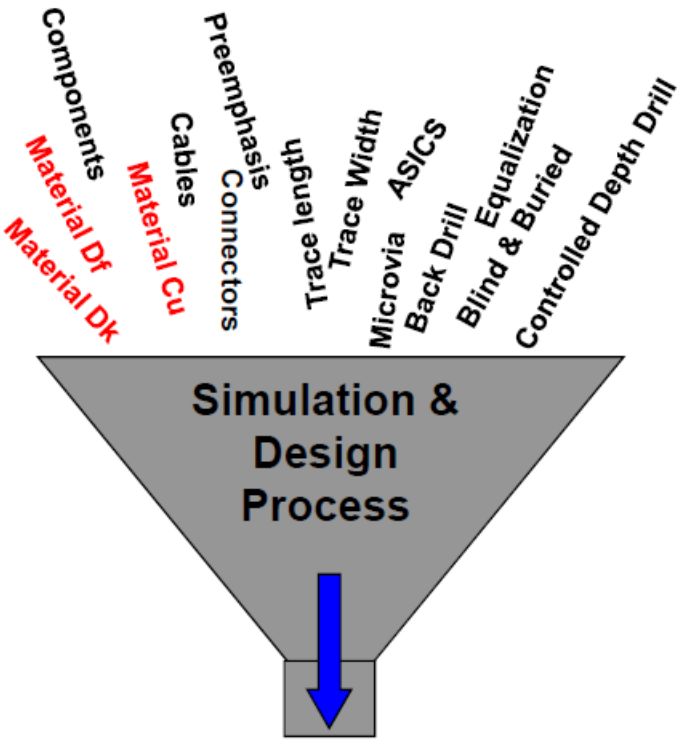
Design Considerations

- Laminate Material Properties are critical for the High Speed Digital PCB Design. A better performing material can offset the need for more expensive design options.

- PCB design options such as structure, interconnect type, layout, can offset the loss of a lesser performing material at a higher cost.

- System design options such as choice of cables, connectors, components, ASICS, can offset the loss of lesser performing material at a higher cost.



Prototype Designs

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Glass Transition Temperature, Tg

- The T_g of a resin system is the temperature at which the material transforms from a rigid or “glassy” state, to a more deformable or softened state.

- T_g is important to understand since the properties of base materials are different above the T_g versus below the T_g.

- IPC TM650 2.4.24C - TM650 2.4.25

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Decomposition temperature, Td

- The decomposition temperature is a measure of actual chemical and physical degradation of the resin system. This test uses thermo-gravimetric analysis (TGA), which measures the mass of a sample versus temperature.

- The decomposition temperature is reported as the temperature at which 5% of the mass of the sample is lost to decomposition when heating up to 550C at 10C/min rate.

- IPC 650 2.4.24-6.

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Time to Delamination

- **T260 -T288 – T300**
- The time to delamination is a measure of the time it takes for the resin and copper, or resin and reinforcement, to separate or delaminate.
- Bring a sample to a specified temperature - measure the time it takes for failure to occur.
- With Pb-free assembly temperatures reaching above 260^{o}C, T288/300 have become a relevant measure of performance.
- IPC TM650 2.4.24-1.

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Coefficient of Thermal Expansion CTE

- **Z-CTE = Thermal expansion in the z-axis**
  - » *(The expansion of the PCB thickness)*
- Z-CTE are measured as PPM per ^{o}C, or as the total material expansion from 50-260^{o}C, in % of thickness. It is specially interesting to know the thermal expansion above Tg, where the expansion rate exellerates rapidely. Here you can sort the good from the ”less good” laminates!
- Z-CTE is described in IPC TM650 2.4.24C
- CTE values are important since they influence the reliability of the finished circuit.
- Other things being equal, less thermal expansion will result in greater circuit reliability as less stress is applied to plated holes

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- Laminate material selection can not be condensed into a single page chart for easy selection. For low speed it can.

- Designers know what they want to achieve.
  High performance laminate material suppliers have a much better understand of material performance.

- Cost to performance evaluations shall be done by the system design team to ensure the lowest cost material that will do the job is selected

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Dk, Df and Copper Type

Dielectric Constant (Dk)

- Matching material performance numbers is important. A small difference in this value between materials can impact impedance, line widths, and thus losses significantly.
- Look at construction options that allow you to find a drop in and match impedance

Dissipation Factor (Df)

- These number vary dramatically by resin content, resin type, frequency, and test method
- Be sure to thoroughly understand the methods used to derive the numbers.
- Compare apples to apples and Df to Df at equal test conditions and resin contents

  when looking at a suppliers data sheets

Copper Type

- Low profile copper provides better results than standard profile copper.
- RTF or DSTF type foils offer significant improvements in loss characteristics. VLP/ HVLP copper foils are being used as well for better impedance but there is a tradeoff with cost and performance that needs to be considered.

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Laminate Data Sheets

- Laminate properties need to be fully tested across a range of resin contents, frequencies and constructions using appropriate test methods. Dk and Df change over resin content.

- **Dk** and **Df** values at 1 MHz and 1 GHz alone do not provide sufficient data for designers for High Speed Digital applications.

- Laminate data sheets provide single points of information for Dk and Df based on a single resin content. Isola uses 55 % resin in Dk/Df data on its data sheets. A range of data is essential for design work. The next slide shows the change in **Dk** and **Df** over the resin % range at 5 GHz from 45 to 75 % resin.

- **Dk** and **Df** data at resin below 50 % are really not representative of materials used in mlb designs unless thicker cores are being used. *Laminate suppliers will use "resin values" to make the **Dk** and or **Df** number look good.*

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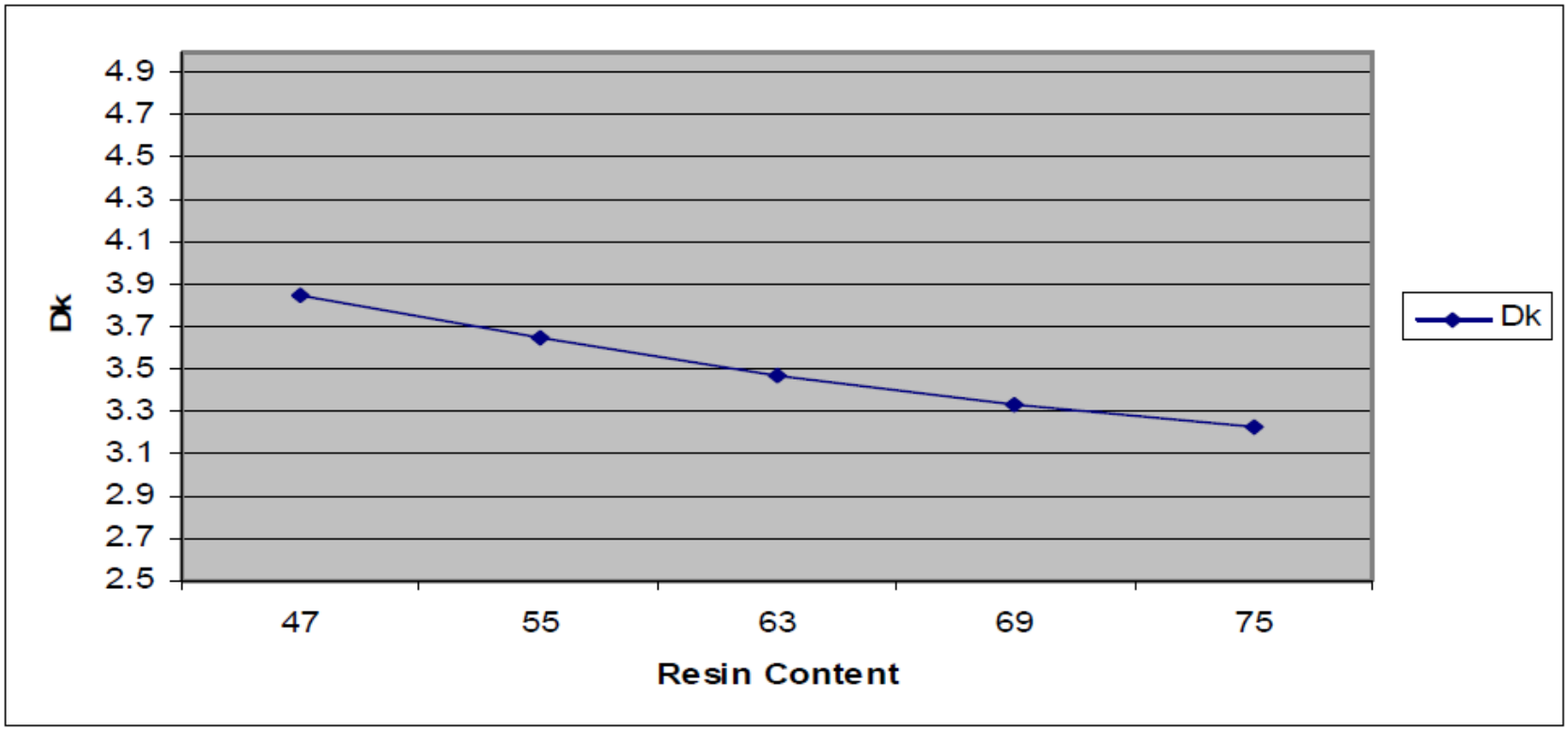
FR408HR Dk vs Resin %



- Thicker cores > 0.3 mm are typically below 50 % resin
- Cores < 0.3 mm are from 50 to 70 % + resin depending on the thickness and glass used
- Prepregs are typically 50 to 76 % resin dependent on the glass style

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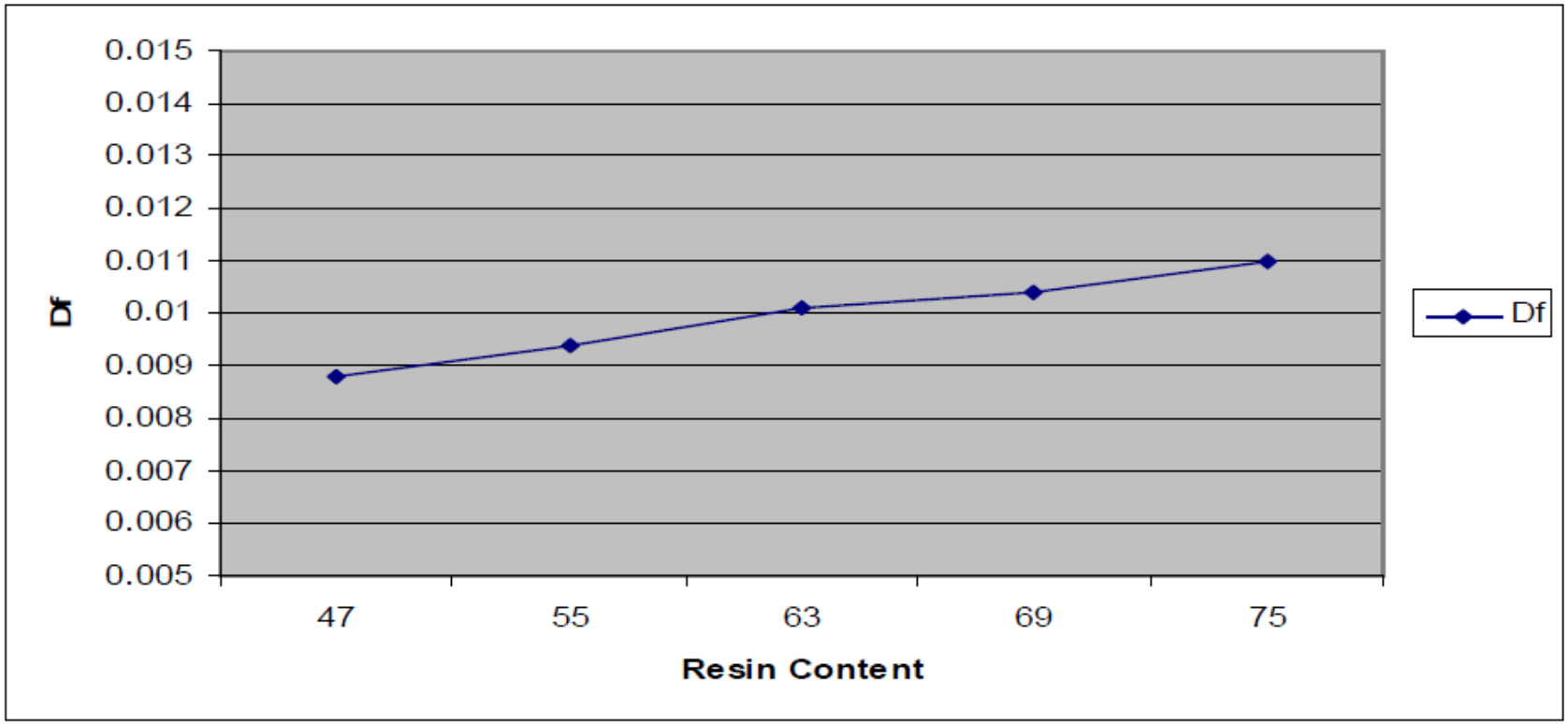
FR408HR Df vs Resin %



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- Prepregs are typically 50 to 76 % resin dependent on the glass style

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Test Methods

Laminate Test Methods

- Study the methods and expected results
- Understand the differences between methods
- Only compare like methods PCB

Test Methods

- Study the methods and expected results
- Standardize the test method
- Validate laminator claims of performance

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Electrical Test Methods

Methods	Specification	Sample		Frequency Range
		Thickness	Size	
Two Fluid Cell	IPC 2.5.5.3	20 to 250 mils	3.2" x 3.2"	1 MHz
Parallel Plate	IPC 2.5.5.9	20 to 60 mils	2" x 2"	100 MHz to 1.2 GHz
IPC Stripline	IPC 2.5.5.5	60 mils	2" x 2.75"	10 GHz
Bereskin Stripline	-	20 - 62 mils	4" x 1.125	2 - 15 GHz
Split Post Cavity	IPC 2.5.5.13	30 mils *	2" x 2.75"	1 GHz - 35 GHz**

All Test Methods are run using samples with no copper
* The sample thickness for the Split Post Cavity Test Method is dependent on the testing frequency
** Isola currently tests SPC at 3, 5 , 7 and 10 GHz

- Different Test Methods will give varying **Dk Df** results on the same resin system
- Sample thickness and preparation are critical. Stacking of thin cores is not recommended.
  Air entrapment between samples will result in incorrect data.
- When comparing data sheets test methods need to be the same in order to compare **Dk and Df** values.

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Test Method -Dk Df Comparison

Test Method	Frequency (GHz)	GETEK	FR408	IS415	IS620
Split Post Cavity Dielectric Constant (Dk)	2 GHz	3.63	3.65	3.70	3.62
	5 GHz	3.62	3.65	3.70	3.58
	10 GHz	3.60	3.63	3.68	3.59
Bereskin Stripline Dielectric Constant (Dk)	2 GHz	3.63	3.67	3.72	3.63
	5 GHz	3.61	3.66	3.71	3.59
	10 GHz	3.60	3.65	3.70	3.59

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Test Method -Dk Df Comparison

Test Method	Frequency (GHz)	GETEK	FR408	IS415	IS620
Split Post Cavity Dissipation Factor (Df)	2 GHz	0.0099	0.0084	0.0095	0.0044
	5 GHz	0.0102	0.0089	0.0096	0.0050
	10 GHz	0.0110	0.0089	0.0096	0.0053
Bereskin Stripline Dissipation Factor (Df)	2 GHz	0.0140	0.0120	0.0129	0.0060
	5 GHz	0.0141	0.0127	0.0130	0.0066
	10 GHz	0.0141	0.0125	0.0130	0.0071

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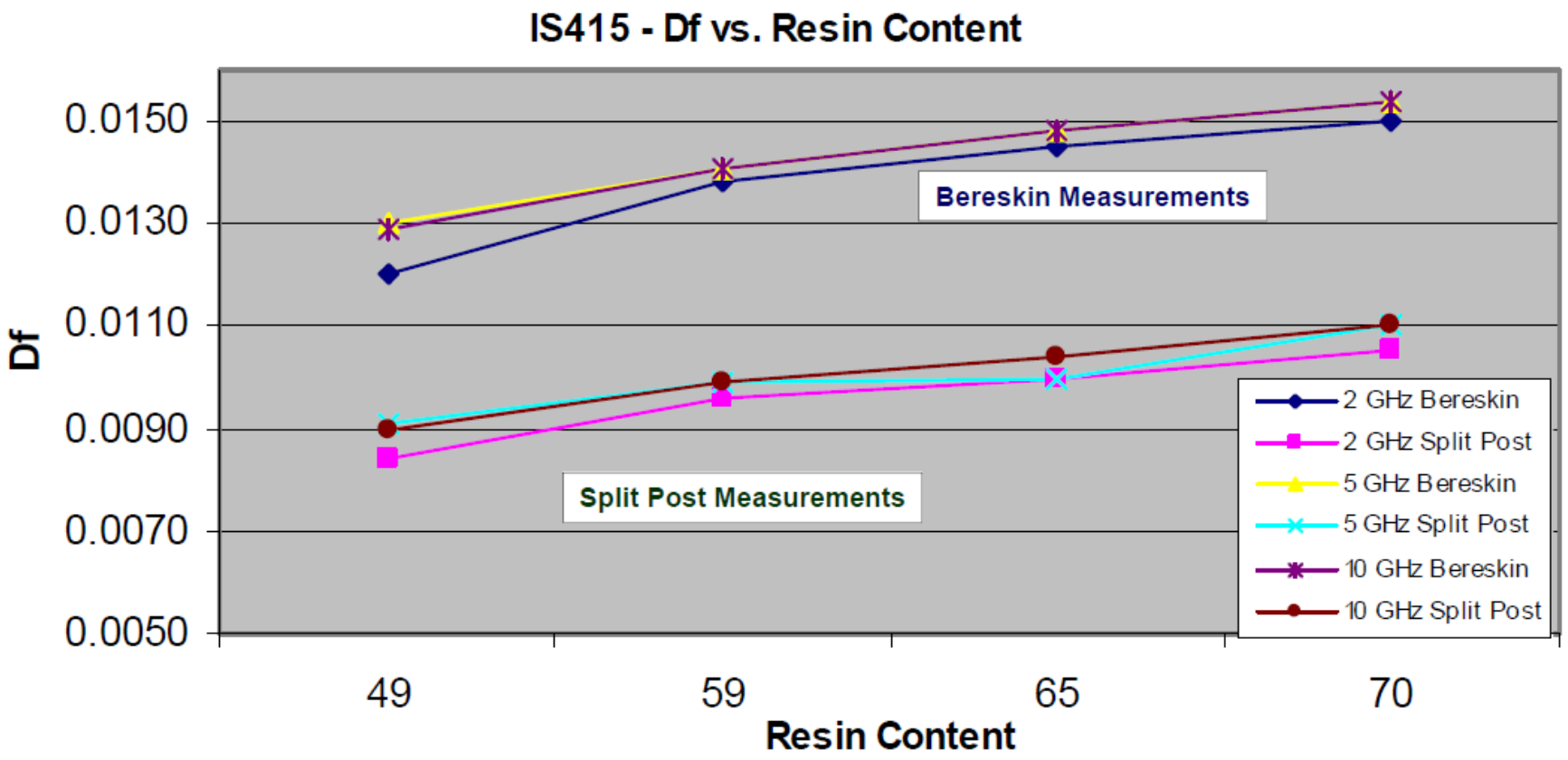
IS415 Df at 2, 5 and 10 GHz
Bereskin Stripline vs Split Post Cavity Test Method



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Summary

Selecting a laminate material is a balancing act.

- Simple substitution by core thickness is not advised
- Use accurate data for modeling
- Use simulation tools to understand changes in stack-up and resulting material properties
- Know your (or your customers) needs in detail

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Typical IS4150 .127mm Core Constructions

Core/ Construction

0.127mm	Resin %
1 x 2116	54 %
2 x 1080	57 %
2 x 1067	70 %

- Dk / Df differences based on **retained** resin %. In this example it is 16 %

At 5 GHz Dk at 54 % = 3.73	Df at 54 % = 0.0130
At 5 GHz Dk at 70 % = 3.38	Df at 70 % = 0.0149

- It is critical that the right core thickness/ construction is used by the OEM/ Designer to meet the impedance criteria.

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Isola

Products

Light version

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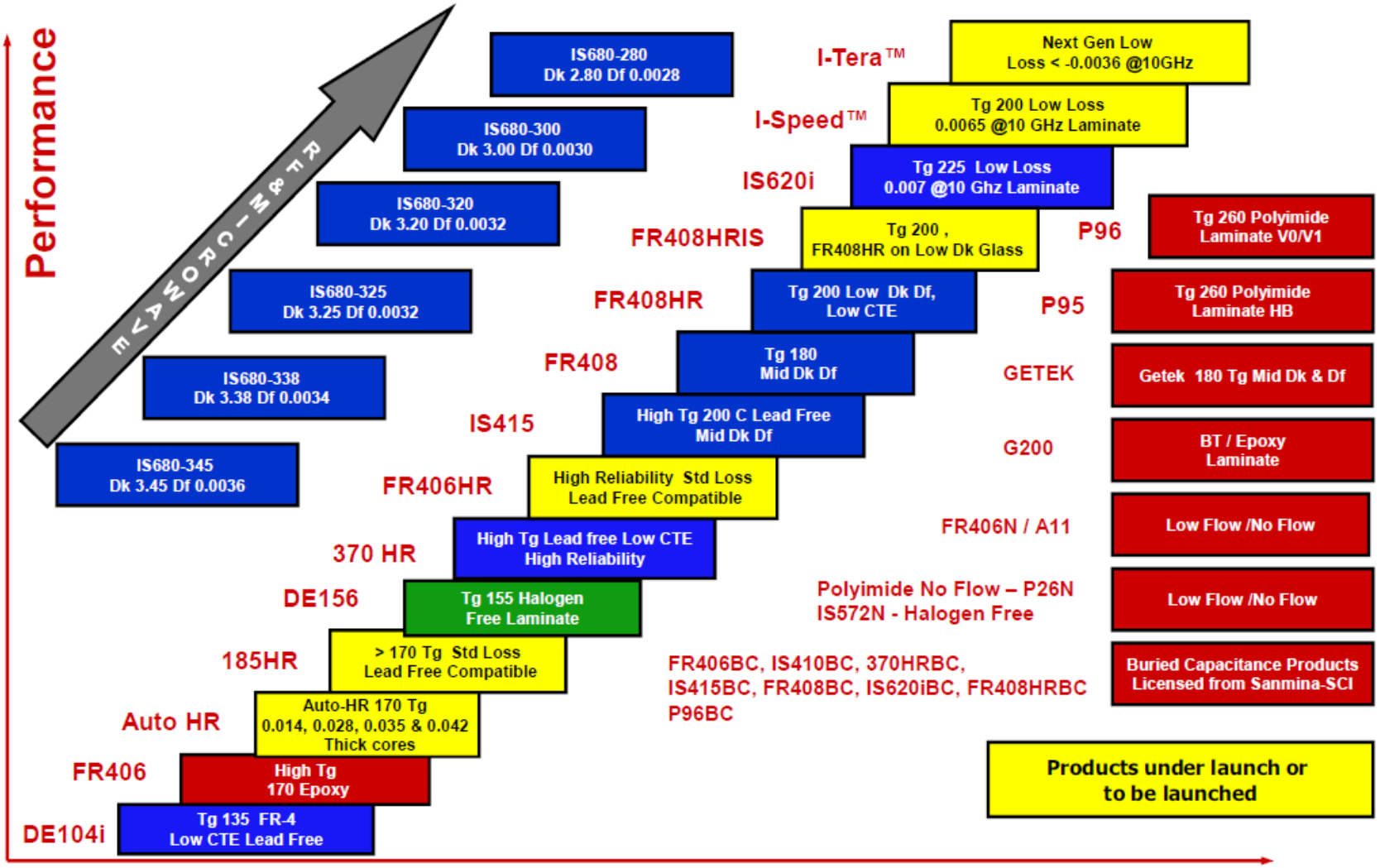
Product Offering



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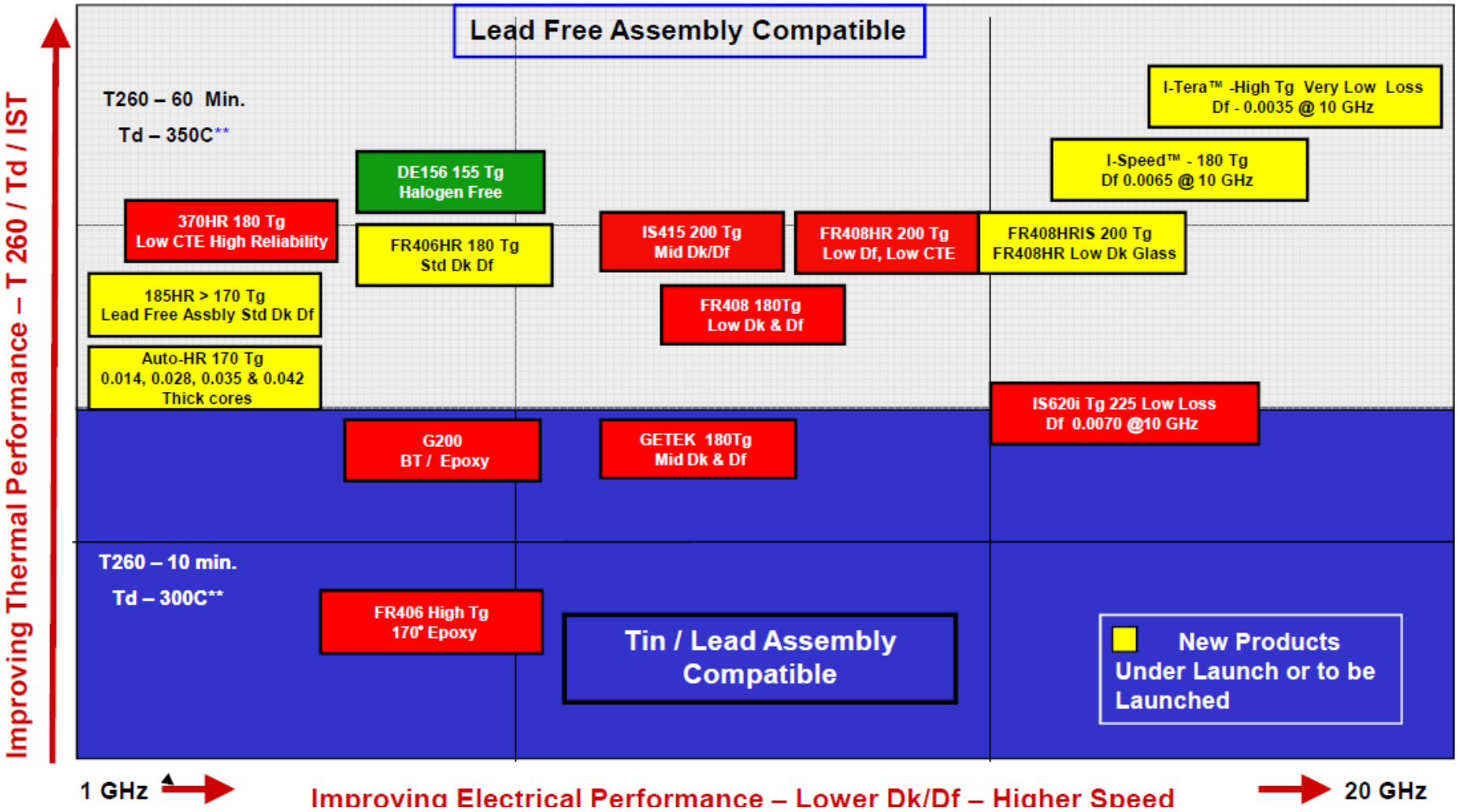
Isola Product Positioning



** Laminate Data -IST performance is a function of Hole diameter, board thickness, plating parameters and laminate attributes. Peed is a function of design such as line length etc.

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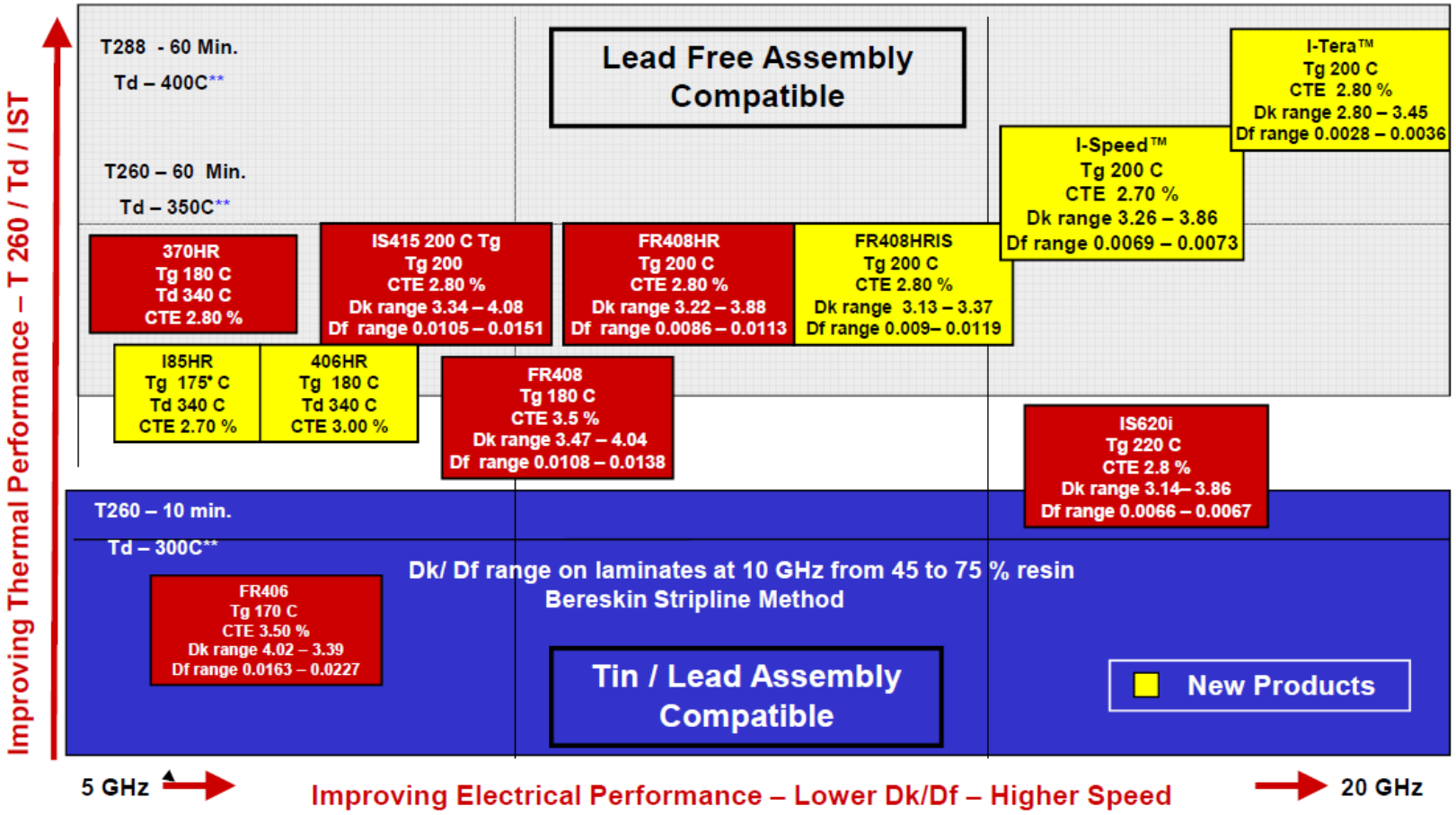
ISOLA HSD Products



** Laminate Data -IST performance is a function of Hole diameter, board thickness, plating parameters and laminate attributes. Speed is a function of design such as line length etc.

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Isola High Speed Digital Comparison Data

Property	Units	IS415	FR408	FR408HR	FR408HRIS	I-Speed™	I-Tera™
Tg C	Degree C	200	180	200	200	180 C	200
Td @ 5 % wt loss	Degree C	370	360	360	360	360	360
CTE z-axis (50 to 260 C)	ppm/ C	2.80 %	3.50 %	2.80 %	2.80 %	2.70%	2.80 %
CTE x-y axis pre-Tg	ppm/ C	13	13	13	13	13	12
CTE x-y axis post Tg	ppm/ C	14	14	14	14	14	13
T-260 (TMA)	minutes	60	60	60	60	60	> 60
T-288 (TMA)	minutes	> 20	> 20	> 30	> 30	> 60	> 60
Dk @ 2 GHz	-	3.72	3.67	3.66	3.39	3.64	3.00
Dk @ 5 GHz	-	3.71	3.66	3.65	3.38	3.63	3.00
Dk @ 10 GHz	-	3.71	3.65	3.64	3.37	3.63	3.00
Df @ 2 GHz	-	0.0134	0.0120	0.0090	0.0088	0.0060	0.0035
Df @ 5 GHz	-	0.0136	0.0127	0.0096	0.0094	0.0067	0.0035
Df @ 10 GHz	-	0.0136	0.0125	0.0094	0.0092	0.0071	0.0035
Typical Data Rates Gb/ sec		5	5	10	10	15	20
Elelctrical Strength	volts/ mil	1100	1400	1700	1700	1700	1200
Peel Strength RTF H oz foil	lb/ in	6.5	6.5	6.5	6.5	6.5	4.0
Peel Strength - after Thermal Stress	lb/ in	7.0	7.0	5.5	5.5	5.5	4.0
Flammability		V-0	V-0	V-0	V-0	V-0	V-0
Moisture Absorption	%	0.15	0.15	0.061	0.061	0.06	0.016
Slash Sheets IPC 4101	Rev C	/21 /24 /26 /28 /121 / 124 / 129	/21 '/24 /121 / 124	/21 /24 /121 /124 /129	/21 /24 /121 /124 /129	/21 /24 /121 /124 /129	IPC 4103 / 17
ZBC 2000 *		Yes	Yes	Yes	Yes	No	No

Test data on core material
Dk Df data by Bereskin Stripline Test Method
Data Rates are listed as those used on current production boards using a particular Isola product.
* ZBC 2000 is licensed from Sanmina SCI

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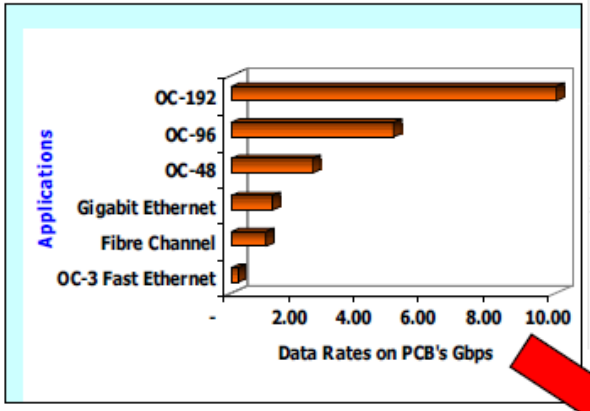
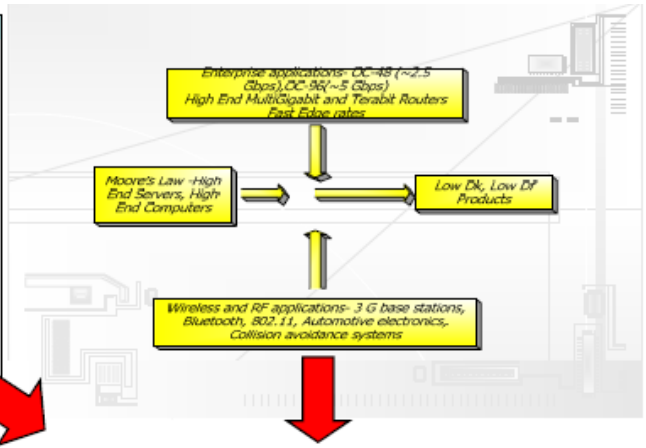
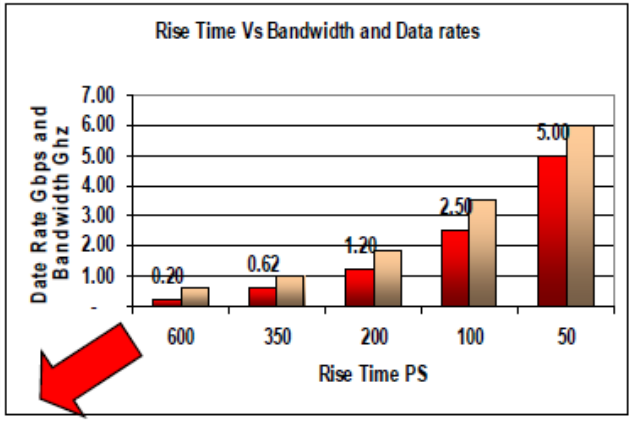
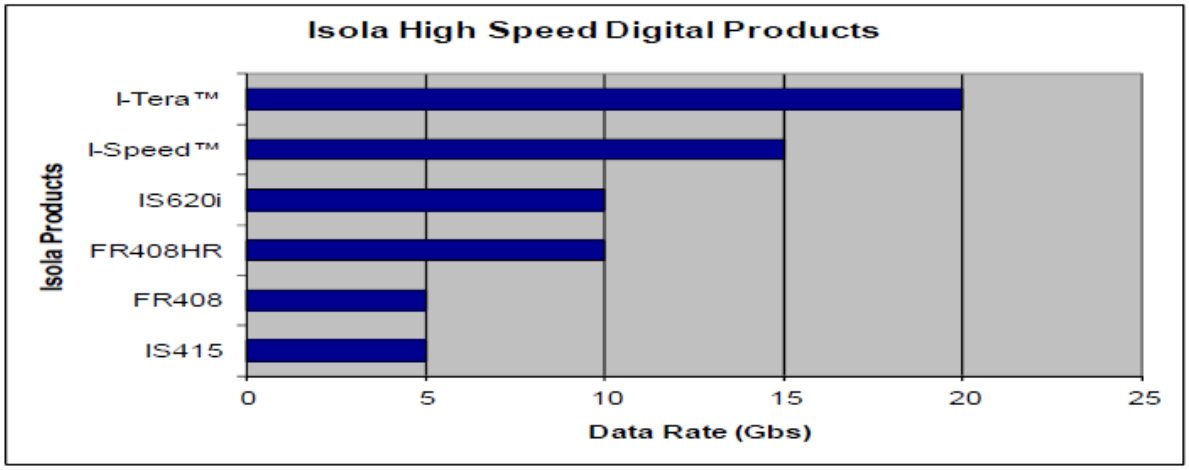
High Speed Digital Roadmap







Trends – Faster edge rates, Rising Bandwidths, Enterprise applications, High end computing driving the need for low Dk/DF solution.



Enabling data rates up to and beyond 10 Gbps

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IPC 4101 Rev C Slash Sheet Matrix

I-Tera™ is qualified to IPC 4103 / 17

Isola Product	IPC 4101 C Slash Sheet Certification
A11	/ 20
DE104i	/ 21 / 121
ED130UV	/ 21
FR402 / IS402	/ 21
254	/ 21 / 24
250 HR	/ 21 / 24 / 97 / 101
370 Turbo	/ 21 / 24 / 26 / 121 / 124
IS400	/ 21 / 24 / 97 / 99 / 101
DE117	/ 24 / 26 / 28
FR406	/ 21 / 24 / 26 / 28
FR406BC	/ 21 / 24 / 26 / 28
FR406N	/ 24 / 26 / 28
IS410	/ 21 / 24 / 26 / 28 / 121 / 124 / 129
IS410BC	/ 21 / 24 / 26 / 28 / 121 / 124 / 129
185HR	/ 21 / 24 / 26 / 98 / 99 / 101 / 126
370HR	/ 21 / 24 / 26 / 98 / 99 / 101 / 126
370HR BC	/ 21 / 24 / 26 / 98 / 99 / 101 / 126
FR406HR	/ 21 / 24 / 26 / 28 / 121 / 124 / 129
IS415	/ 21 / 24 / 26 / 28 / 121 / 124 / 129
IS415 BC	/ 21 / 24 / 26 / 28 / 121 / 124 / 129
IS420	/ 98 / 99 / 101
DE156	/ 94
GETEK	/ 25
FR408	/ 24 / 121 / 124
FR408BC	/ 24 / 121 / 124
FR408HR	/ 21 / 24 / 121 / 124 / 129
FR408HRIS	/ 21 / 24 / 121 / 124 / 129
I-Speed™	/ 21 / 24 / 121 / 124 / 129
G200	/ 30
IS620/ IS620i	/ 30
IS620BC	/ 30
P-95 & P25	/ 40 / 41 / 42
P-96 & P26	/ 40 / 41 / 42
P96 BC	/ 40 / 41 / 42

For dedicated material information look at: Isola-group.com

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IPC 4101C – Lead Free

- **IPC-4101C/99.** High Tg FR-4, inorganic fillers,
- **IPC-4101C/101.** Low Tg FR-4, inorganic fillers,
- **IPC-4101C/102.** PPE (Non FR-4) Extra High Tg, Inorganic fillers
- **IPC-4101C/103.** PPO (Non FR-4) High Tg, Inorganic fillers
- **IPC-4101C/121.** Low Tg FR-4, no fillers,
- **IPC-4101C/122.** Low Halogen, Low Tg, no fillers
- **IPC-4101C/124.** High Tg FR-4, no fillers,
- **IPC-4101C/125.** Low Halogen, High Tg, no fillers,
- **IPC-4101C/126.** Very high Tg, inorganic fillers, CAF
- **IPC-4101C/127.** Low Halogen, LowTg, inorganic fillers
- **IPC-4101C/128.** Low Halogen, HighTg, inorganic fillers
- **IPC-4101C/129.** Very high Tg, no fillers, CAF
- **IPC-4101C/130.** Low Halogen, Inorganic filler, CAF
- **IPC-4101C/131.** Low Halogen, no fillers, CAF

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Material Selection guide

Laminate groups

Laminate groups	IPC4101C	Min Tg	Min Td	Max CTE
Low Tg	101/121/122*/127*	110	310	4,00 %
High Tg	99/103/124/125*/128*	150	235	3,50 %
Very high Tg	126/129/130*/131*	170	340	3,00 %
Extra high Tg	102	185	340	2,8 %

* Low halogen materials

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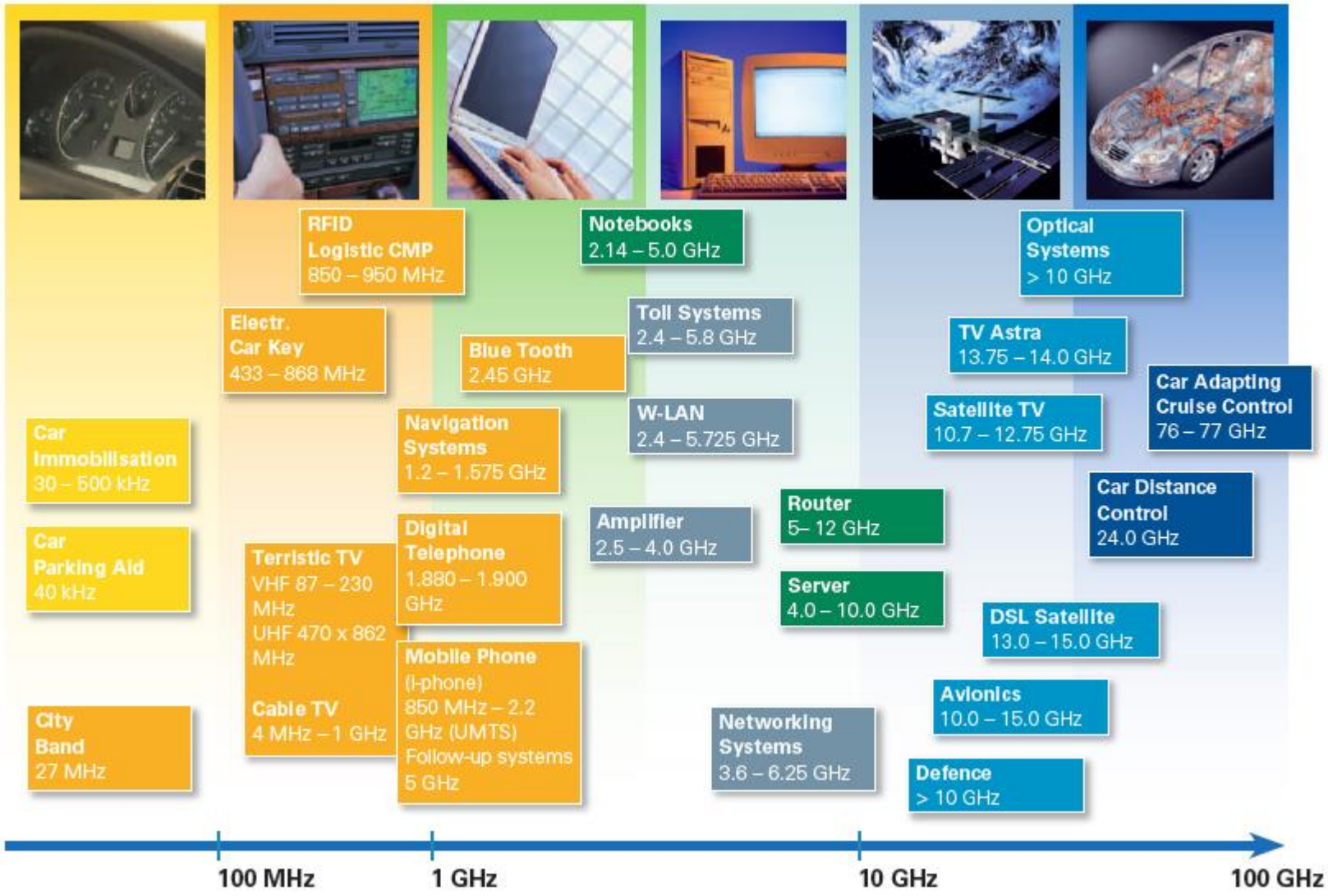
Medium to High Frequency Applications



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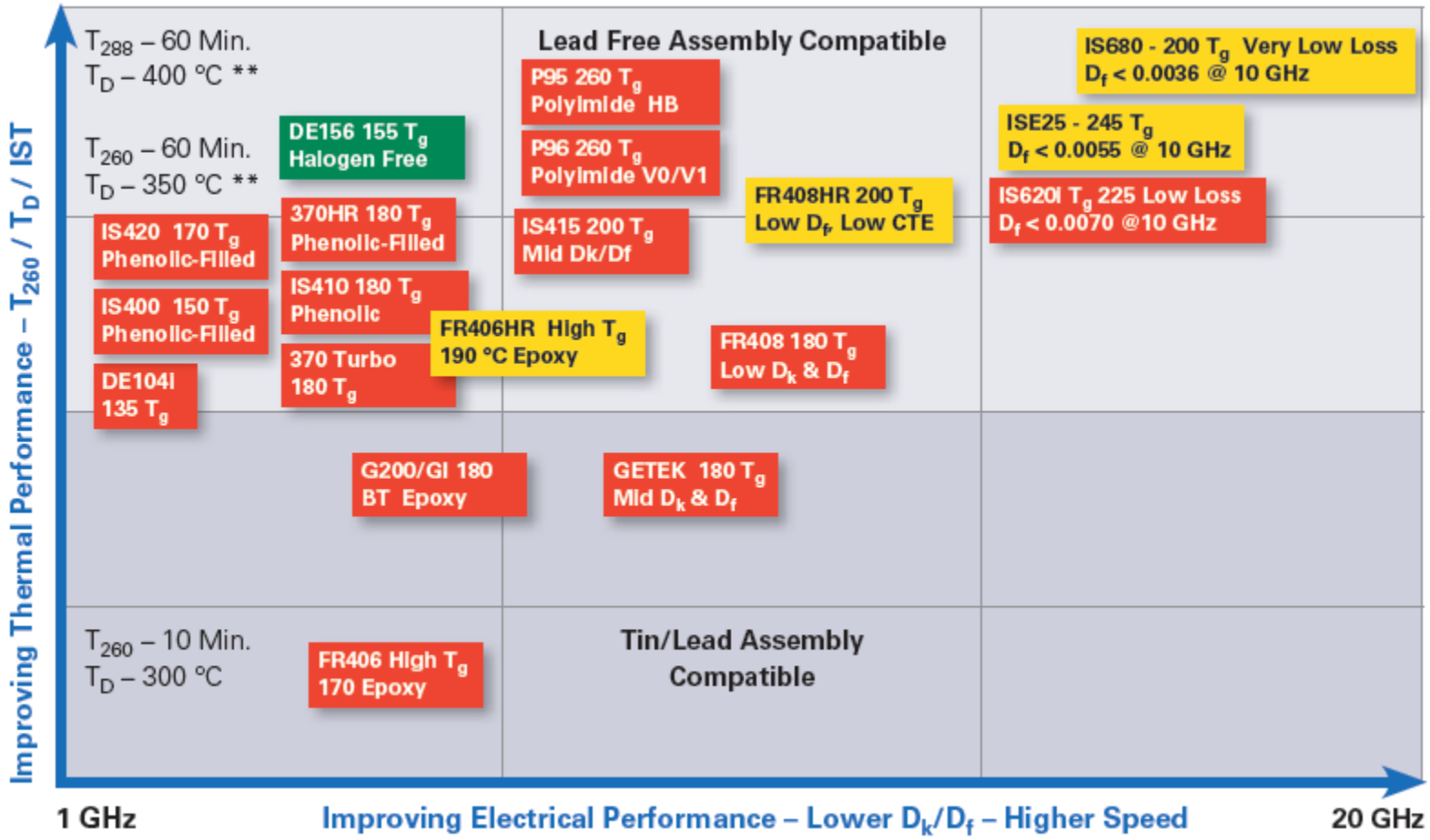
Speeding up your products…



** *Laminate Data - IST performance is a function of Hole diameter, board thickness, plating parameters and laminate attributes.*

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Laminate - manufacturers we see, ..frequently

Arlon	Berquist	Dosan
DuPont	EMC	Espanex
Grace	Innox	Isola
Iteq	Kingboard	Laird
Lamitec-Dielektra	Mitsubishi	Nam Hing
Nanmei	Nanya	Nelco
Panasonic	PIC	Rogers
Shengyi	Shinemore	Sumitomo
Taconic	TUC	Ventec

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more…. **MATERIALS**

self study

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General characteristics of laminates

All of the basic materials mentioned, which are used by Elmatica, comply with the current versions of the following international standards:

Material	Standard
Base material for rigid circuit boards, 1 and 2 sided, multilayer	IPC-4101
Base material for HF applications	IPC-4103
Laminated copper films for flexible printed circuits	IPC-4204
Flexible adhesive coated films for flexible printed circuits	IPC-4203

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General characteristics of laminates

Thermal characteristics:

The key parameters are less the glass transition temperature Tg, but rather the delamination time at 260° C and 288° C, the coefficient of thermal expansion (CTE) along the X, Y & Z axes, and susceptibility to thermal cycle tests.

The increased soldering temperature for lead-free solder means an increase in the thermal stress on the printed circuit board, which increases the danger of cracked sleeves, corner cracks, copper lifting and delamination.

Particularly the reliability of printed circuit boards in automotive applications is increasingly checked using cyclical temperature tests.

Typical conditions for this are -40C to +125° C / >500 cycles or –40° C to +140° C / 1000 cycles. This performance is only provided by materials with limited expansion along the Z axis, in other words with a low CTE (z).

While the Tg can only serve as a guideline for a permanent thermal stress of the printed circuit board (approx. 20° C - 25° C below the Tg), the other characteristics mentioned, especially the CTE(z) are the relevant values when considering the reliability of the circuit.

"Modern" FR4 substrates using an FR4 resin system have these characteristics, but only have a Tg of 140° C - 150° C.

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General characteristics of laminates

Electrical characteristics:

--Dielectric constants (related to a defined frequency, mostly specified at 1 MHz, 1 GHz and 10 GHz)
-- Loss angle (related to a defined frequency - see above)
-- Proof voltage
-- Resistivity
-- Surface resistance
-- CTI (Conductive Tracking Index), describes the susceptibility to tracking current
-- CAF resistance (conductive anodic filament - electromigration between vias)

Mechanical characteristics:

-- Adhesion of the Cu foil
-- Bending strength
-- Elasticity

Other characteristics:

--Water absorption
--Density

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Values for a few selected typical groups of materials

Materials group	Tg	CTEz	ε_r(1 MHz/1 GHz/10 GHz)	Proof voltage	Surface resistance	Conductive Tracking Index (CTI)	Water absorption	Cu adhesion
	°C	ppm/K	-	KV/mm	MΩ	V	%	N/mm
Standard FR4	125°C-140°C	<70	4,7/4,3/-	50	10^7	>200	0,06	1,5
Modified FR4	135°C-180°C	<55	4,6/4,2/-	45	10^7	>200	0,06	1,5
FR4 halogen free	150°C-170°C	<40	5,0/4,8/4,6	50	10^8	>500	0,06	1,5
BT epoxy	Approx. 200°C	<40	4,4/4,1/-	70	10^8	>200	0,05	1,6
CE epoxy	Approx. 250°C	<25	3,9/3,7/3,5	65	10^7	>200	0,05	1,6
Polyimide	220°C-260°C	<55	4,0/3,8/3,8	45	10^8	>100	0,3	1
PTFE (pure)	200°C-230°C	<70	2,6/2,4/2,2	45	10^7	>600	0,04	1,3
RO3000	-	<40	3,0/2,8/2,6	30	10^7	>600	0,1	2,5
RO4000	Approx. 280°C	<45	3,3/3,0/2,8	30	10^9	>600	0,04	1,0

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Example materials for various requirements

Standard applications

Name	Reinforce-ment	Resin	Comment	Examples	Cost factor (reference: FR4 standard) ***
FR2	Paper	Phenol	Low technology, “white goods“, not lead-free solderable	Cobrisol FR2; Aismalibar	0,3
FR3	Paper	Epoxy	Low technology, “white goods“, almost no longer available	Cobrisol FR3; Aismalibar	0,6
CEM1	Paper	Epoxy	Low technology	Cobrisol CEM1;Aismalibar	0,7
CEM3	Glass mat	Epoxy	Low technology	---	0,8
FR4Standard	Glass	Epoxy	Tg 130°C-140°C;conforms to RoHS/WEEE	MC-100 EX*, R-1766; Panasonic	1,0
FR4halogen free	Glass	Epoxy	Thermally very stable,CAF resistant, Tg >= 150°C	DE 156, IS 500; IsolaR-1566W; Panasonic	1,3

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Example materials for various requirements

Use at high temperatures

Name	Reinforce-ment	Resin	Comment	Examples	Cost factor (reference: FR4 standard) ***
FR4 medium Tg	Glass	Epoxy	Tg approx. 140-160°C, increased thermal stability, low Z axis ex-pansion, high reliability for lead-free soldering process, often CAF resistant	R-1755C; Panasonic IS 400**; Isola	1,15
FR4 high Tg	Glass	Epoxy	Tg approx. 160-190°C,see aver-age Tg	R-1755S,R-1755T, Panasonic, IS 410**, IS 420**, Isola	1,4
Rigid PI	Glass	Polyim-ide	Tg approx. 260°C, high perform-ance laminate for high reliability and high operating tempera-tures	G 200, P 95, P96;Isola N7000 se-ries; Nelco	5
CE	Glass	Cyanate ester	Tg approx. 250°C, use is rapidly declining, replace by high Tg FR4 and PI materials	N8000 series; Nelco	2,5
BT	Glass	Bismale-imide-triazine resin	Tg approx. 200°C, very low ther-mal expansion, use is rapidly de-clining, replace by high Tg FR4 and PI materials	N5000 series; Nelco	2,5

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Example materials for various requirements

Controlled impedance & HF applications

Name	Reinforce-ment	Resin	Comment	Examples	Cost factor (reference: FR4 standard) ***
Teflon	Ceramic filler	PTFE	Suited for machining, assembly of multilayer and hybrid systems possible with FR4	RO3003®;Rogers	4
Teflon	Glass	PTFE	Very low ε_r values, high CTE (z)	RT5870®, RT5880®; Rogers	3
Polymers	Ceramic filler	Duro-plast	Suitability for machining is simi-lar to FR4, assembly of multilay-er and hybrid systems possible with FR4	RO4003C®**, RO4350®**; Rogers, 25N**; Arlon	3,5
Various	Glass	Epoxy	Low and constant ε_r values and loss angle, high Tg, thermal per-formance and suitability for ma-chining are similar to FR4	IS620, IS640; Isola	3

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Example materials for various requirements

Flexible applications

Name	Reinforce-ment	Resin	Comment	Examples	Cost factor (reference: FR4 standard) ***
Polyimide with acrylic adhesive	---	---	For dynamic flexible applica-tions, adhesive has a very large CTE(z)	Pyralux® LF/FR se-ries**; DuPont	5
Polyimide with epoxy adhesive	---	---	For semi-dynamic and static flexible applications	Teclam® series*; DuPont Akaflex® series*; Krempel	3
Adhesive free polyimide	---	---	For dynamic flexible applica-tions, good thermal perform-ance	Espanex series*; Nippon Steel AP se-ries®**; DuPont	5-6
LCP (Liquid Crystal Poly-mer)	---	---	For dynamic, flexible applica-tions, very good thermal per-formance, low water absorp-tion, also suited for HF applica-tions in the high GHz range	R/flex®3600, R/flex®3850; Rogers	8-10

There is no universal base material for printed circuit boards. Whether for standard applications, HF, high temperature or other applications: A large number of substrate types is available.
For further technological questions concerning circuit boards, please contact your Elmatica team.

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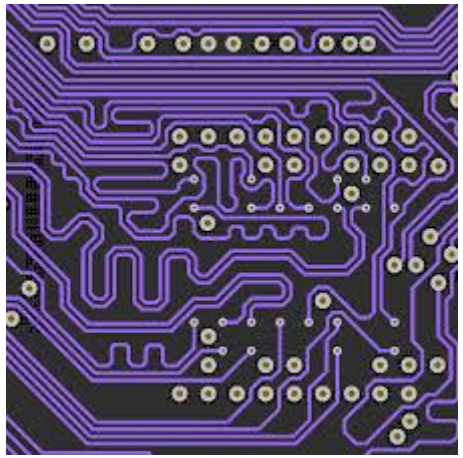

Design Rules, design aspects, errors seen.

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Some GOOD safe values from a typical manufacturer

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Cost Considerations

The following list presents some general rule-of-thumb trade-offs that will provide the most cost effective, high performance and/or high density interconnect solution.

- Use the least amount of layers
- Use a smaller line width/space before adding layers

- Investigate how boards will fit into a production panel to ensure that maximum material utilization occurs.

- Ensure that the optimum material stackup, construction, is being used. Let your manufacturer perform this analysis.

- Smaller holes before adding layers. Down to 0.25mm and a (8) 10:1 aspect ratio.
- Use blind vias before buried vias.

- Use high frequency materials only between the layers where it is required. Do not change all layers to the high performance materials unless it is required. Warp & Twist to be considered.

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Some GOOD safe values from a typical manufacturer

Drill hole Aspect ratio chart

START BOARD THICKNESS	MINIMUM DRILLED HOLE DIAMETER	ASPECT RATIO
0.3mm	0.15mm	2.0 : 1
1.6mm	0.20mm	8.0 : 1
2.4mm	0.30mm	8.0 : 1
3.2mm	0.35mm	10.7: 1
4.0mm	0.50mm	8.0 : 1
5.0mm	0.50mm	10.0: 1

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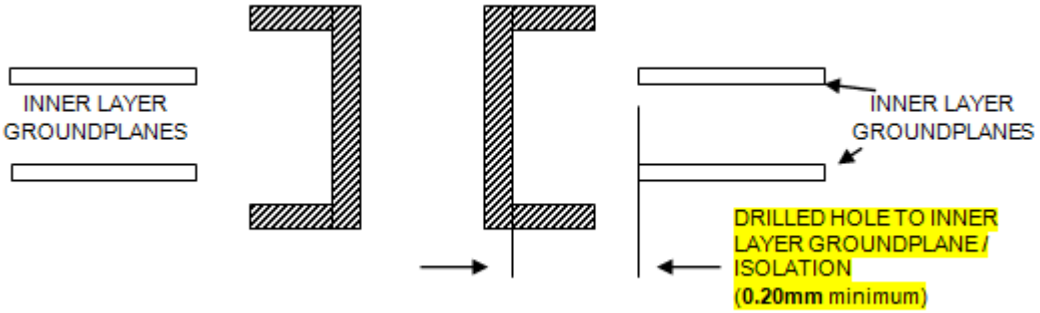
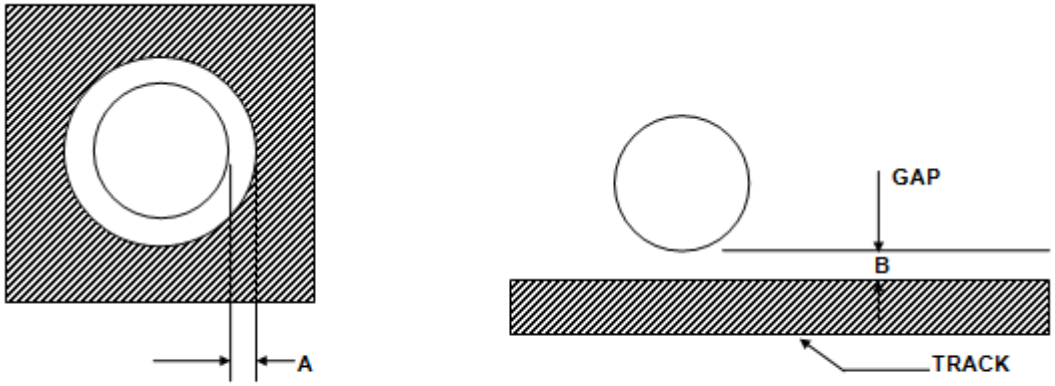
PTH to inner-lay er plane isolation



Non plated holes in copper lands



A	0.30mm MIN
B	0.20mm if no greater than 20% of the hole circumference

Solder resist clearance

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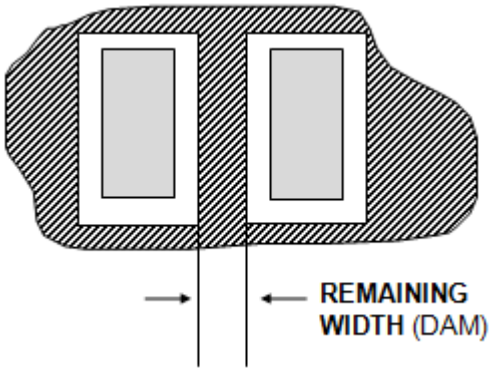
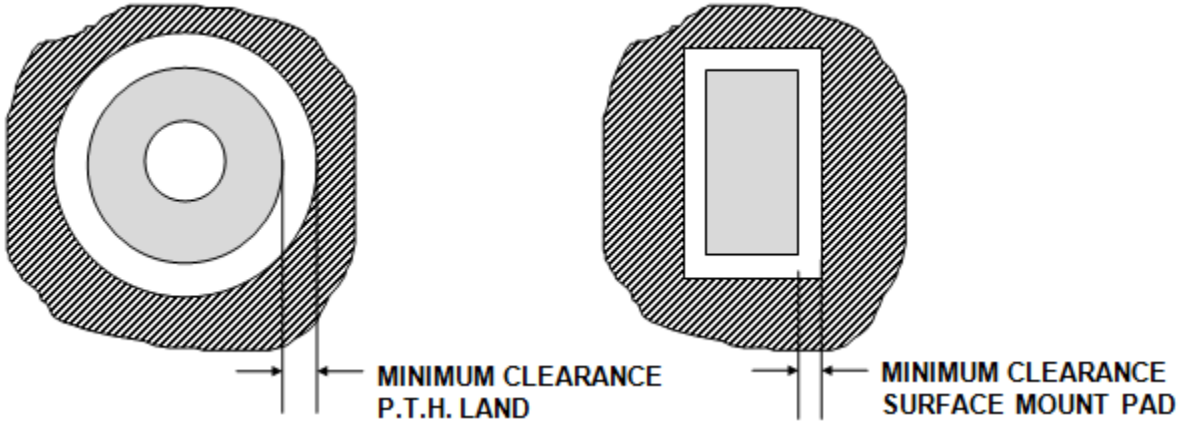
REMAINING WIDTH



SOLDER RESIST TYPE	COLOUR	MINIMUM WIDTH
LIQUID PHOTOIMAGEABLE	GREEN	0.076mm
LIQUID PHOTOIMAGEABLE	RED	0.101mm
LIQUID PHOTOIMAGEABLE	BLUE	0.101mm
LIQUID PHOTOIMAGEABLE	WHITE	0.127mm
LIQUID PHOTOIMAGEABLE	BLACK	0.127mm

CLEARANCE AROUND COMPONENT LAND



SOLDER RESIST TYPE	MINIMUM CLEARANCE TO PTH LAND	MINIMUM CLEARANCE TO SURFACE
LIQUID PHOTOIMAGEABLE	0.050mm	0.050mm

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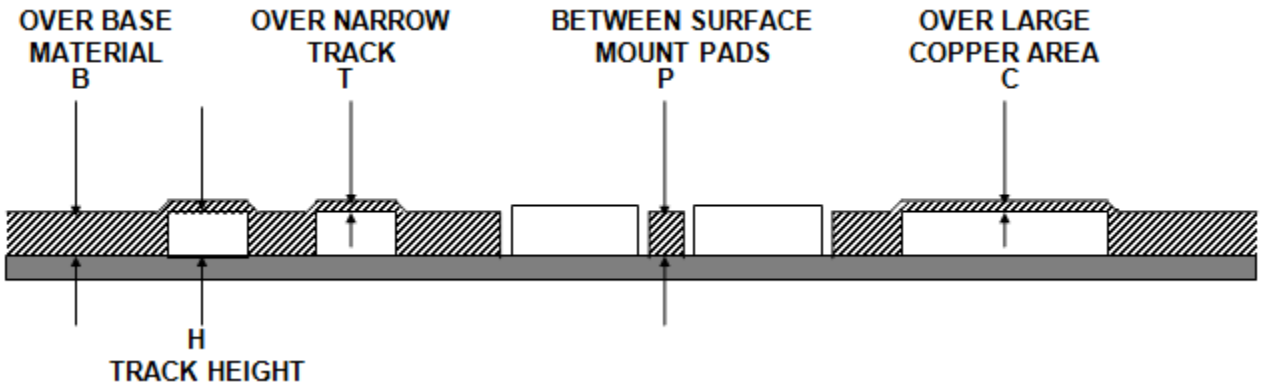
Solder resist thickness



RESIST TYPE	H	B	P	T	C
COATES XV501 T4 (Screen Print)	35um	20um	35um	19um	20um
	45um	20um	45um	18um	20um
	60um	20um	60um	17um	20um
COATES XV501 T4 (Curtain Coat)	35um	35um	35um	16um	30um
	45um	35um	37um	12um	30um
	60um	35um	40um	8um	30um

Photoimageable solder resist for screen print application: - Coates Red, Blue, White and Black inks.

We often specify soldermask thickness between 8-30um acc. to IPC.

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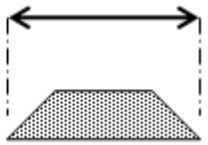
Etch factors

INNER LAYERS – Add minimum after etch allowance

BASE COPPER THICKNESS		ETCH FACTOR	
09um	(0.25oz)	0.004mm	Per Side
12um	(0.3oz)	0.004mm	Per Side
17um	(0.5oz)	0.00625mm	Per Side
35um	(1.0oz)	0.0125mm	Per Side
70um	(2.0oz)	0.025mm	Per Side
105um	(3.0oz)	0.0375mm	Per Side
140um	(4.0oz)	0.0500mm	Per Side

NOTE: Measurement taken at base width due to Impedance calculation.

CROSS SECTIONAL VIEW



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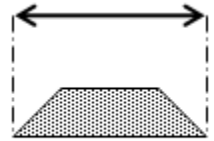
OUTER LAYERS – Add minimum after etch allowance



CROSS SECTIONAL VIEW

BASE COPPER THICKNESS		ETCH FACTOR	
09um	(0.25oz)	0.00625mm	Per Side
12um	(0.3oz)	0.00625mm	Per Side
17um	(0.5oz)	0.0125mm	Per Side
35um	(1.0oz)	0.025mm	Per Side
70um	(2.0oz)	0.05mm	Per Side
105um	(3.0oz)	0.075mm	Per Side
140um	(4.0oz)	0.10mm	Per Side

NOTE1: Measurement taken at base (se diagram below.

Minimum Track/Start copper thickness

START COPPER	MINIMUM TRACK OUTERS	MINIMUM TRACK INNERS	MINIMUM GAPS OUTERS	MINIMUM GAPS INNERS
09um (0.25oz)	0.075mm	0.065mm	0.075mm	0.065mm
12um (0.25oz)	0.075mm	0.065mm	0.075mm	0.075mm
17um (0.5oz)	0.100mm	0.075mm	0.100mm	0.100mm
35um (1.0oz)	0.125mm	0.100mm	0.150mm	0.100mm
70um (2.0oz)	0.200mm	0.15mm	0.250mm	0.200mm
105um (3.0oz)	0.300mm	0.20mm	0.300mm	0.250mm
140um (4.0oz)	0.400mm	0.25mm	0.400mm	0.300mm

NOTE: No Etch Factor allowance has been added to the above figures.

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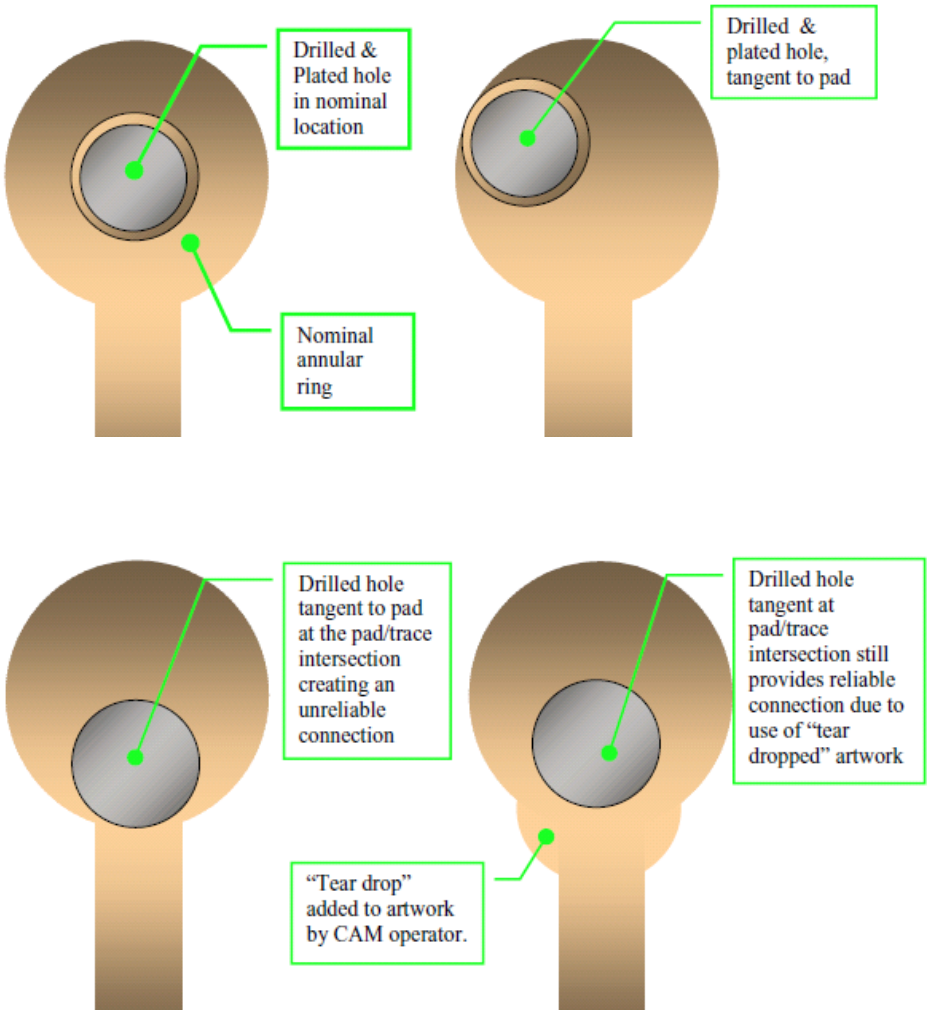
Drill Location and Inner Layer Annular Ring, Drill Tangency, and "Tear Dropped" Artwork



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Breakaway tabs

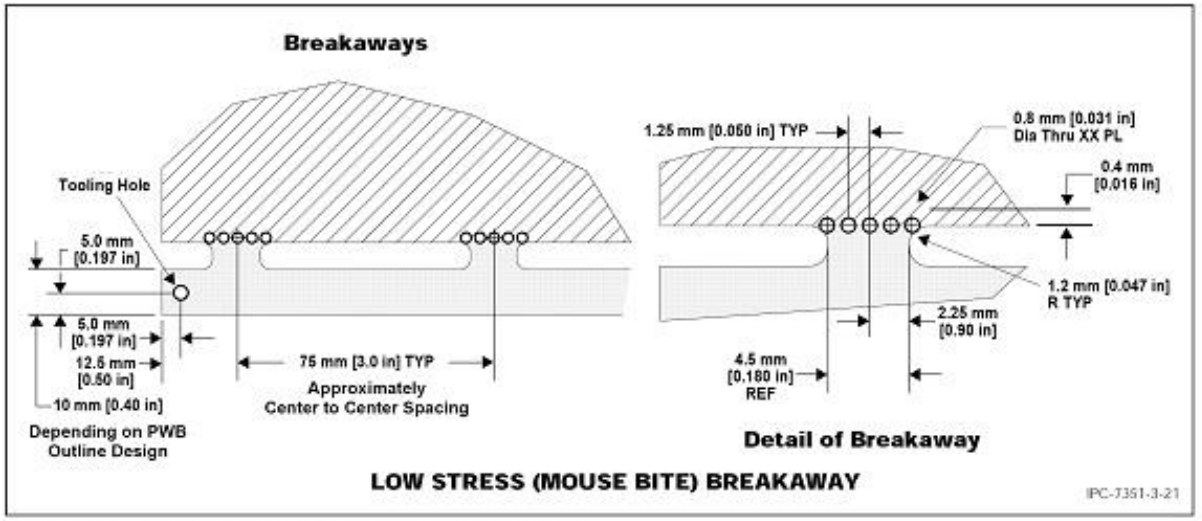
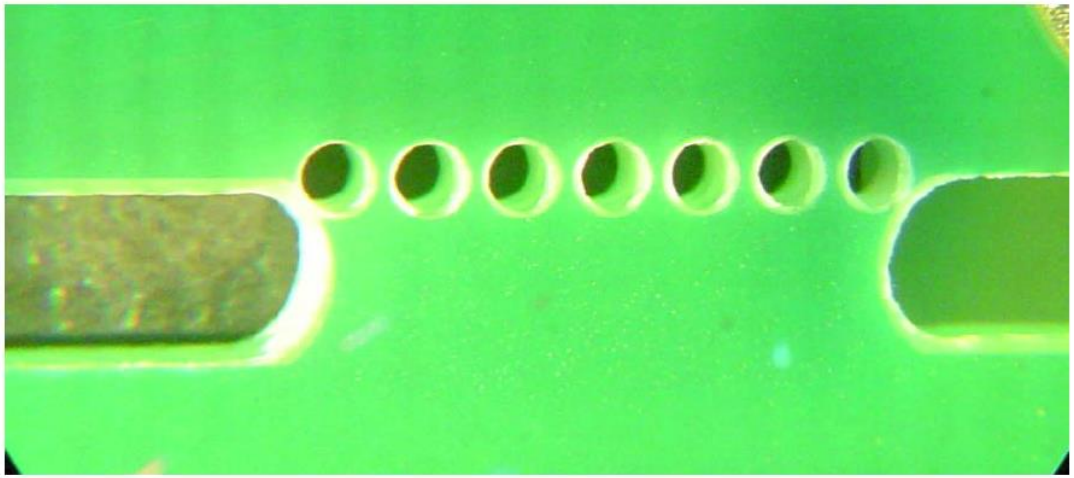


Figure 3-21 Breakaway (Routed Pattern) with Routed Slots



You should consider where to add your tabs. Distance to cu pattern and mechanical need.

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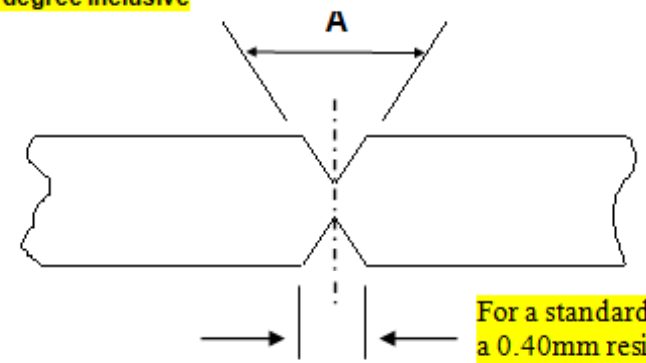
ANGLE OF SCORE (A)

Angle of score 30° degree Inclusive

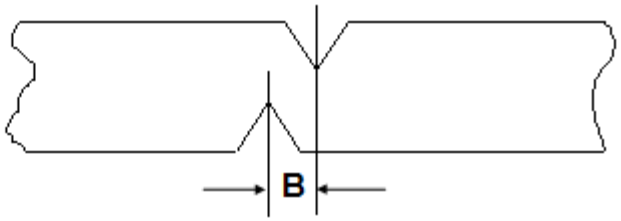


For a standard 1.6mm thick panel, with a 0.40mm residual. The width of score would: -

=2(Tan 15 x 0.6)
=0.32mm (0.01262)

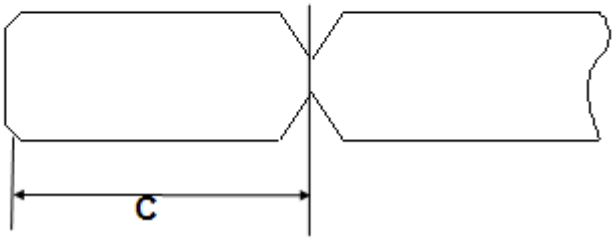
MISREGISTRATION (B)

Misregistration to be **± 0.1mm** (maximum).



POSITIONAL TOLERANCE TO DRILLED HOLE (C)

Positional tolerance from the board edge to be **± 0.2mm.**



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PARALLELNESS

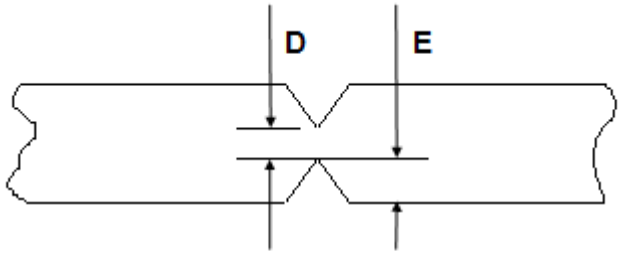
Scores should be parallel to board edge to within **± 0.15mm.**

SCORE DEPTH

Score depth should be such that the residual material is as per the table below.

MATERIAL THICKNESS	0.80mm	1.00mm	1.20mm	1.60mm	2.00mm	2.40mm
RESIDUAL (D)	0.30mm ± 0.1mm	0.35mm ± 0.1mm	0.35mm ± 0.1mm	0.40mm ± 0.1mm	0.40mm ± 0.1mm	0.40mm ± 0.1mm

NOTE 1: Score depths for laminate thickness other than the above should be agreed with the manufacturer



NOTE 2: Minimum score depth **(E)** on either side should be **0.15mm.**

NOTE 3: Score depth **(D)** should be even from side to side to within **0.2mm.**

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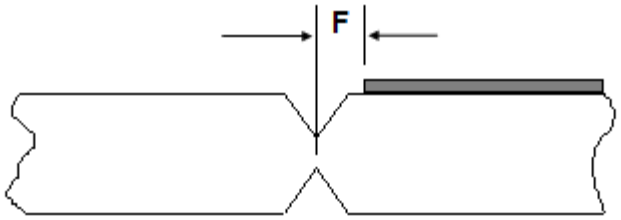
PATTERN CLEARANCE (F)

Minimum distance from centre of score to copper pattern **MUST** not be closer than **0.3mm + HALF WIDTH of top surface score.**



Board Thickness	Top Score Width	Half Top Score Width used in conjunction with Pattern Clearance
1.00 mm	0.16 mm	0.08 mm
1.60 mm	0.32 mm	0.16 mm
2.00 mm	0.43 mm	0.22 mm
2.40 mm	0.54 mm	0.27 mm
3.20 mm	0.75 mm	0.38 mm

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Artwork Design Rules		
Design External Layers (17um copper clad, 1.6mm finished thickness)	Minimum Feature Size um	Preferred Feature Size um
Trace Width	100	127
Trace to Trace Spacing	100	127
Trace to Pad Spacing	100	127
Trace to Plane Spacing	127	200
Trace to Unplated Hole	300	350
Trace to NC Routed Edge	400	500
Trace to Punched Edge	1600	1600
Trace to Scored Edge (Dependent on the angle of the knife)	500	600
Trace to Misc Metal Features (Logo, UL Marking, etc.)	100	500
Pad to Pad Spacing	75	127
Pad Size = FHS + (x.xxx)	250	380
Via Pad Size = FHS +(x.xxx)	250	380
Via Pad to Via Pad Spacing. Pad is SM Covered	75	127
Via Pad to Via Pad Spacing. No SM cover. With SM Web.	250	300
Pad to Plane Spacing	127	200
Pad to NC Routed Edge	400	500
Pad to Punched Edge	1600	1600
Pad to Scored Edge (Dependent on the angle of the knife)	500	600
Unplated Hole Edge to Board Edge	500	1270
Unplated Hole Edge to Unplated Hole Edge. </= 1800 FHS	250	400
Unplated Hole Edge to Unplated Hole Edge. >/= 1800 FHS	250	400

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Internal Layers (Signals) (35um copper clad, 1.6mm finished thickness)		
Trace Width	75	127
Trace to Trace Spacing	75	127
Trace to Pad Spacing	75	127
Trace to Plane Spacing	127	150
Trace to Unplated Hole	250	300
Trace to Routed Edge	400	500
Trace to Punched Edge	1600	1600
Trace to Scored Edge (Dependent on the angle of the knife)	500	600
Trace to Misc Metal Features (Scales, Fiducials, etc.)	100	500
Pad to Pad Spacing	100	150
Pad Size = FHS + (x.xxx)	250	380
Via Pad Size = FHS +(x.xxx)	250	380
Via Pad to Via Pad Spacing	75	127
Pad to Plane Spacing	127	200
Pad to Routed Edge	500	600
Pad to Punched Edge	1600	1600
Pad to Scored Edge (Dependent on the angle of the knife)	500	600

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Internal Layers (Planes) (17 oz. copper clad, 1.6mm finished thickness)		
Plane Clearance = FHS + (x.xxx)	500	635
Pad Size = FHS + (x.xxx)	250	380
Plane to NC Routed Board Edge	500	750
Plane to Scored Edge (Dependent on the angle of the knife)	500	750
Connection Annular Ring = Drill + (x.xxx)	127	150
Solder Mask Clearance		
Liquid Photo Imagable		
Pad Size = External Pad + (x.xxx)	75	127
Pad Size = Unplated Hole + (x.xxx)	127	500
Min. Width (Webbing)	100 (Few can do 75)	127
Legend		
Minimum Height	1000	1500
Minimum Stroke Width	127	150
Legend to Solder Mask Clearance Edge	127	250
Legend to Board Edge	250	500
Preferred Practices		
Via Pad Tear Dropping on all Signal Connections	yes	yes
Breakaway Slot Width (See also IPC-7361-3-21)	800	1600
Breakaway Slot Web Width	500	1000
Smallest Internal Radius	400	800
Nonfunctional pads on Internal Signals	manufacturer choice	manufacturer choice

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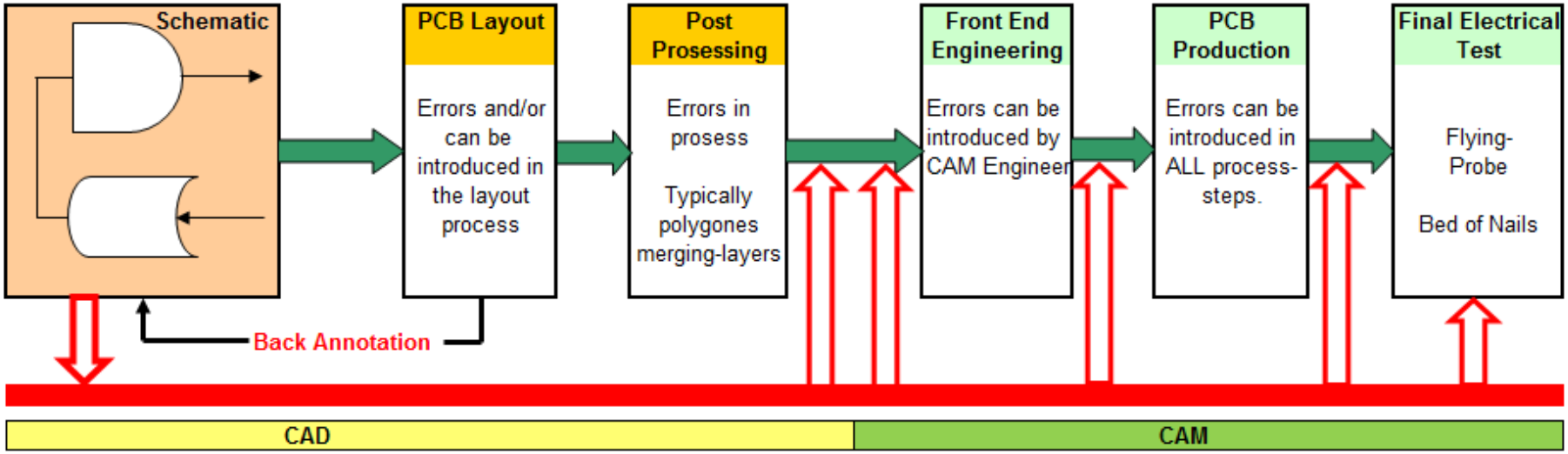
IMPORTANS of NETLIST



Net list format: IPC D-356B

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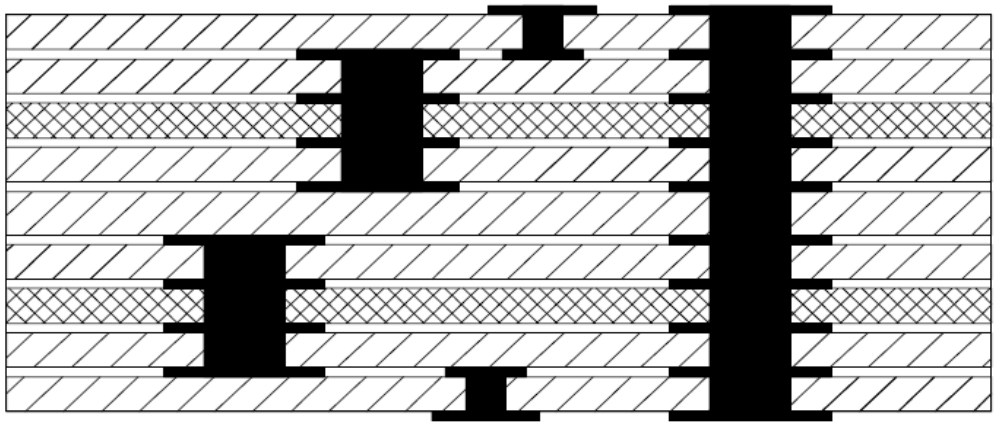
What to do when you need a stack up with impedance requirements:

USAGE		
Components, signals	L1	Prepreg
Signals	L2	Prepreg
GND plane	L3	Core
Signals	L4	Prepreg
GND plane	L5	Prepreg
PWR plane	L6	Prepreg
Signals	L7	Core
GND plane	L8	Prepreg
Signals	L9	Prepreg
Components, signals	L10	



Additional information:

- Final thickness 1.6mm
- Single ended 50 ohms,
- 100 ohms differential,
- Prefered min track width is

Size: 110 x 70mm
routing on Layer 1, 2, 4, 7, 9 & 10
routing on layer 4 and 7.
0.127mm.

Your Manufacturer will supply you a build.

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Changes in physical parameters will affect impedance as follows:

As Physical Values Change	Impedance Will Move
Dielectric Constant (DK) ↓	↑
Dielectric Thickness (h)	↑
Line Width (w) ↓	↑
Line Thickness (t) ↓	↑

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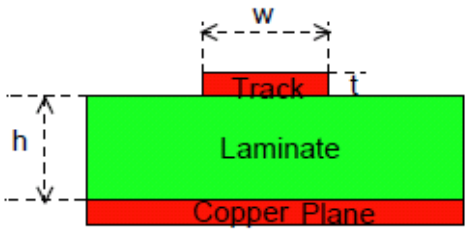
Effect of variables on impedance value.

We can take a simple strip-line configuration, vary one element at a time, and calculate the resulting value.

$$Z_0 = \frac{60}{\sqrt{\varepsilon_r}} \ln\left[\frac{4h}{0.67\pi(0.8w+t)}\right]$$

Er	w	h	t	Zo	Δ	
4.7	0.15 mm	0.5 mm	0.035 mm	50.18 Ω		
4.5				51.29 Ω	+ 1.10	±
4.9				49.15 Ω	- 1.03	2.1%
± 4.3%	0.175mm			46.82 Ω	- 3.36	±
	0.125mm			54.01 Ω	+ 3.82	7.2%
	± 16.7%	0.55mm		52.82 Ω	+ 2.64	±
		0.45mm		47.27 Ω	- 2.92	5.5%
		± 5.0%	0.025mm	52.03 Ω	+ 1.85	±
			0.045mm	48.45 Ω	- 1.73	3.6%
			± 28.6%			



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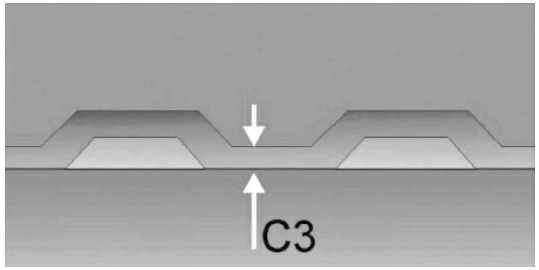
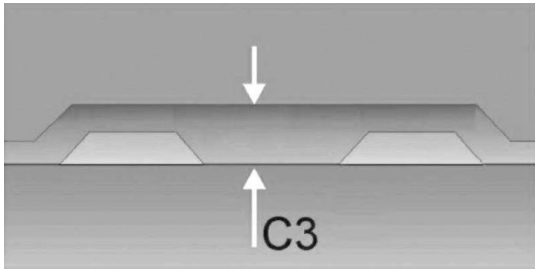
Thickness of coating will influence on impedance

coating is often excluded on RF applications



Substrate 1 Height	H1	4.2500
Substrate 1 Dielectric	Er1	4.2000
Substrate 2 Height	H2	4.2500
Substrate 2 Dielectric	Er2	4.2000
Lower Trace Width	W1	7.0000
Upper Trace Width	W2	6.0000
Trace Separation	S1	3.0000
Trace Thickness	T1	1.2000
Coating Above Substrate	C1	1.0000
Coating Above Trace	C2	1.0000
Coating Between Traces	C3	1.0000
Coating Dielectric	CEr	4.2000
Differential Impedance	Zdiff	85.23



Substrate 1 Height	H1	4.2500
Substrate 1 Dielectric	Er1	4.2000
Substrate 2 Height	H2	4.2500
Substrate 2 Dielectric	Er2	4.2000
Lower Trace Width	W1	7.0000
Upper Trace Width	W2	6.0000
Trace Separation	S1	3.0000
Trace Thickness	T1	1.2000
Coating Above Substrate	C1	1.0000
Coating Above Trace	C2	1.0000
Coating Between Traces	C3	2.2000
Coating Dielectric	CEr	4.2000
Differential Impedance	Zdiff	82.43

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What to do when you need a stack up with impedance requirements: (Cont'd)

Feed back from manufacturer should be:

- **Complete stack up, BOM.**
- **Track width to use on the impedance traces**
- **Space to use between the impedance traces**
- **Calculation result**

Make your critical tracks visible and easy to find

- Use a dedicated D-Code for these traces

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BASIC
Two major applications areas, RF/analog and Digital

The major differences between these two areas are the ability of the PCB involved to tolerate signal losses and the complexity of the PCB.

RF/Analog applications are characterized by the need for **low dielectric losses, low leakage,**
a need for a **low and uniform dielectric constant**
followed by a **low layer count.**

Further, since this type of PCB "tends" to be small, cost of the dielectric material has less effect on overall product cost than on other components.

As a result, using more exotic /expensive materials to meet performance goals is **acceptable**. For this class of PCB, choosing a material based on it's **Dk** characteristics and **Df** losses usually dominates over other considerations.

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Digital applications are characterized by high layer counts, a large numbers of drilled /plated holes, can have buried / blind and small via holes.

The processing costs associated with registering, laminating/bonding many layers, drilling and plating ease, usually dominate the choice of materials.

Absolute dielectric constant value of the insulating material is important, but less important than processing costs and dimensional stability.

As a result, woven glass reinforced materials are nearly always required.
The choice of resin system used with the glass reinforcement is made based on keeping Z-axis expansion within acceptable limits.

The thicker the PCB is, the higher the Tg must be to produce a reliable PCB.
Digital applications are nearly always subjected to pricing pressures, so material choices must be made to just achieve performance requirements without adding extra cost.

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Material Property Comparison between E-Glass and NE-Glass

The primary component of most fiberglass yarns is **E-glass**, S-glass, or **NE-glass.** **E-glass** or "electronic glass" is the primary glass used in yarns that are used to construct fiberglass fabrics, and is the least expensive among the three.

S-glass is generally used for non-electrical applications.

NE-glass has improved electrical and mechanical performance over E-glass and is typical used in the Nelco 4000-13SI and N6000-21SI high-performance laminate product lines.

Property	E-Glass	NE-Glass
CTE (Coefficient of Thermal Expansion) – ppm/C	5.5	3.4
Dielectric Constant (Er) @ 1MHz	6.6	4.4
Dissipation Factor @ 1MHz	0.0012	0.0006

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Skew__

traces that are neither parallel nor intersecting with the glass pattern

- ***Altera*** recommends that you pay close attention to the skew/fiber weave effect for high-speed data rates of 6.375 Gbps and up.

- For identical dielectric materials, wider traces in general show less susceptibility to fiber weave skew compared to narrow traces.

- If possible, use a dense weave (2116) rather than a sparse weave such as 106 or 1080 where this effect is predominant.

- For “marginal” cost increase 25% , move to a better laminate such as Nelco 4000-13 made of NE-glass (lower Er) compared to the regular E-glass (higher Er).

Altera Corporation is a Silicon Valley manufacturer of PLDs, reconfigurable complex digital circuits

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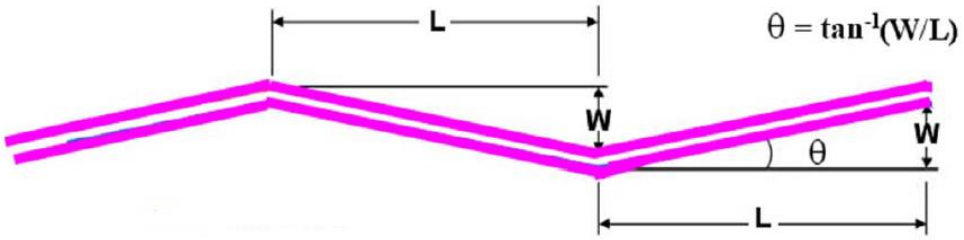
Skew__

traces that are neither parallel nor intersecting with the glass pattern

- Plan the routing on the board in such a way that the routing ends up being at an angle rather than orthogonal.

- Make use of zig-zag routing. The trace can be routed so that it traverses a minimum of 3 times the fiberglass pitch before reversing the direction of routing.
  The drawbacks is the increase in board real estate along with the difficulty associated with routing at arbitrary routing angles other than the typical 0°, 45°, and 90°,



2014 Josse:
Changes in materials will help on, eliminate skew

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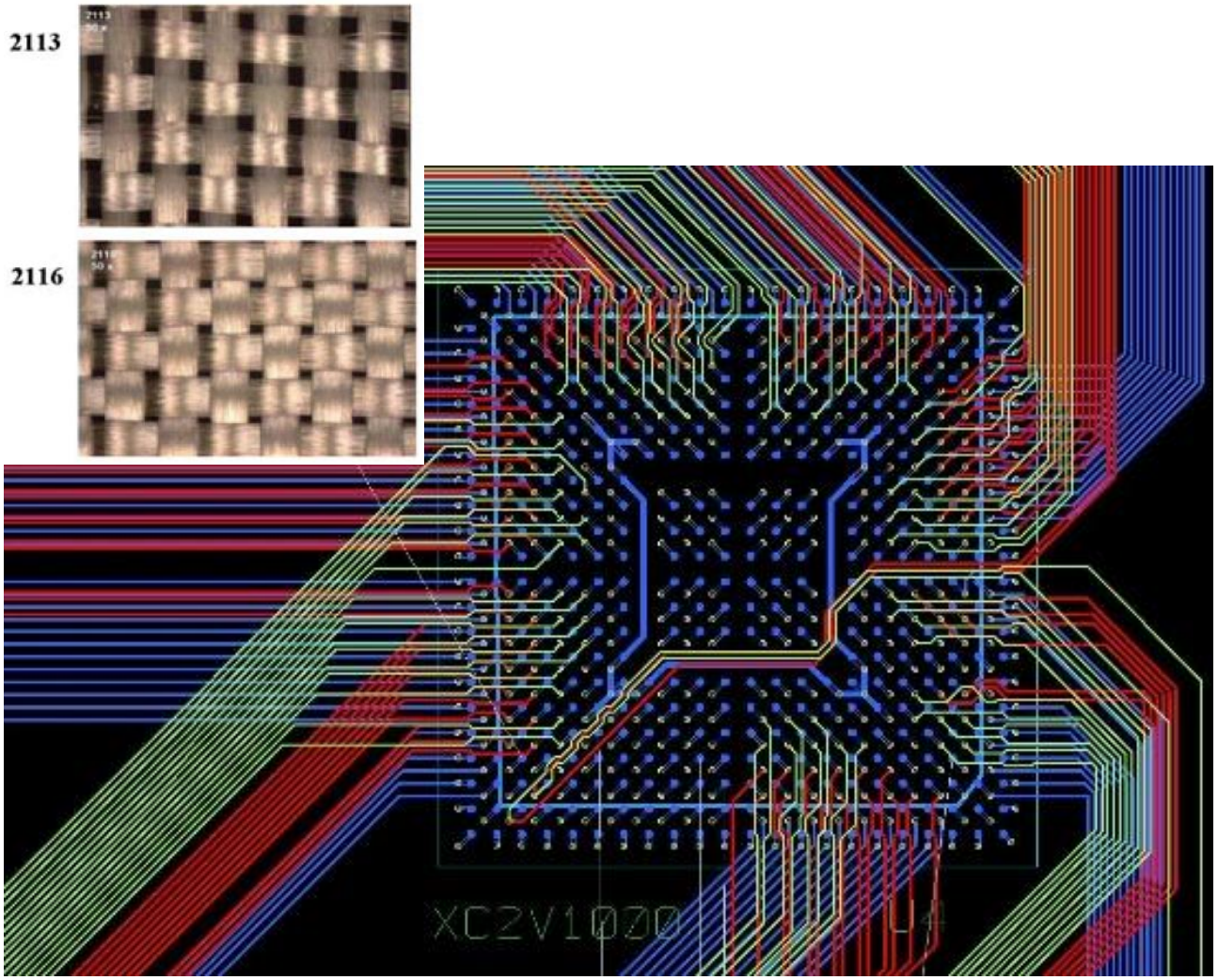

Designers should pay close attention to the layout and the dielectric materials in the PCB design. At high frequencies, dielectric loss is dominant, and is dependent on the dissipation factor (loss tangent) for a given dielectric material. The orientation of the trace with respect to the glass weave determines the amount of skew seen, due to the fiber weave glass pattern.

Prepregs that are more homogeneous , **eg 3313** are available, and more will come…..

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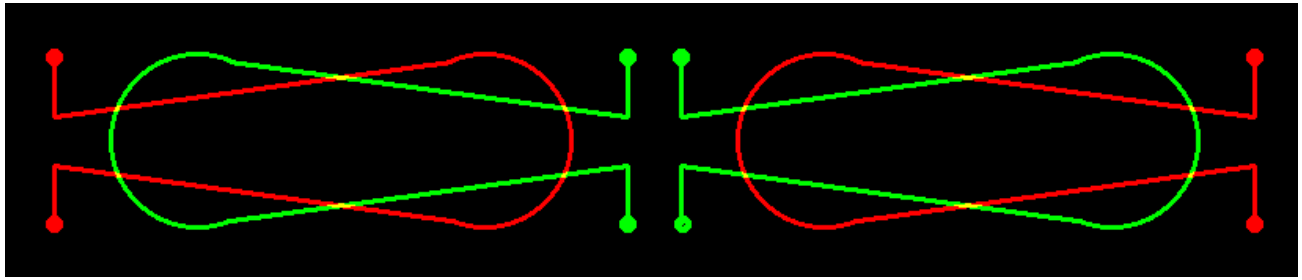
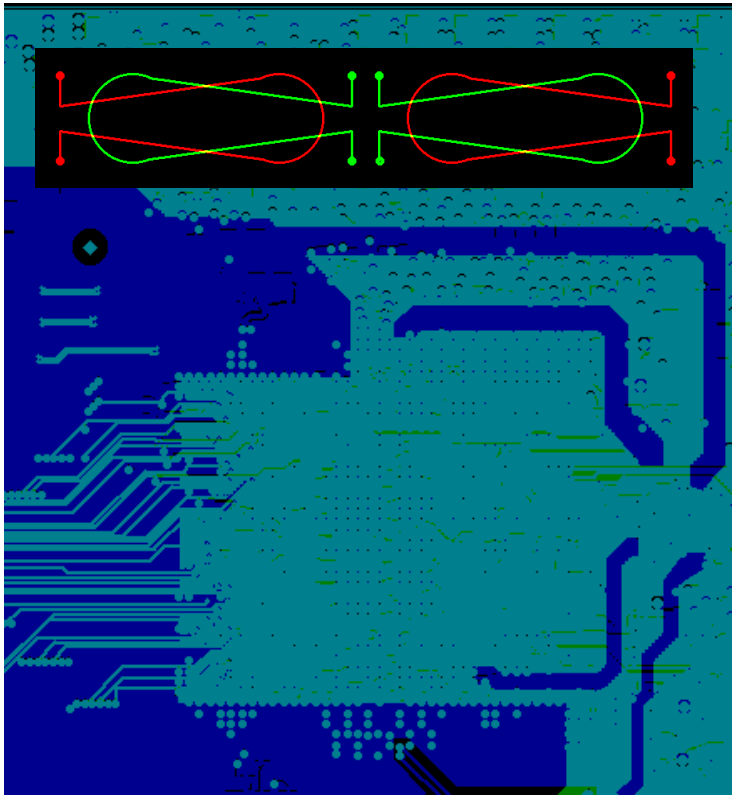


The embedded component. Size is 130 x 30mm

S A M P L E

RF Board with embedded component (Filter)



- 12 layer board, board size: 300 X 240mm

- The board is a high frequency RF board with an embedded component between layer 3 and 4. The side to side alignment between the 2 figures on layer 3 and 4 is critical. Alignment must be within +/-25um.

Due to a military confidential design, the illustrations shown here is not the original ones.

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1) Build Roger / FR4

				Layer
1	OL Cu 18 µm + plating Total 40-50um	Signal	50	1
	IL Core RO4350B 250 µm		250	
2	IL Cu 18 µm	Plane	17	2
	150 3x 106 FR4		150	
3	IL Cu 18 µm	Signal	0	3
	IL Core RO4350B 100 µm		100	
4	IL Cu 18 µm Cu	Signal	0	4
	150 3x 106 FR4		150	
5	IL Cu 18 µm	Plane	0	5
	IL Core RO4350B 250 µm		250	
6	IL Cu 18 µm	Plane	17	6
	100 2x 106 FR4		100	
7	IL Cu 18 µm	Plane	17	7
	IL Core RO4350B 250 µm		250	
8	IL Cu 18 µm	Plane	17	8
	150 3x 106 FR4		150	
9	IL Cu 18 µm	Signal	0	9
	IL Core RO4350B 100 µm		100	
10	IL Cu 18 µm	Signal	0	10
	150 3x 106 FR4		150	
11	IL Cu 18 µm	Plane	17	11
	IL Core RO4350B 250 µm		250	
12	OL Cu 18 µm + plating Total 40-50um	Signal	50	12
	Total Thickness		2085	

Blind Via L1-L2 -Size 0.25mm

Blind Via L1-L4, 8 holes, -Size on drill-bit 0.25mm

RO4350B: Dissipation fact. DF : 0.0037 / 10GHz.

FR4: Typical DF 0.017 / 1MHz

2) Build Roger / Roger

				Layer
1	OL Cu 18 µm + plating Total 40-50um	Signal	50	1
	IL Core RO4350B 250 µm		250	
2	IL Cu 18 µm	Plane	17	2
	200 µm RO4450F prepreg		200	
3	IL Cu 18 µm	Signal	0	3
	IL Core RO4350B 100 µm		100	
4	IL Cu 18 µm Cu	Signal	0	4
	200 µm RO4450F prepreg		200	
5	IL Cu 18 µm	Plane	0	5
	IL Core RO4350B 250 µm		250	
6	IL Cu 18 µm	Plane	17	6
	100 µm RO4450F prepreg		100	
7	IL Cu 18 µm	Plane	17	7
	IL Core RO4350B 250 µm		250	
8	IL Cu 18 µm	Plane	17	8
	200 µm RO4450F prepreg		200	
9	IL Cu 18 µm	Signal	0	9
	IL Core RO4350B 100 µm		100	
10	IL Cu 18 µm	Signal	0	10
	200 µm RO4450F prepreg		200	
11	IL Cu 18 µm	Plane	17	11
	IL Core RO4350B 250 µm		250	
12	OL Cu 18 µm + plating Total 40-50um	Signal	50	12
	Total Thickness		2285	

Blind Via L1-L2 -Size 0.25mm

Blind Via L1-L4, 8 holes, -Size on drill-bit 0.25mm

RO4350B:

Rogers use HP foil in the manufacture of their cores, has coarse dendrites (rough on the back) which can cause rough edges and over etching.

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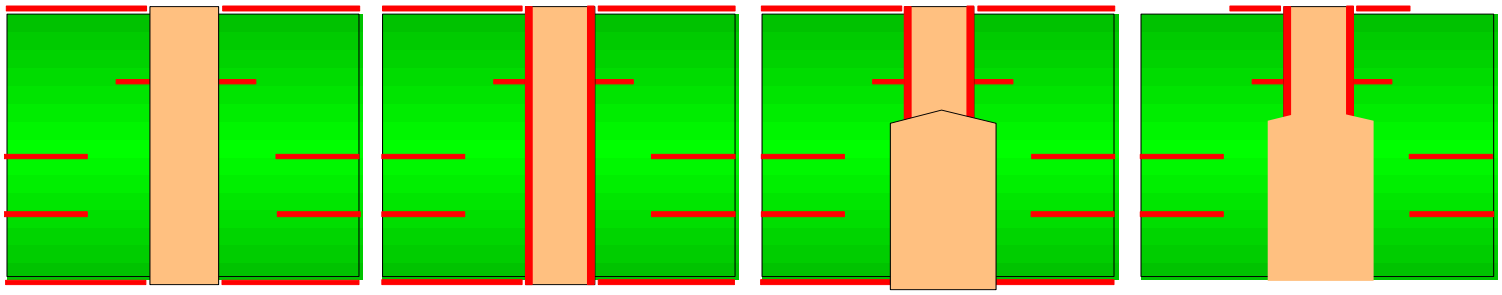
Backdrilling



Drilling

Electroless & PP

Back-drilling

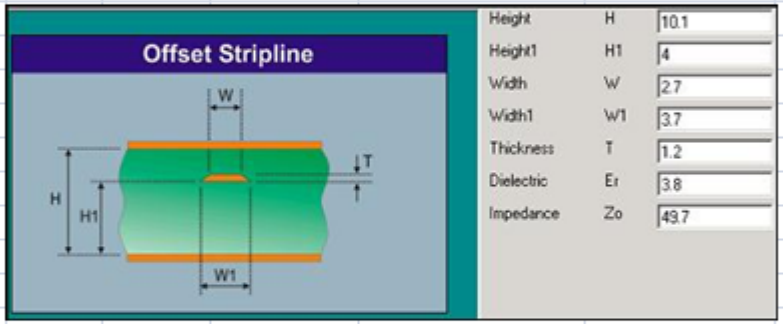
Finished Product

More S A M P L E s 1/2

Advanced Multilayer build

12 layer stack up for 64mil+/-10% board thickness			Thickness (mil)	Thickness (mm)
		Solder mask	1	0.025
L1		copper foil + plated	1.6	0.041
		Prepreg 1080x1	3.1	0.079
L2		copper foil 1.0 oz	1.2	0.030
		CORE	4	0.102
L3		copper foil 1.0 oz	1.2	0.030
		Prepreg 2116x1	4.9	0.124
L4		copper foil 1.0 oz	1.2	0.030
		CORE	4	0.102
L5		copper foil 1.0 oz	1.2	0.030
		Prepreg 1080x1	3	0.076
L6		copper foil 0.5 oz	0.6	0.015
	PTH 1-12	CORE	10	0.254
L7		copper foil 0.5 oz	0.6	0.015
		Prepreg 1080x1	3	0.076
L8		copper foil 1.0 oz	1.2	0.030
		CORE	4	0.102
L9		copper foil 1.0 oz	1.2	0.030
		Prepreg 2116x1	4.9	0.124
L10		copper foil 1.0 oz	1.2	0.030
		CORE	4	0.102
L11		copper foil 1.0 oz	1.2	0.030
		Prepreg 1080x1	3.1	0.079
L12		copper foil + plated	1.6	0.041
		Solder mask	1	0.025
		Total:	64	1.626

layer	Ref. layer	Type	Imped. control (+/- 10%)	Imped. Line width/ space (mil)
L4	L3/L5	Single	50ohm	3.7
L9	L8/L10	Single	50ohm	3.7
L1	L2	Diff	90ohm	4.9/8
L12	L11	Diff	90ohm	4.9/8
L1	L2	Diff	100ohm	4/10
L12	L11	Diff	100ohm	4/10



Material: TU-752
TG 180 ,
Dk: 4.3 / 1GHz __ Dk4.1 / 10GHz

Calculated with Dk 3.8

Notes: All dielectric layer thickness are estimated based on inner layer copper remain ratio 70%

All copper layers, 1.0oz (35um) Look at line width/space for 50 ohm ss

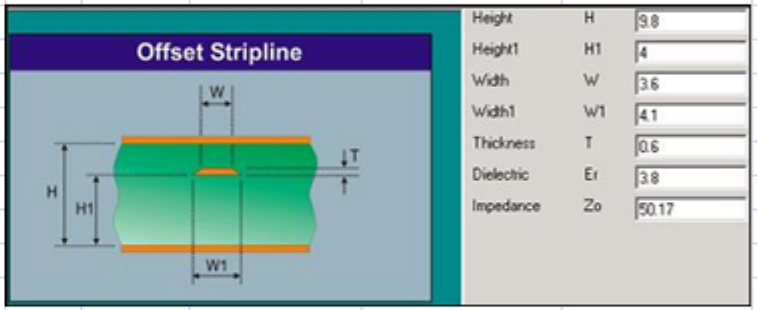
More S A M P L E s 2/2

Advanced Multilayer build

12 layer stack up for 64mil+/-10% board thickness		Thickness (mil)	Thickness (mm)
	Solder mask	1	0.025
L1	copper foil + plated	1.6	0.041
	Prepreg 1080x1	3	0.076
L2	copper foil 0.5 oz	0.6	0.015
	CORE	3	0.076
L3	copper foil 0.5 oz	0.6	0.015
	Prepreg 2116x1	5.2	0.132
L4	copper foil 0.5 oz	0.6	0.015
	CORE	4	0.102
L5	copper foil 0.5 oz	0.6	0.015
	Prepreg 1080x1	3.2	0.081
L6	copper foil 0.5 oz	0.6	0.015
	CORE	15	0.381
L7	copper foil 0.5 oz	0.6	0.015
	Prepreg 1080x1	3.2	0.081
L8	copper foil 0.5 oz	0.6	0.015
	CORE	4	0.102
L9	copper foil 0.5 oz	0.6	0.015
	Prepreg 2116x1	5.2	0.132
L10	copper foil 0.5 oz	0.6	0.015
	CORE	3	0.076
L11	copper foil 0.5 oz	0.6	0.015
	Prepreg 1080x1	3	0.076
L12	copper foil + plated	1.6	0.041
	Solder mask	1	0.025
	Total:	63	1.600

PTH 1-12

layer	Ref. layer	Type	Imped. control (+/- 10%)	Imped. Line width/ space (mil)
L4	L3/L5	Single	50ohm	4.1
L9	L8/L10	Single	50ohm	4.1
L1	L2	Diff	90ohm	4.7/8
L12	L11	Diff	90ohm	4.7/8
L1	L2	Diff	100ohm	4/10
L12	L11	Diff	100ohm	4/10



Material: TU-752
TG 180 ,
Dk: 4.3 / 1GHz __ Dk4.1 / 10GHz

Calculated with Dk 3.8

Notes: All dielectric layer thickness are estimated based on inner layer copper remain ratio 70%

All copper layers, 0.5oz (17um) Look at line width / space for 50 ohm ss

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Another S A M P L E 1/1

Advanced Multilayer build

16L layer stack up for 1.73mm+/- 10% board thickness		Thickness (mil)	Thickness (mm)
	Solder mask	1.0	0.025
L1	copper foil + plated	1.6	0.041
	Prepreg 1080x1	3.0	0.076
L2	copper foil 0.5 oz	0.6	0.015
	CORE 3 mil	3.0	0.076
L3	copper foil 0.5 oz	0.6	0.015
	Prepreg 2116x1	4.1	0.104
L4	copper foil 0.5 oz	0.6	0.015
	CORE 4 mil	4.0	0.102
L5	copper foil 0.5 oz	0.6	0.015
	Prepreg 2116x1	4.1	0.104
L6	copper foil 0.5 oz	0.6	0.015
	CORE 4 mil	4.0	0.102
L7	copper foil 0.5 oz	0.6	0.015
	Prepreg 2116x1	4.1	0.104
L8	copper foil 0.5 oz	0.6	0.015
	CORE 3 mil	3.0	0.076
L9	copper foil 0.5 oz	0.6	0.015
	Prepreg 2116x1	4.1	0.104
L10	copper foil 0.5 oz	0.6	0.015
	CORE 4 mil	4.0	0.102
L11	copper foil 0.5 oz	0.6	0.015
	Prepreg 2116x1	4.1	0.104
L12	copper foil 0.5 oz	0.6	0.015
	CORE 4 mil	4.0	0.102
L13	copper foil 0.5 oz	0.6	0.015
	Prepreg 2116x1	4.1	0.104
L14	copper foil 0.5 oz	0.6	0.015
	CORE 3 mil	3.0	0.076
L15	copper foil 0.5 oz	0.6	0.015
	Prepreg 1080x1	3.0	0.076
L16	copper foil + plated	1.6	0.041
	Solder mask	1.0	0.025
	Total:	69.2	1.758

PTH 1-16

layer	Ref. layer	Type	Imped. control (+/- 10%)	Imped. Linewidth/ space (mil)	Evaluated	
L1	L2	Single	50ohm	4.5	50.12	
L5	L4/L6	Single	50ohm	3.7	49.79	
L12	L11/L13	Single	50ohm	3.7	49.79	
L16	L15	Single	50ohm	4.5	50.12	
L1	L2	Single	75ohm	3	58.89	Can't meet 75ohm.
L1	L3	Single	75ohm	4.3	74.99	
L5	L4/L6	Single	75ohm	3	54.84	Can't meet 75ohm.
L5	L3/L7	Single	75ohm	3.2	75.04	
L12	L11/L13	Single	75ohm	3	54.84	Can't meet 75ohm.
L12	L10/L14	Single	75ohm	3.2	75.04	
L16	L15	Single	75ohm	3	58.89	Can't meet 75ohm.
L16	L14	Single	75ohm	4.3	74.99	
L1	L2	Diff	90ohm	4.7/8	90.13	
L5	L4/L6	Diff	90ohm	4.3/7	89.57	
L12	L11/L13	Diff	90ohm	4.3/7	89.57	
L16	L15	Diff	90ohm	4.7/8	90.13	
L1	L2	Diff	100ohm	3.7/8	99.38	
L5	L4/L6	Diff	100ohm	3.5/8	99.9	
L12	L11/L13	Diff	100ohm	3.5/8	99.9	
L16	L15	Diff	100ohm	3.7/8	99.38	

To be creative:

Alternative ref. layer has been suggested for the 75ohm single impedance lines on layer 1 , 5 , 12 and 16.

Notes:
All dielectric layer thickness are estimated based on inner layer copper remain ratio 70%

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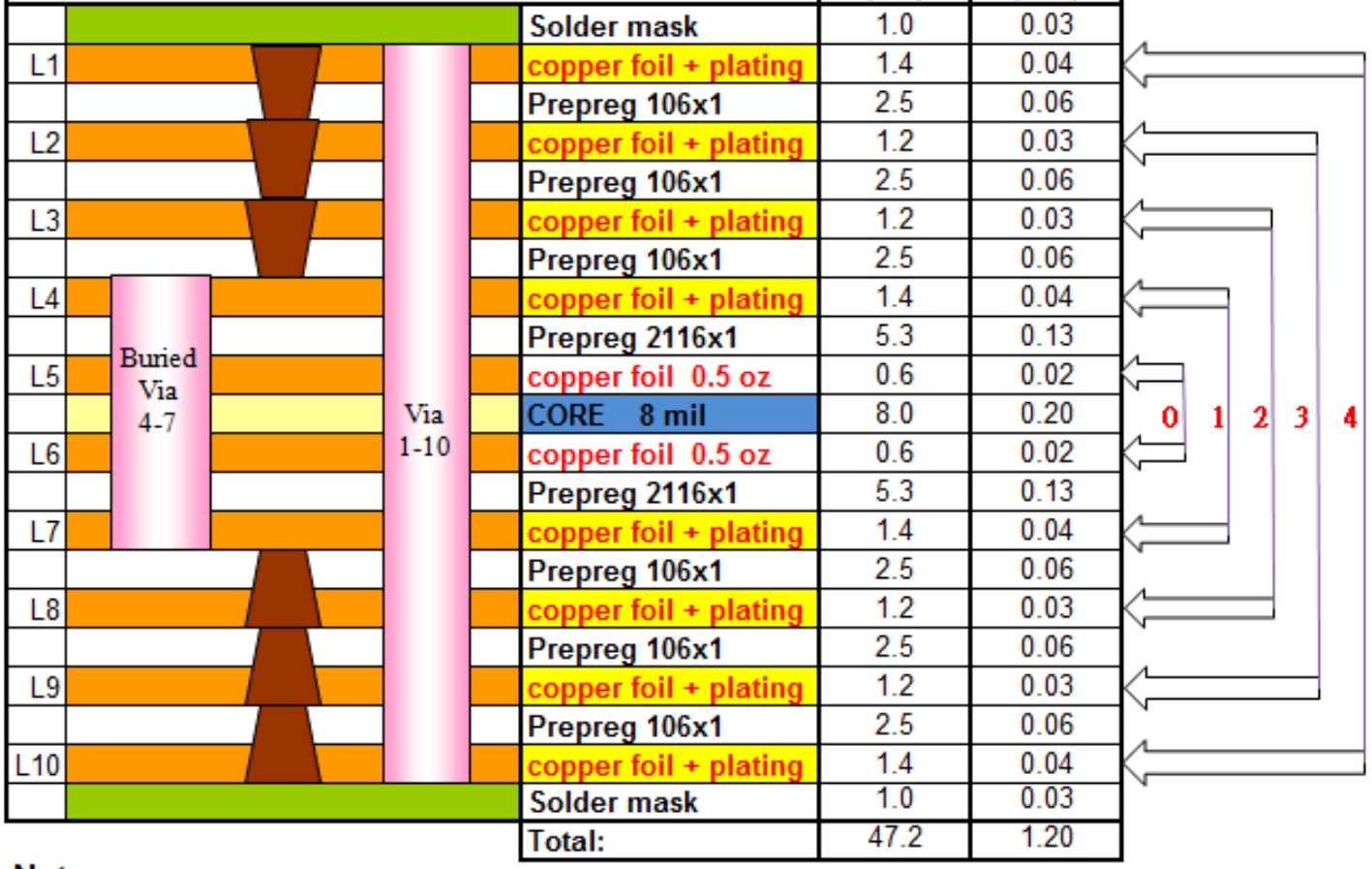
Crasy ? ..not any longer

3-4-3 layer stack up for 1.2mm+/-10% board thickness		Thickness (mil)	Thickness (mm)
	Solder mask	1.0	0.03
L1	copper foil + plating	1.4	0.04
	Prepreg 106x1	2.5	0.06
L2	copper foil + plating	1.2	0.03
	Prepreg 106x1	2.5	0.06
L3	copper foil + plating	1.2	0.03
	Prepreg 106x1	2.5	0.06
L4	copper foil + plating	1.4	0.04
	Prepreg 2116x1	5.3	0.13
L5	copper foil 0.5 oz	0.6	0.02
	CORE 8 mil	8.0	0.20
L6	copper foil 0.5 oz	0.6	0.02
	Prepreg 2116x1	5.3	0.13
L7	copper foil + plating	1.4	0.04
	Prepreg 106x1	2.5	0.06
L8	copper foil + plating	1.2	0.03
	Prepreg 106x1	2.5	0.06
L9	copper foil + plating	1.2	0.03
	Prepreg 106x1	2.5	0.06
L10	copper foil + plating	1.4	0.04
	Solder mask	1.0	0.03
	Total:	47.2	1.20



Notes:

All dielectric layer thickness are estimated based on inner layer copper remain ratio 60%

No of bonding operations = 4. 8 out of 10 layers are plated

Cu balancing on plated layers - minimum prepregs - critical for impedance result,

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Sample on how an error can occore

EVEN if a netlist is attached with original data,

or netlist is generated from the PCB

Manufacturers CAM system.

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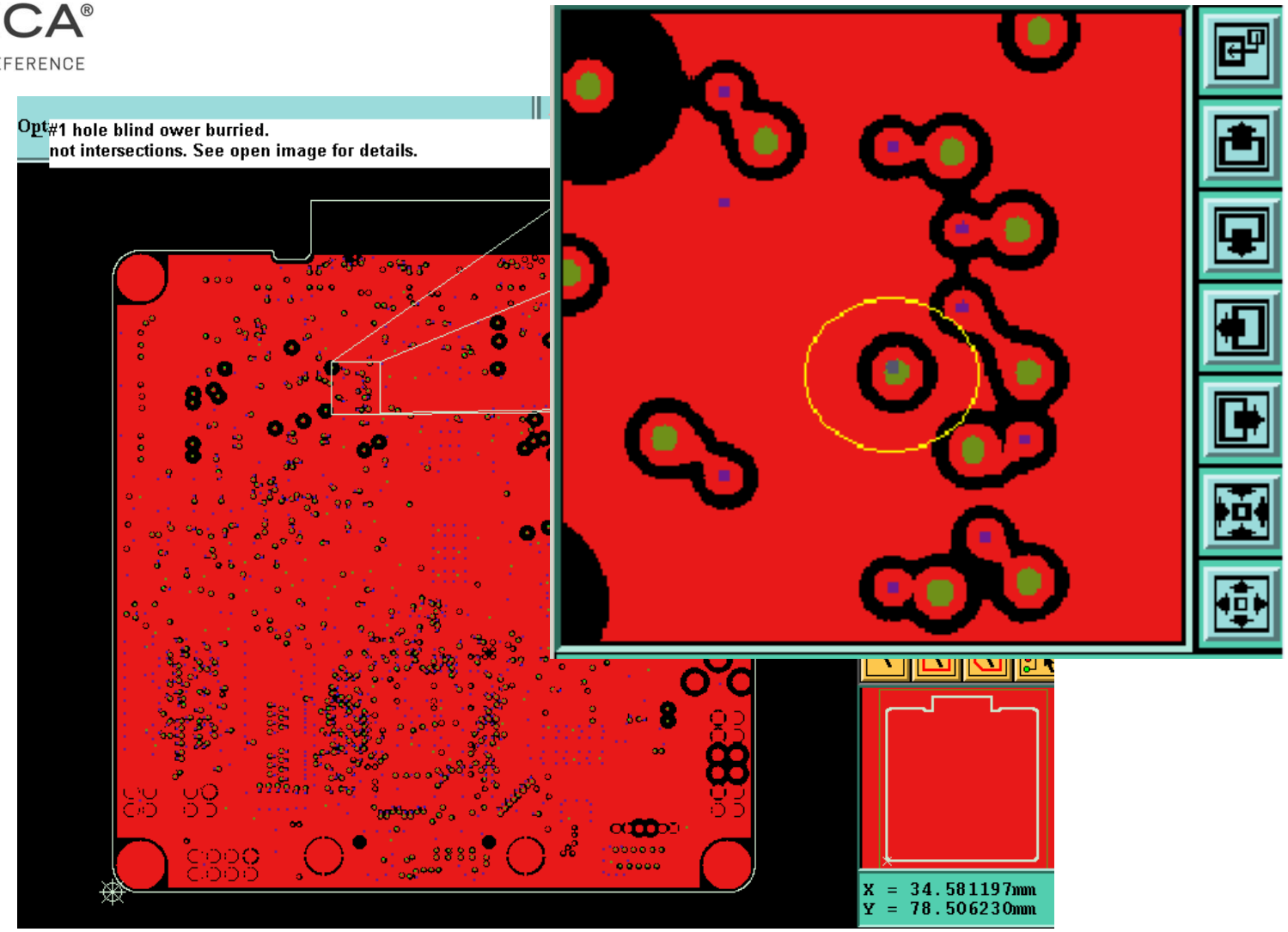

All mvia connections are of ”dog-bone type”, except one

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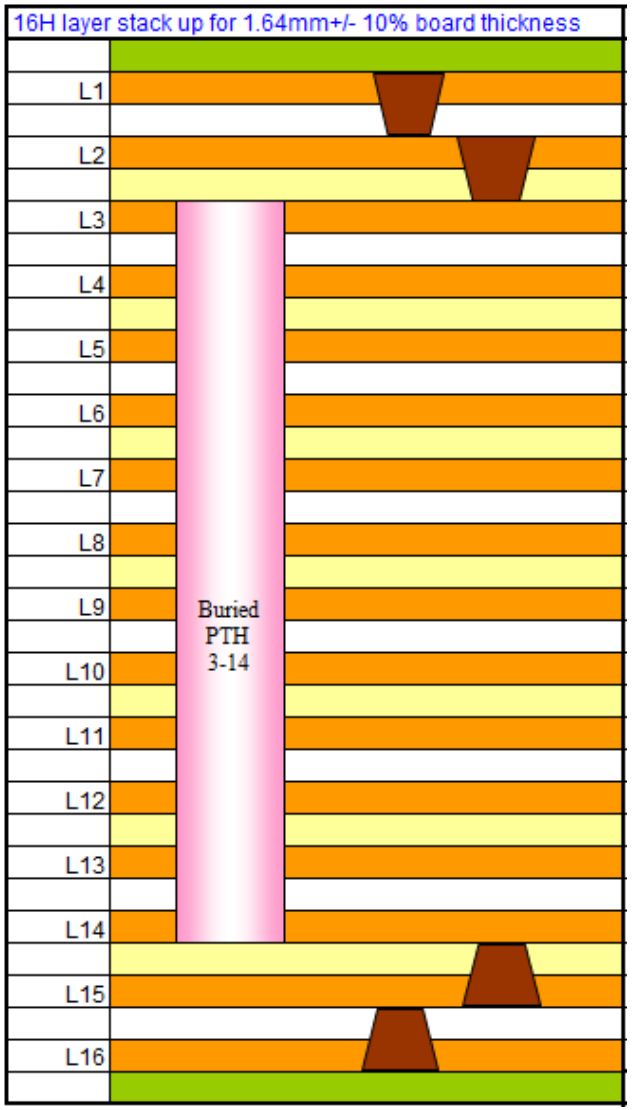
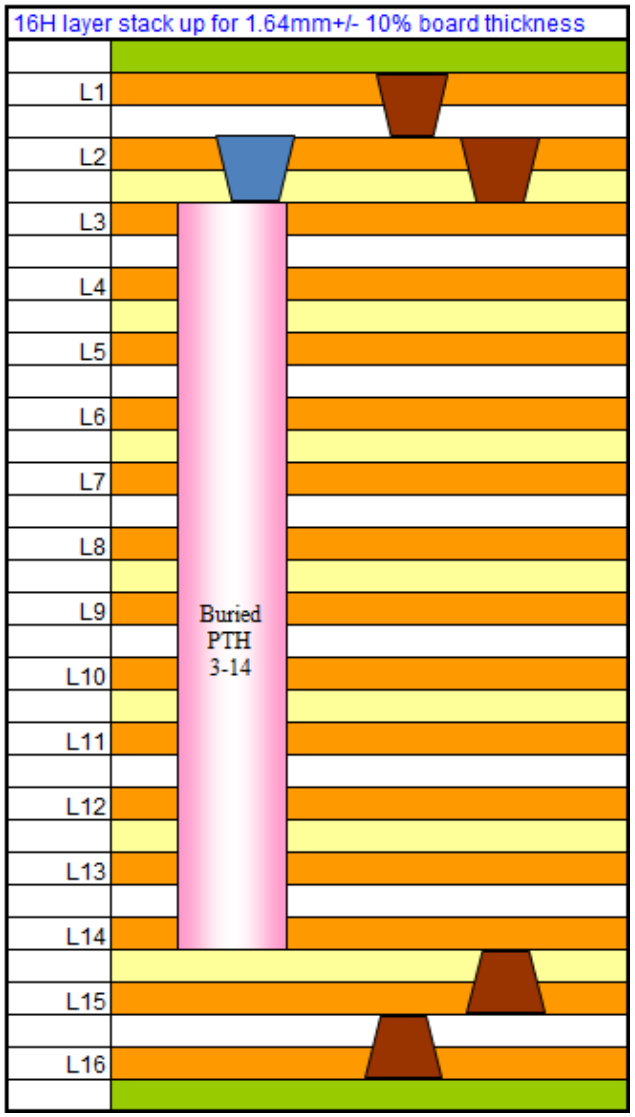
Supplied build - Actual build





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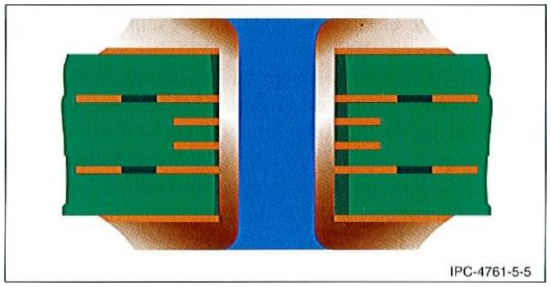
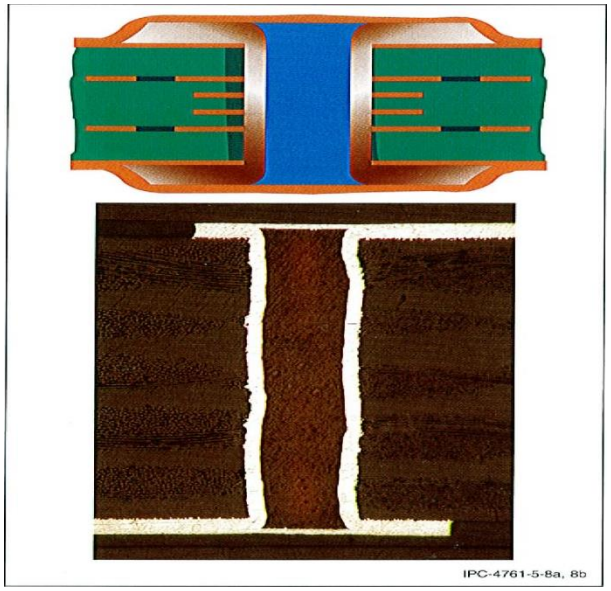
IPC 4761 Type V: Filled via

Specification	A via with material applied into the via targeting a full penetration and encapsulation of the hole.
Requirements	All holes shall be blocked and hole wall shall be 100% covered with solder mask Dents are acceptable as long as the hole-wall is covered with solder mask or plugging ink Boards with exposed copper or surface finish inside via holes could be rejected. To secure 100 % covering of hole-wall the filling level should be minimum 70%
Illustration	**Via hole as a function of the specified stack up**



IPC 4761 Type VII: Filled and capped via

Specification	A Type V via with a metalized coating applied over the via (illustration). The metalized capping shall be applied from both sides.
Requirements	Thickness of copper plating inside via shall meet the requirement for normal through via according to IPC class 2 unless a stricter requirement is specified in the procurement documentation.Cap plating shall be in accordance to IPC 6012C - 3.6.2.11.2 Fig 3.16 and table 3-10 class 3: Copper thickness: Minimum 12 um -Dimples over resin filling maxium 76um -Bumps/protrusion over resin filling maximum 50 um
Illustration	**Via hole as it should have been specified in the stack up**



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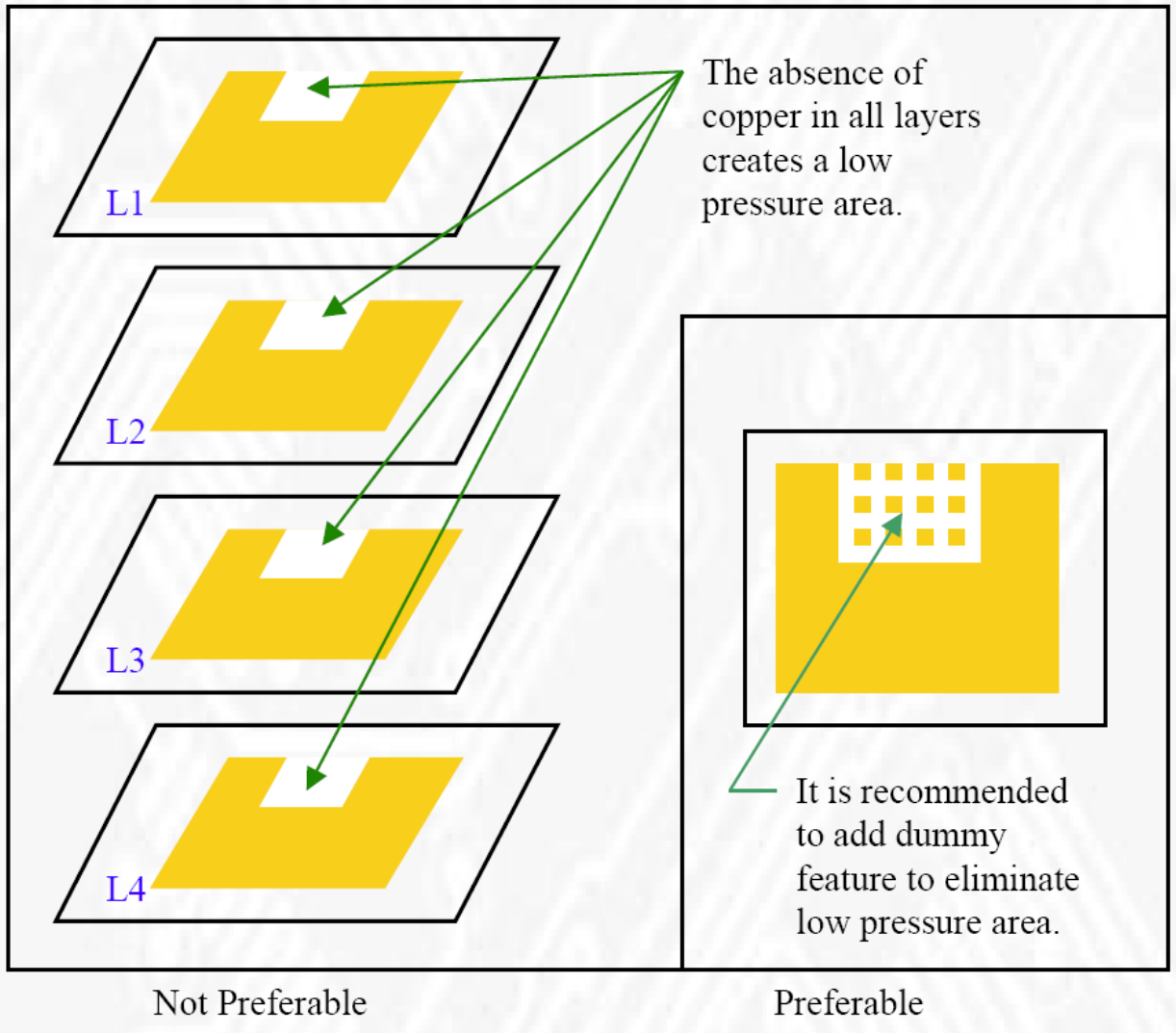
Copper Balancing (Eliminating Low Pressure Area)

Avoid having unbalanced pattern on inner layer. Otherwise, there is a risk of creating a low pressure area during lamination. It is recommended to add dummy copper feature to facilitate lamination.



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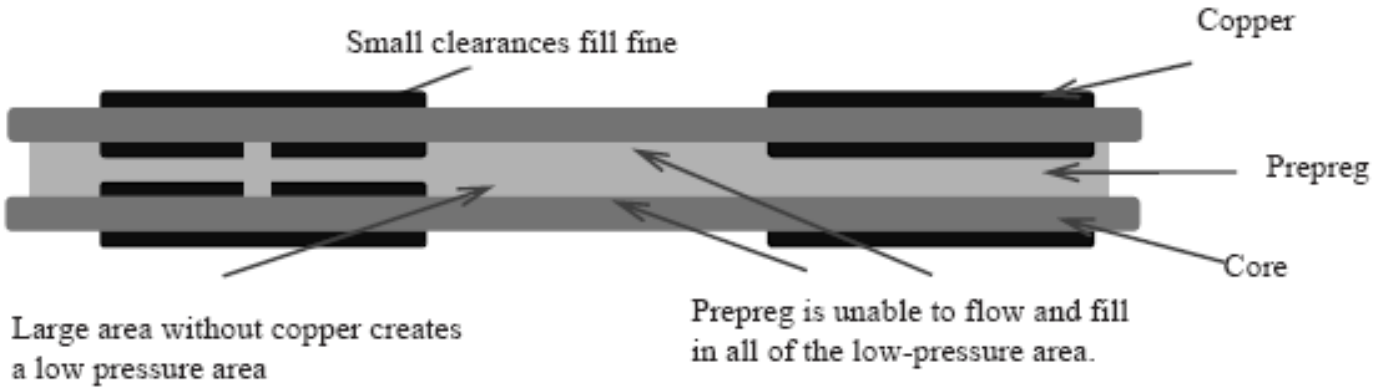
Copper Balancing (Eliminating Low Pressure Area)



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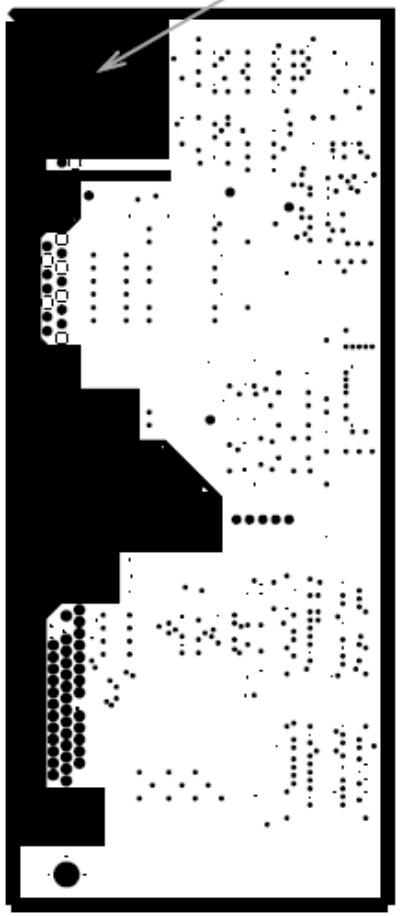
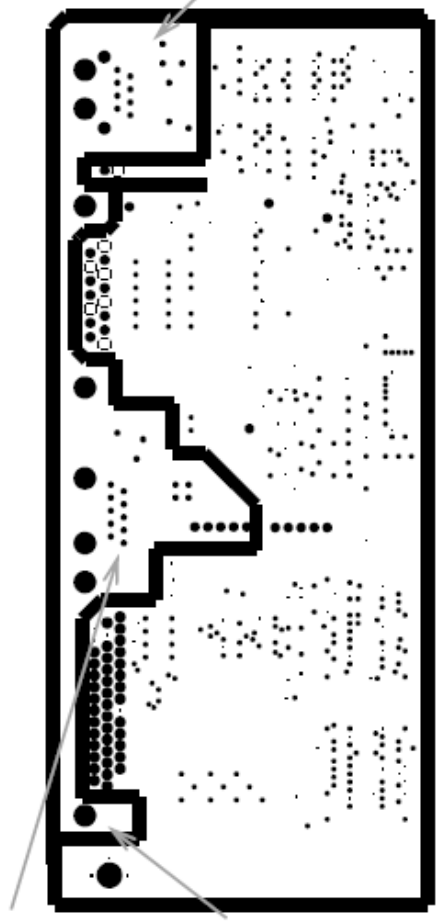
Copper Balancing (Eliminating Low Pressure Area)

Large area void of copper creates a low-pressure area during lamination



Avoid

Non-functional copper added to fill low-pressure area



Clearance antipads keep holes from touching unused copper

Preferred

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Non-Functional Pad Removal

A pad is considered as non-functional if its removal will not change electrical connectivity. Example of non-functional pads include:

- Pad not connected to any circuit
- Pad repeats in the same position
- Pad entirely removed by drill
- Pad covered by outer features

The removal of the non-functional pads (from inner layers) has the following advantages:

- Reduce the chances of short-circuit
  This is particularly for non-functional pads that are close to adjacent features.
- Increase drill accuracy
  This is because amount of copper being drilled is minimized
- Reduce wear of drill bit
  This is because amount of copper being drilled is minimized.

However, for thicker panels sometimes it is good to have non-function pads on some layers.

- 60~125mil thick : 2 NF pad layers
- 125~250 mil thick : 4 NF pad layers

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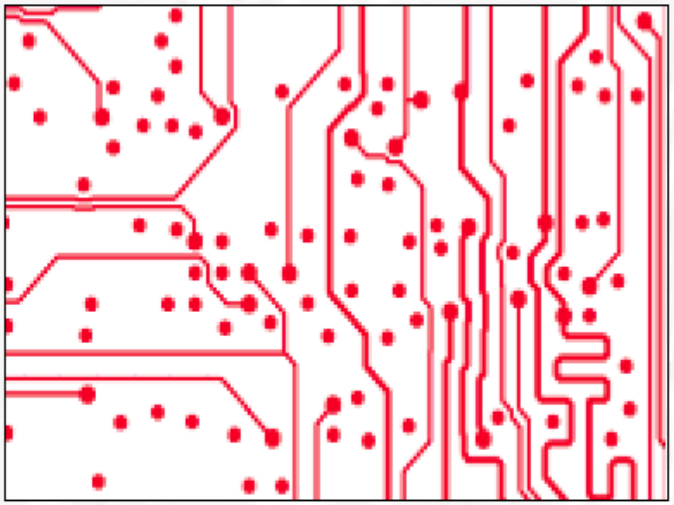
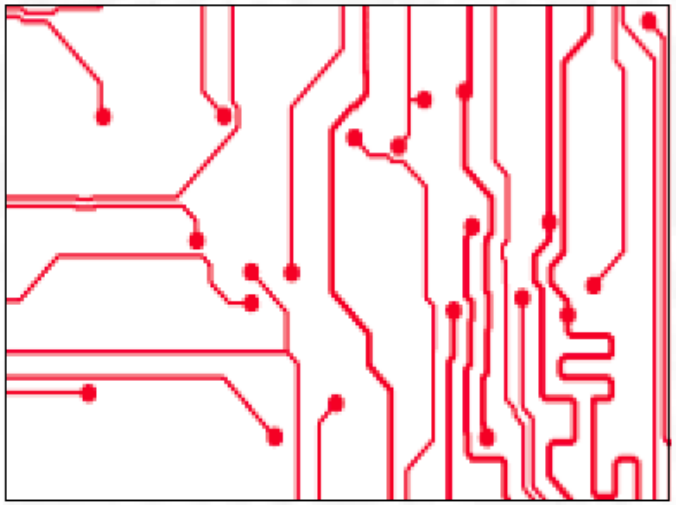


Not Preferable



Preferable

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Some “errors” seen

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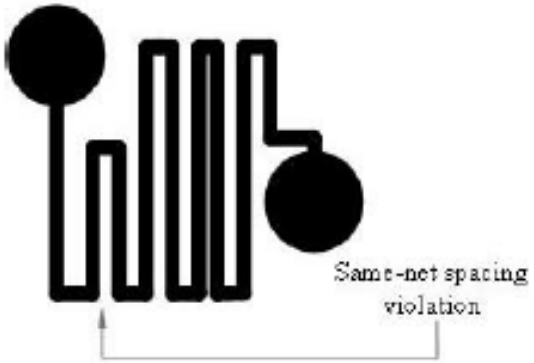
Same net spacing

Space between circuit and pad edge is > 0.005"
Avoid Preferred

Space between pad and the circuit is less than 0.005" mils

Photo resist has broken loose during processing and is re-deposited on the surface mount pad.



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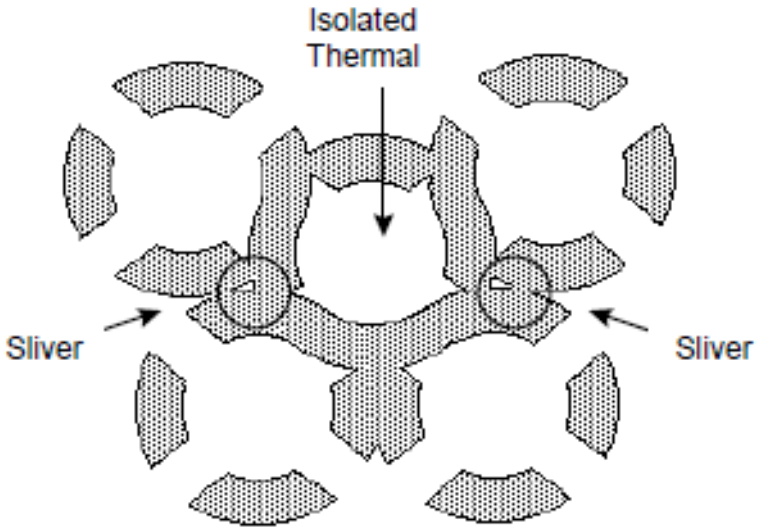
Power/Ground Plane Clearance and Thermal Pads



Avoid thermal isolation & slivers of copper

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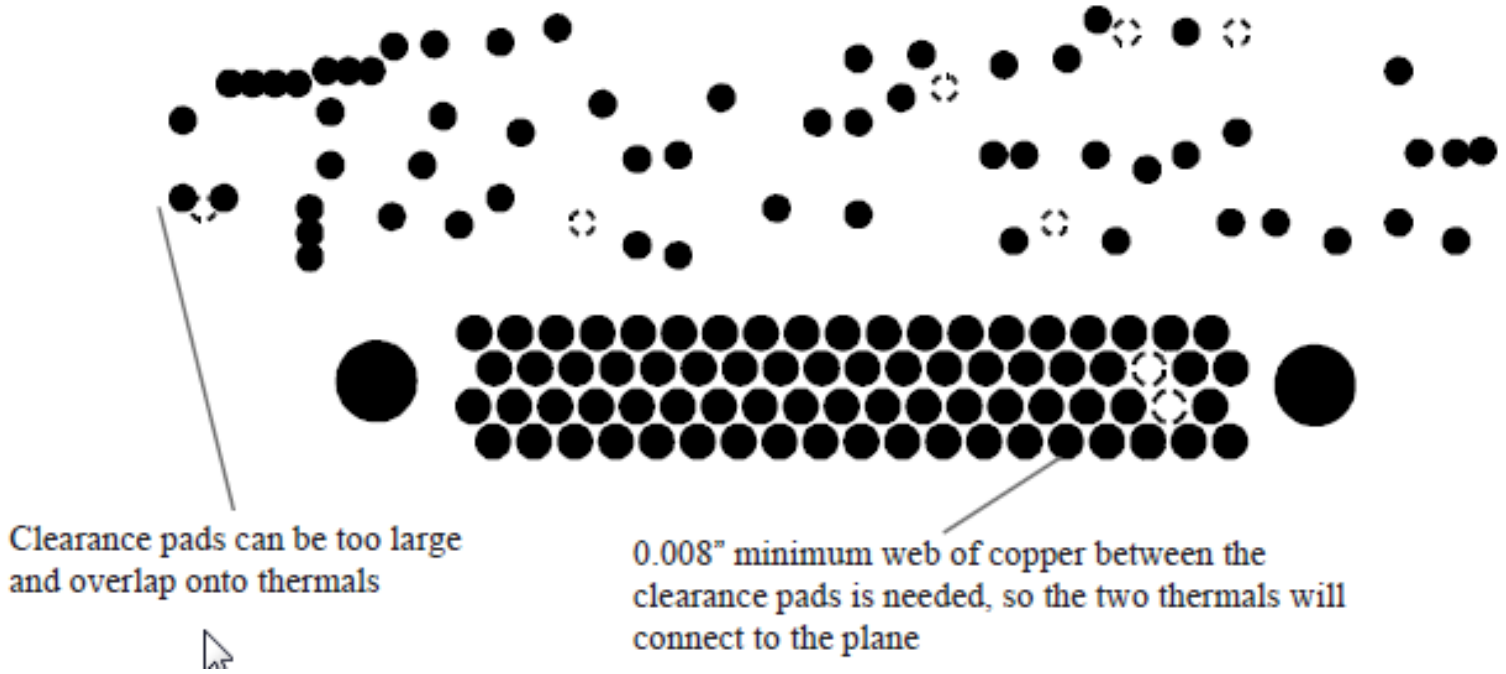
Clearance Pads



Avoid thermal isolation & slivers of copper

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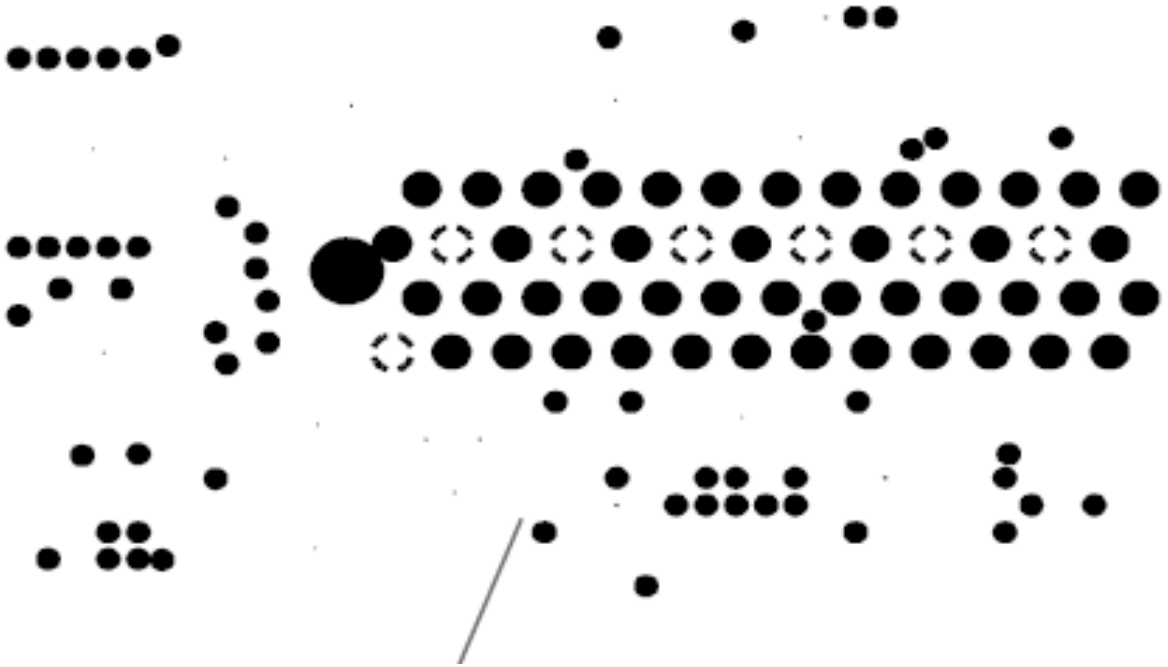
Direct Connect Vias (No Thermal Pad)



Direct connection of holes to a plane should include a clearance anti-pad half of the diameter of the hole placed at these locations.
This will reduce the amount of copper that needs to be drilled, and will result in less drill breakage of smaller drills.

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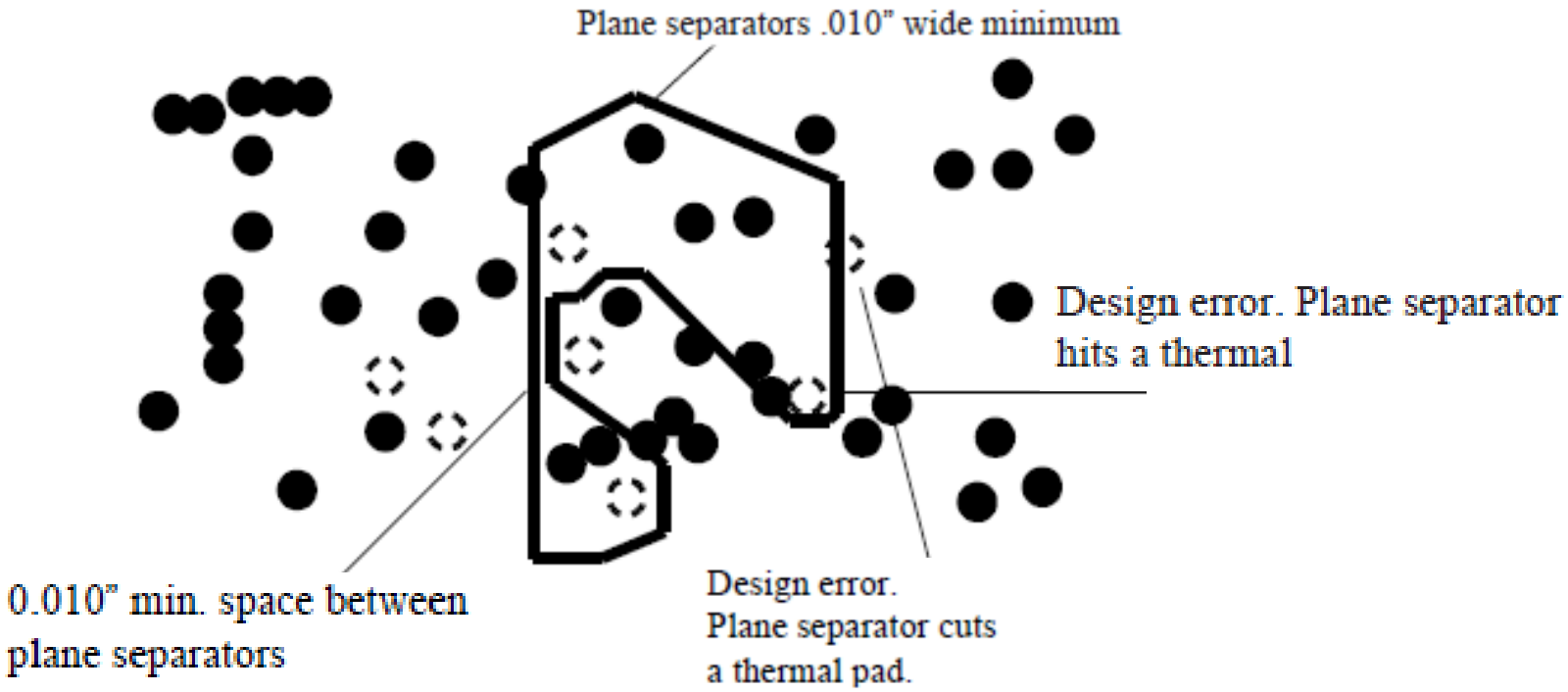
Voltage Plane Separation



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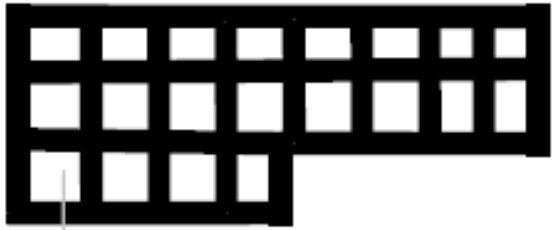
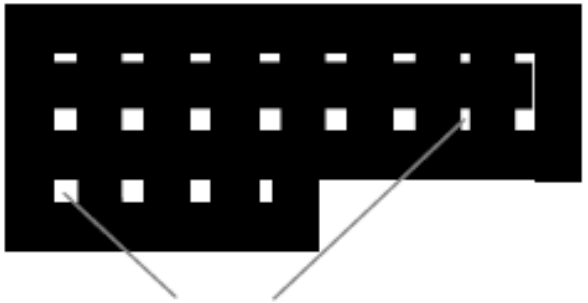
Crosshatch



Preferred minimum 0.025" squares

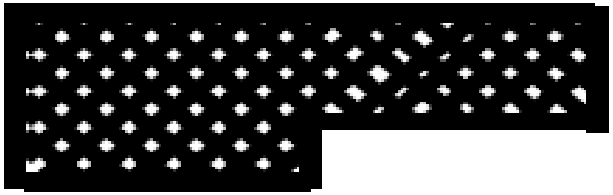
Preferred



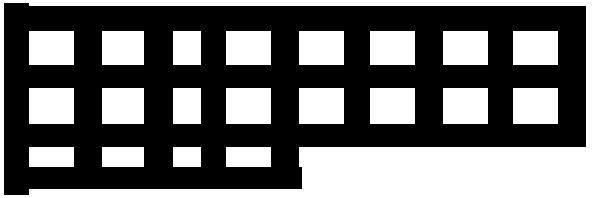
Avoid squares less then 0.008"

Avoid

Keep crosshatched drawn areas as vertical and horizontal lines. Do not run them at 45 degrees. These may flake off during processing, and may cause scrap, rework, and false design rule violations in CAM. All over preferred – keep the planes solid!



Avoid



Preferred

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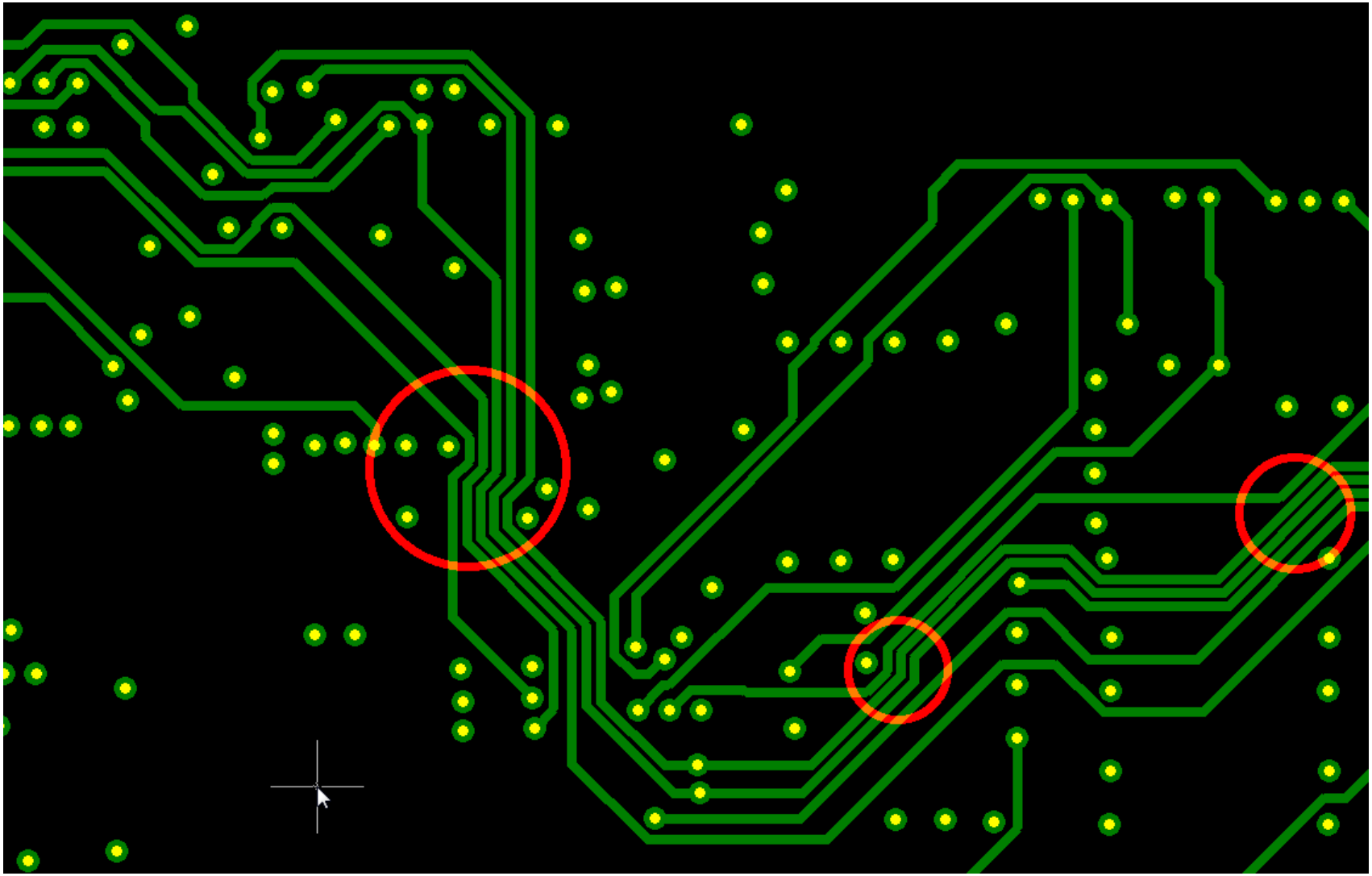
Layer 2 Unessesary dence packing of tracks …unbalanced



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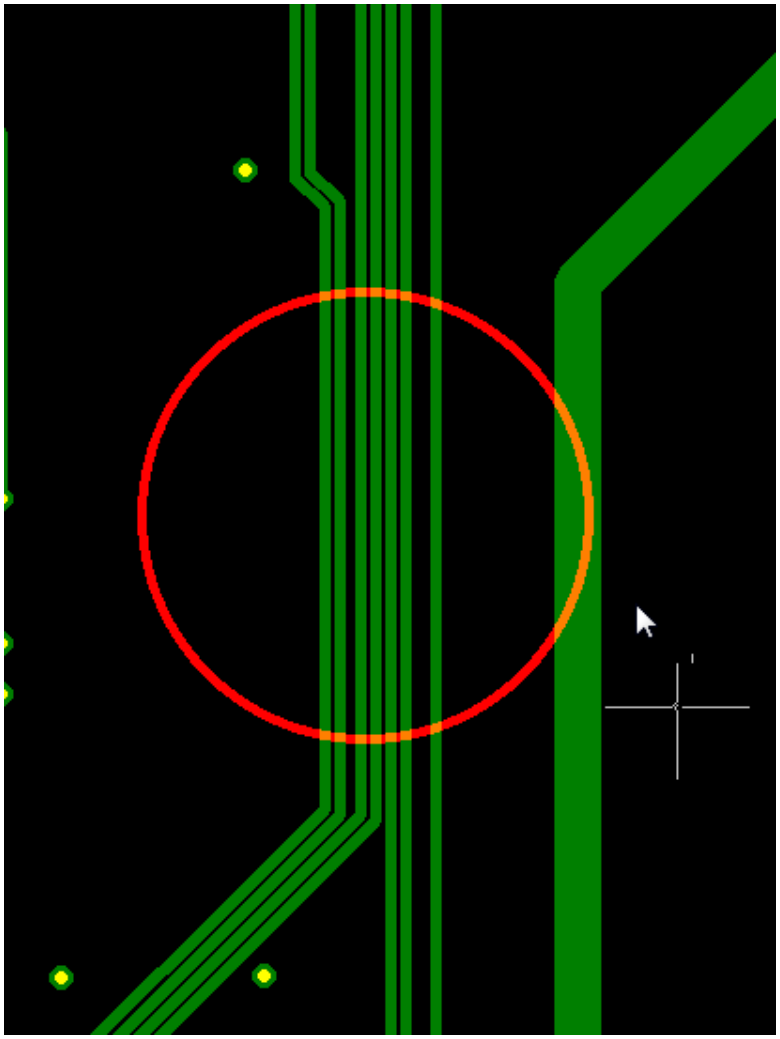

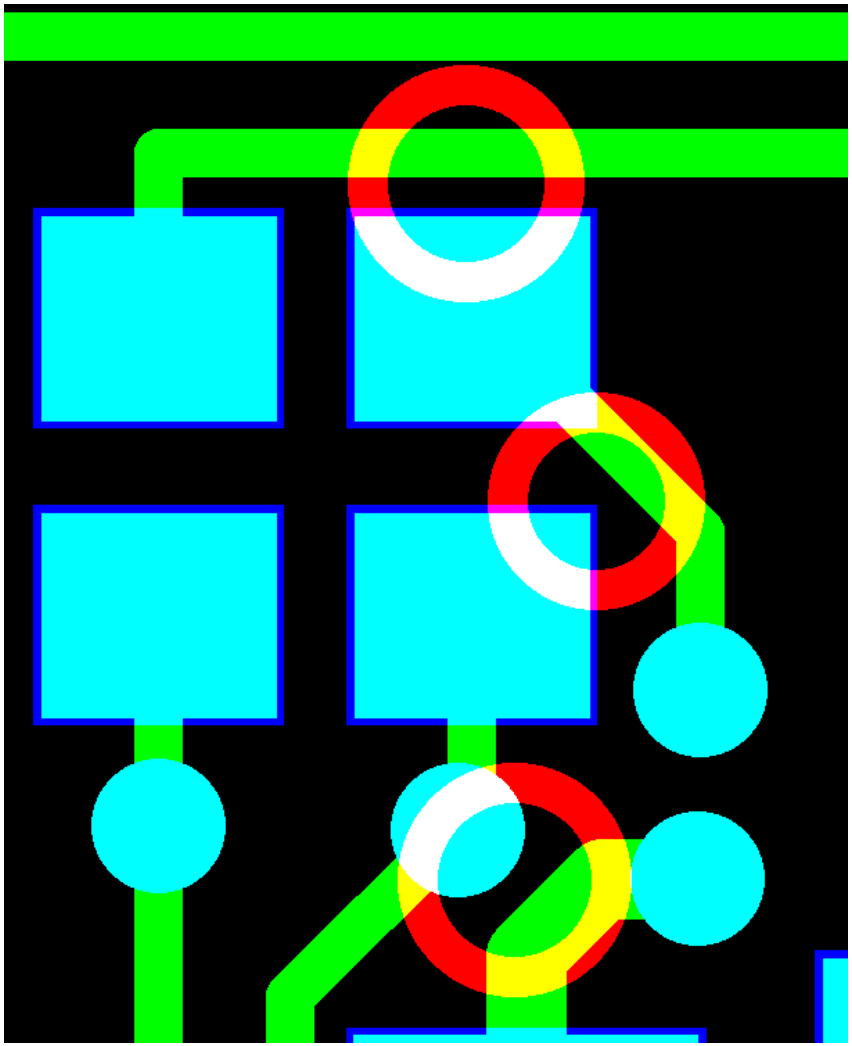

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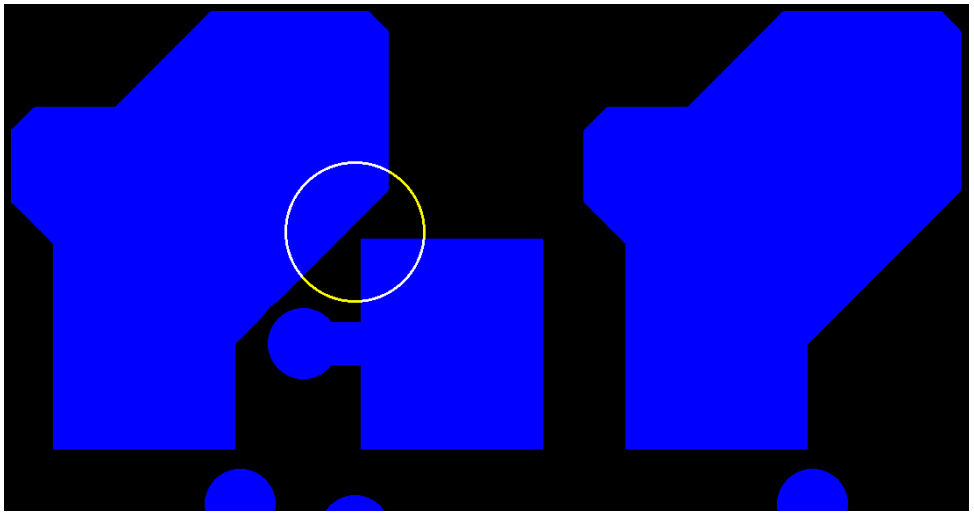
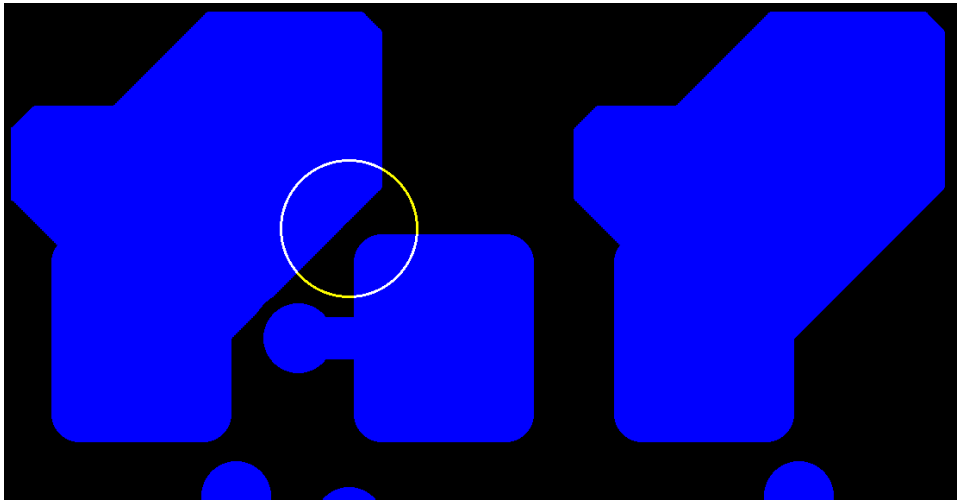
--before



Rounded corners on Sqare & rectangulare SMD Pads ?

Why not?

--after



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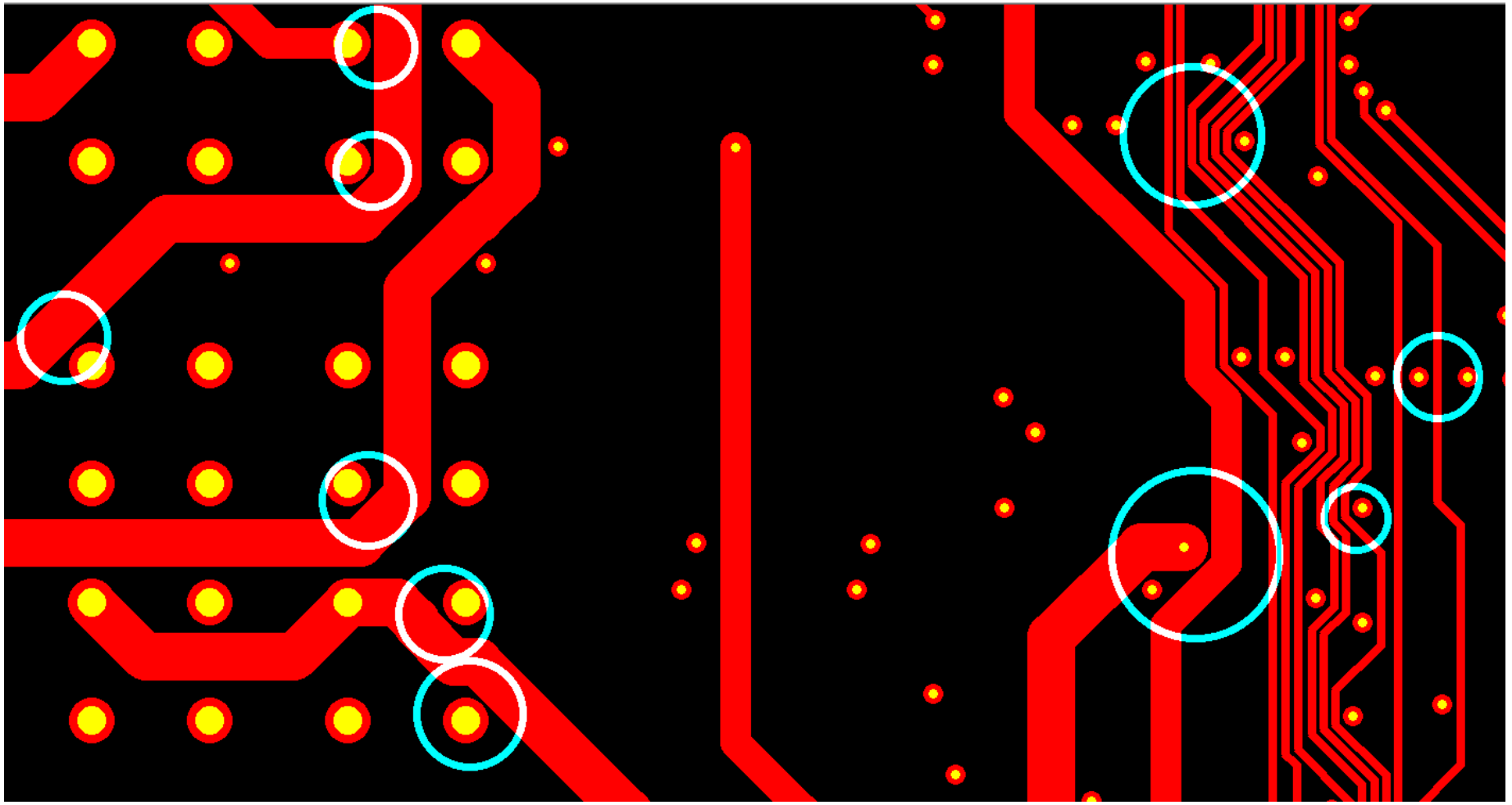
Layer 5 …unbalanced



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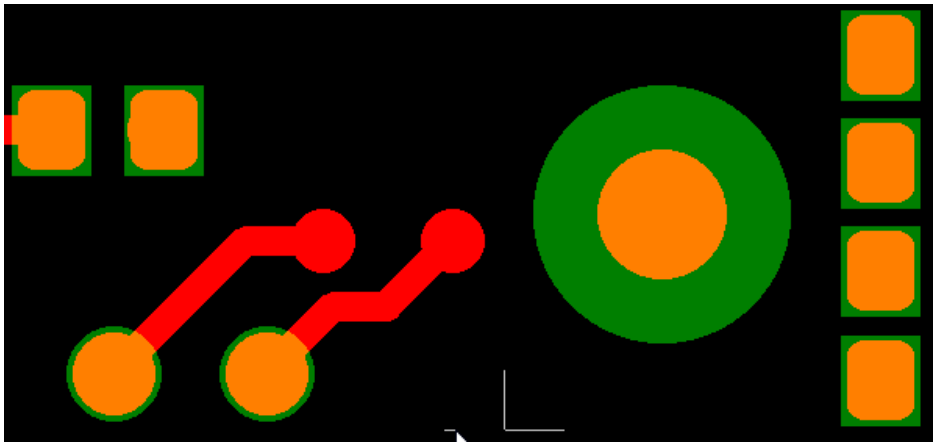
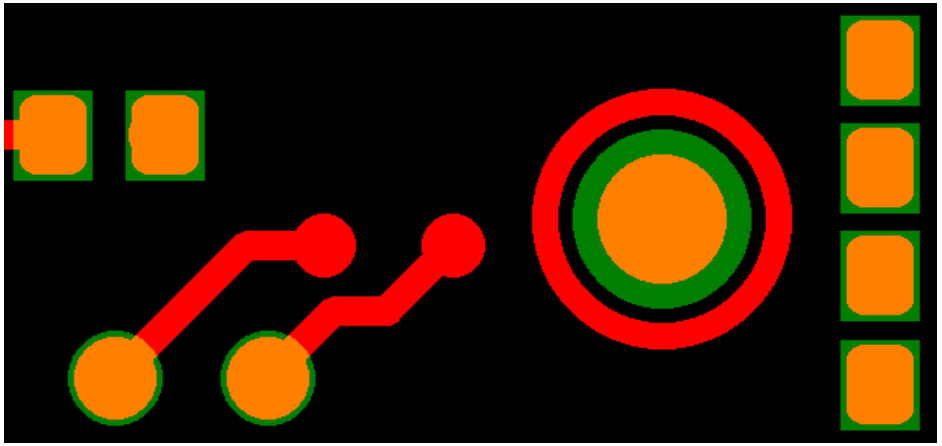
before



By adding a ring around the fiducials, you will both tell it is a fiducial and also secure the shape of it.

after



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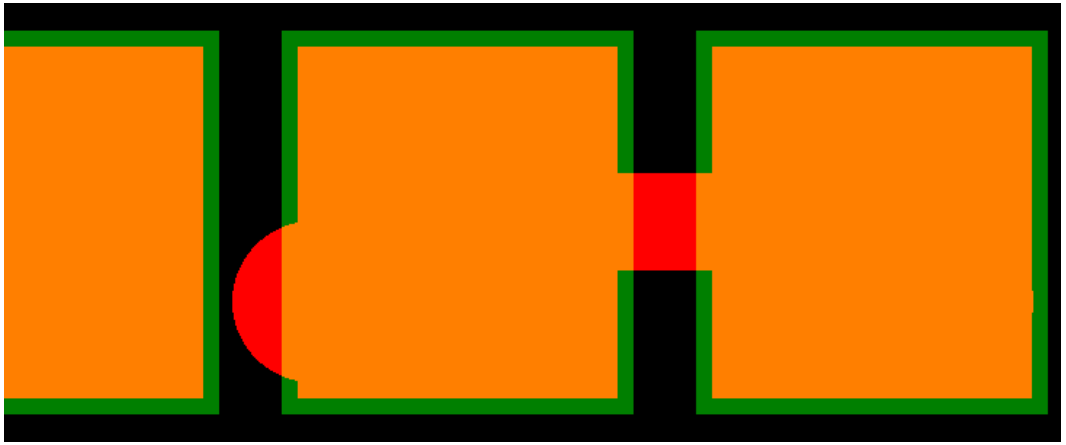
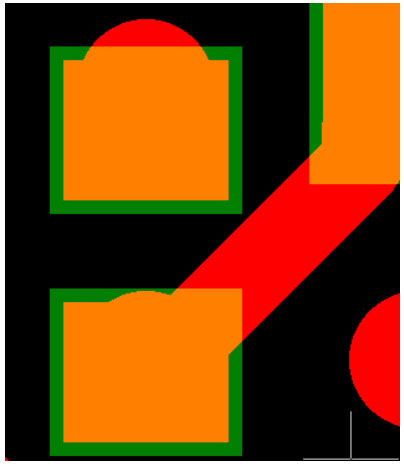
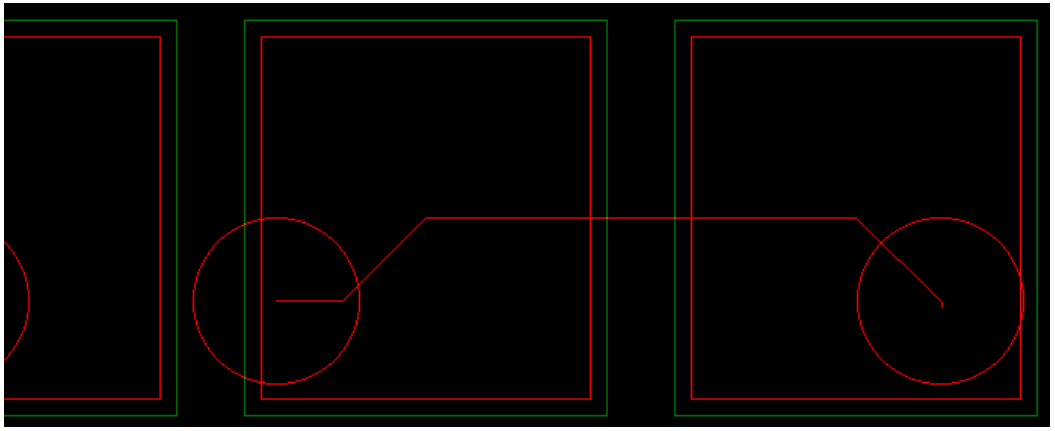
There will always be room for cleaning up….

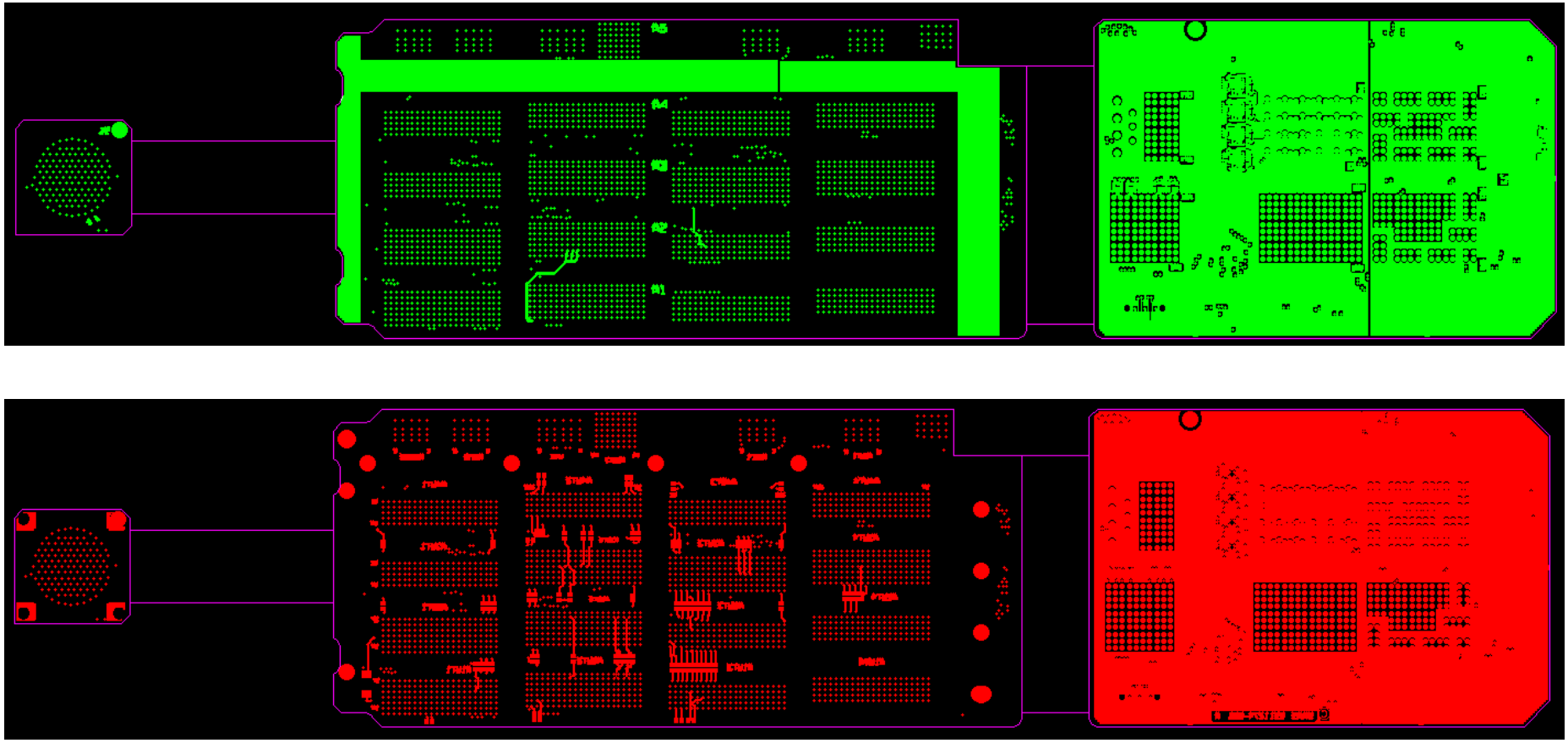






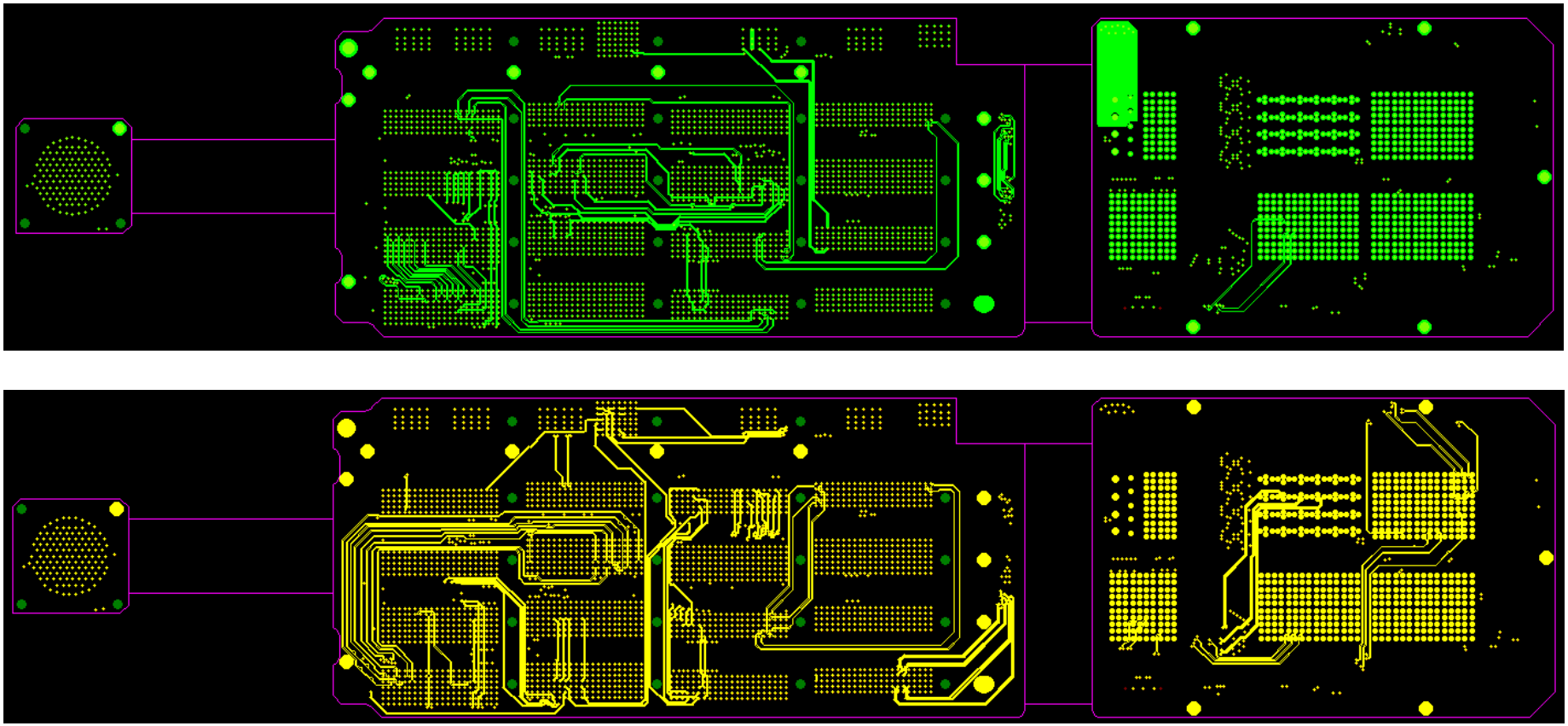
The following is showing some DFM on a 18 layer Flex Rigid PCB

Cu balance layer 01 & 18



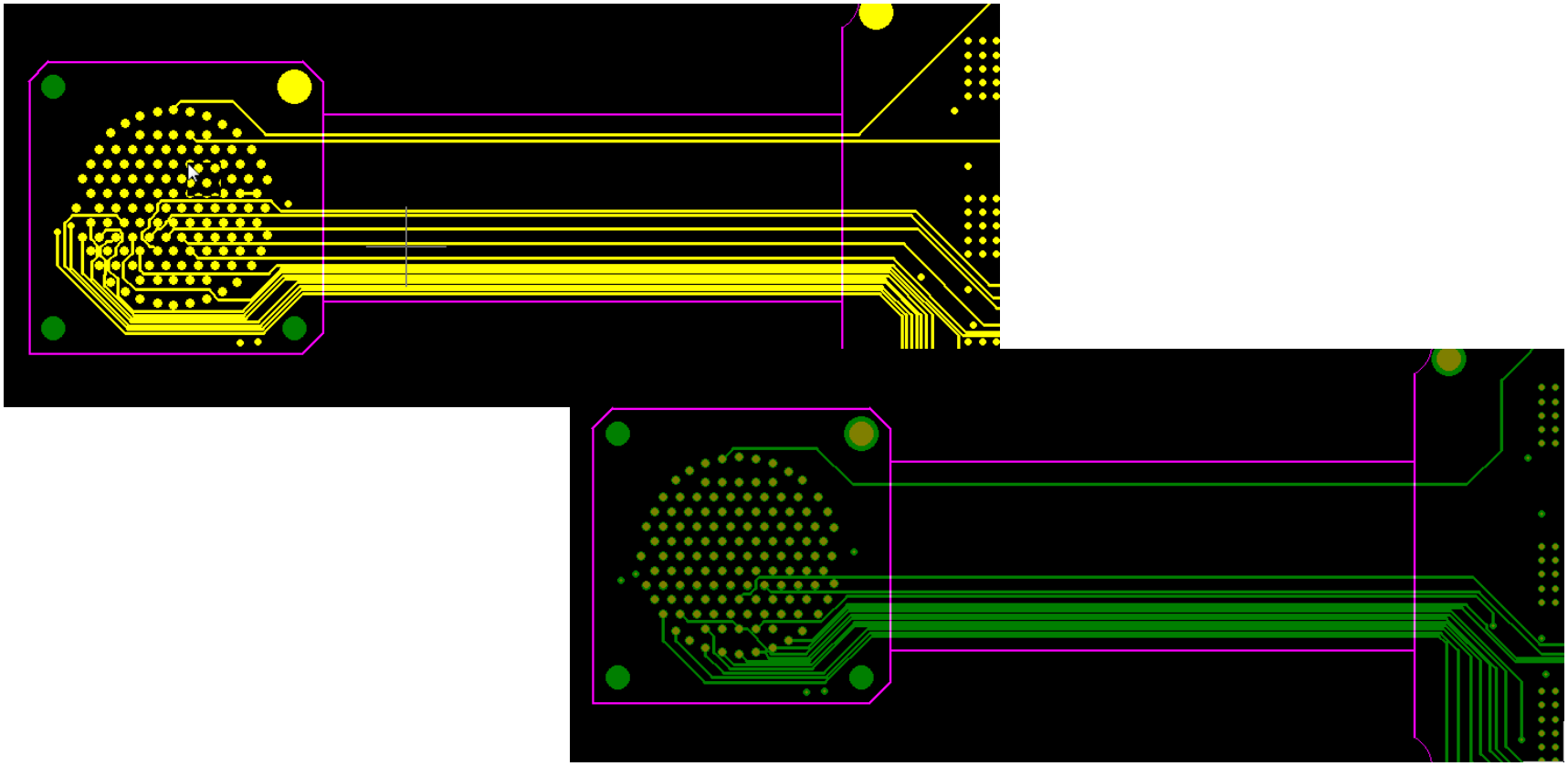
Cu balance layer 14 & 16

More copper can be added on innerlayers to improve balancing.
Better stability ref. bow & twist, - less risk delamination due to low preassure areas.



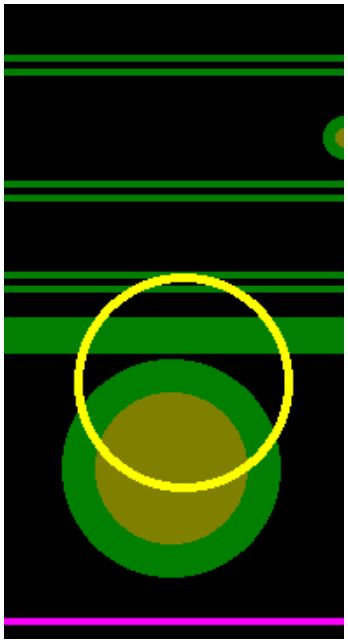
Layer 06 & 08

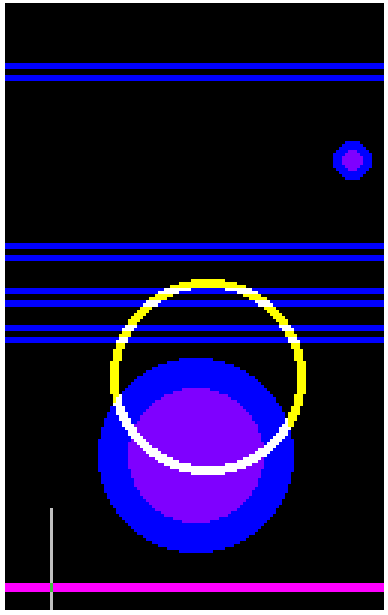
Signals can be more evenly spread over the flex

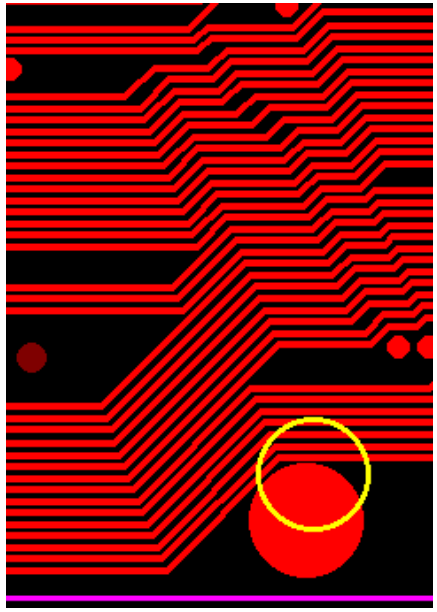


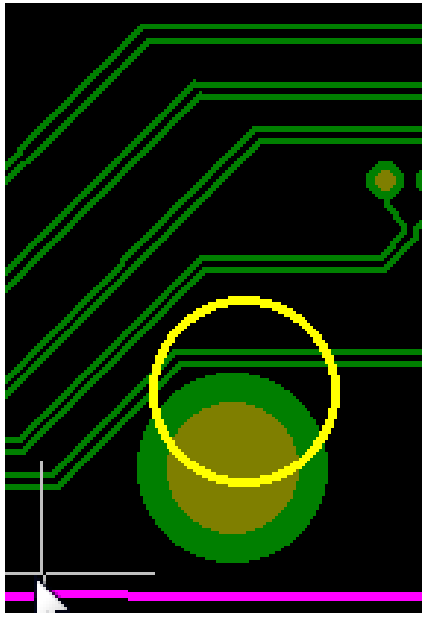
Same pos. shown on 4 innerlayers

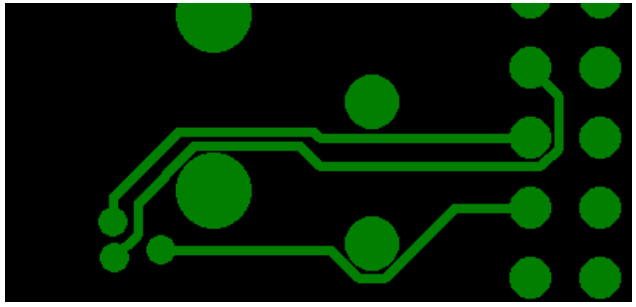
Lay 06 Lay 08 Lay 10 Lay 12



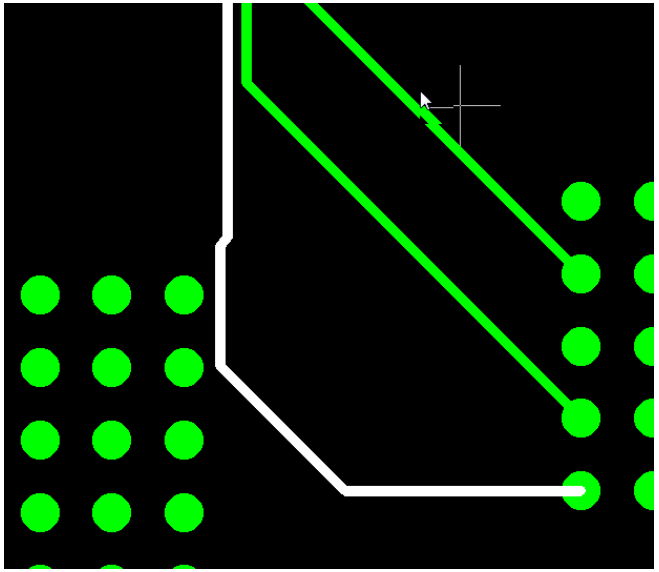






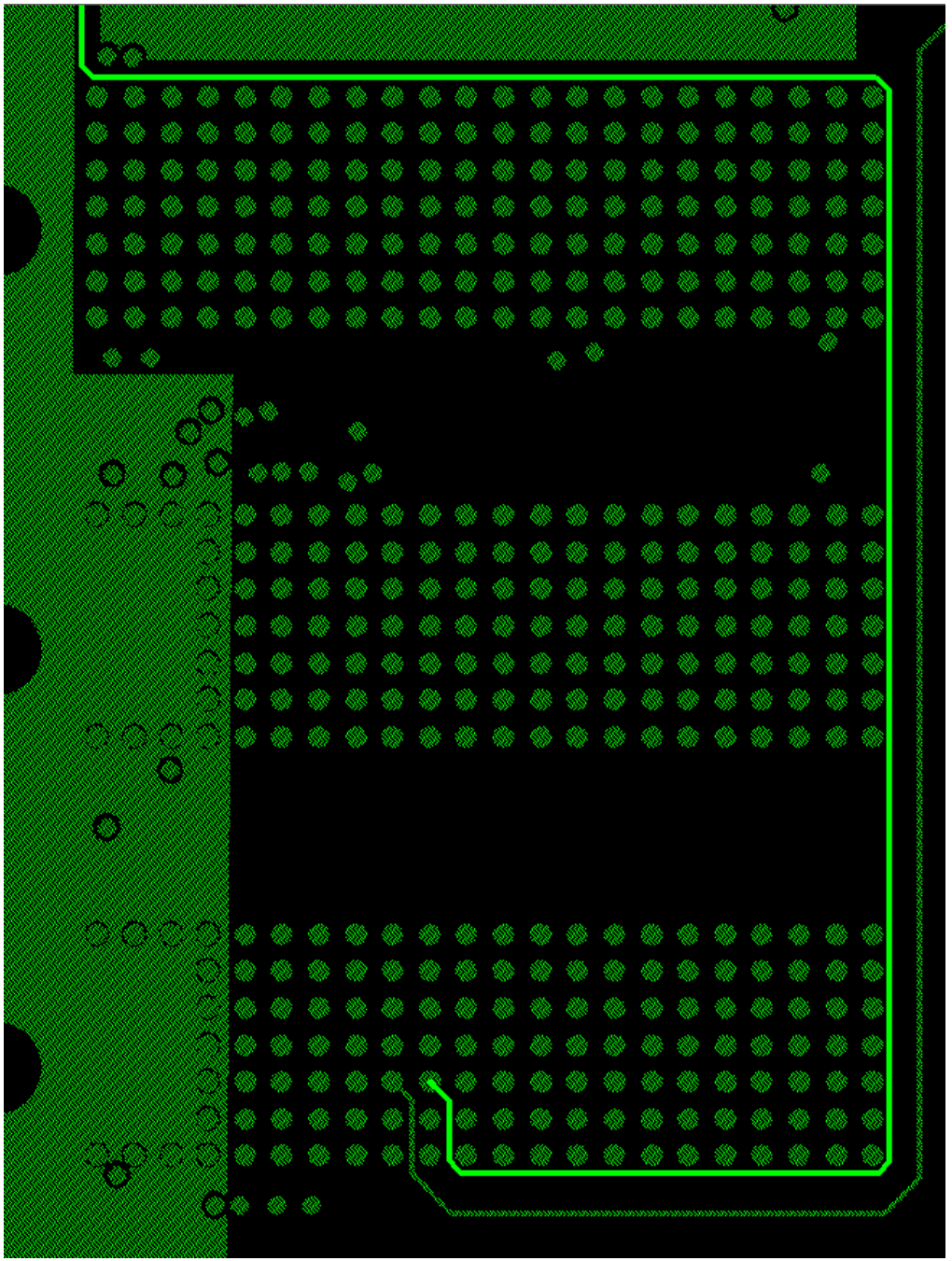


<- Layer 06. It is all about cleanup..



Both are from Lay 17:

Just to make sure that
I keep the distance
to a absolute minimum.

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Advanced HDI PCBs,

- microvia holes,
- stacked and staggered,
- buried vias and buried holes.

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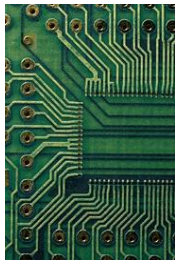
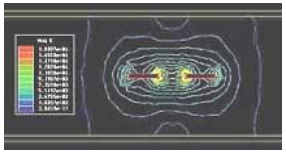
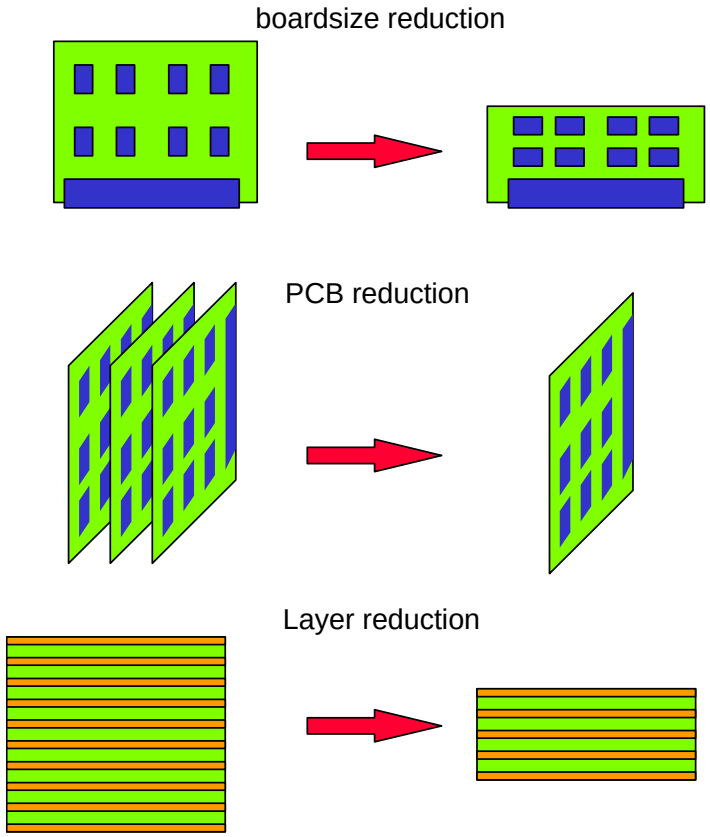
HDI TECHNOLOGY OVERVIEW





HDI Advantages



Although PCB price will increase by adding Microvias, the total system costs can be reduced.

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HDI Advantages

- **Increasing Fan-out**

  No lost routing space on innerlayers.

  More routing space between pads.

- **Less risk during soldering process on;**

  solder-bridge

  solder paste flow away through via holes.

- **Advanced electrical properties**

  Shortest possible connection

- **Advanced thermal properties**

  Thermal Microvias

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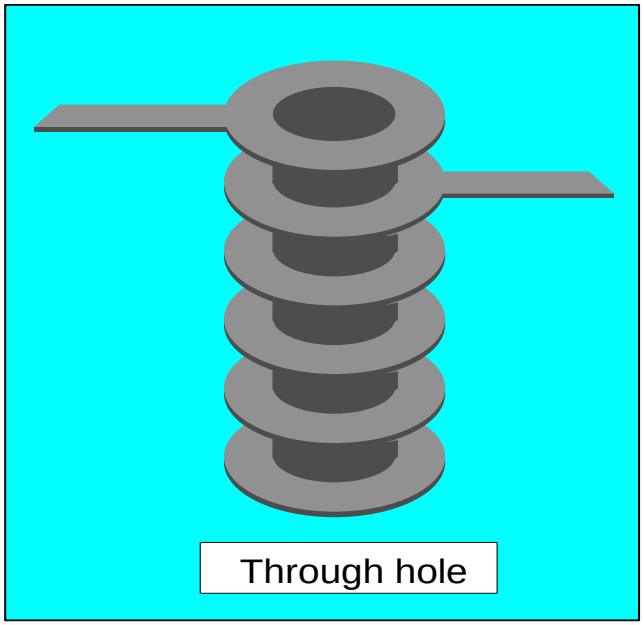
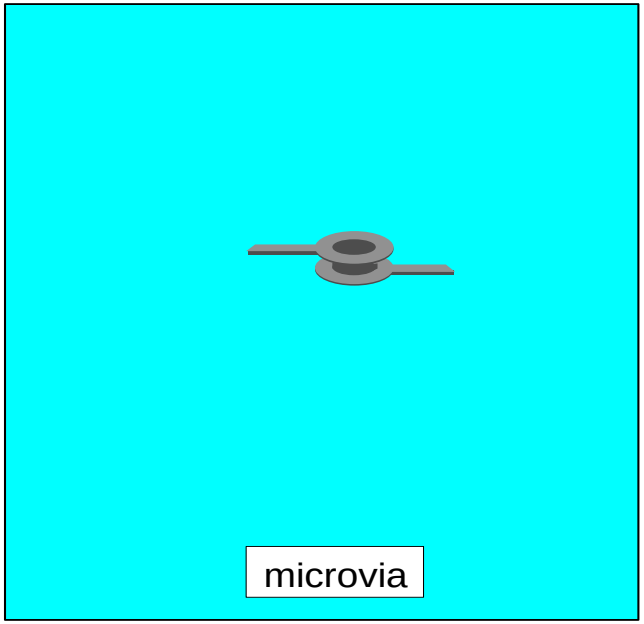
High Density Interconnect



High Inductance



Lower Inductance

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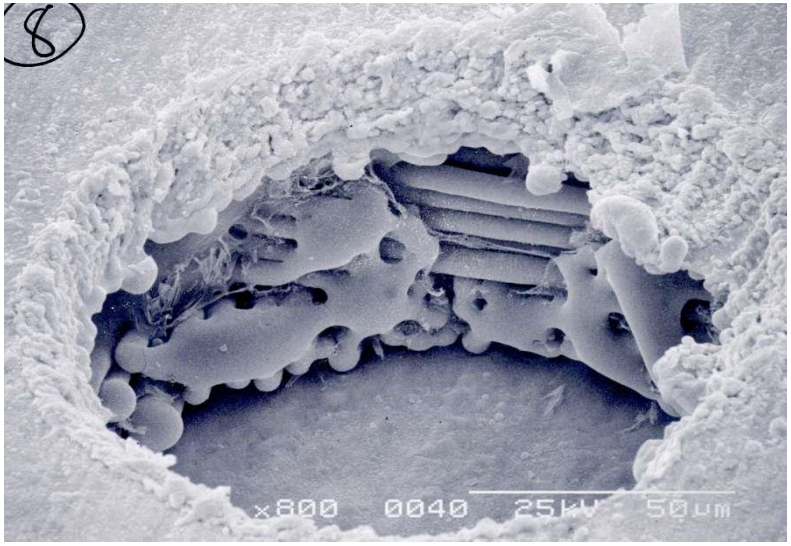
High Density Interconnect

- Dual head Laser
  - UV – copper ablating laser
  - CO_2 – Dielectric ablating laser



Microvia under 800x magnification

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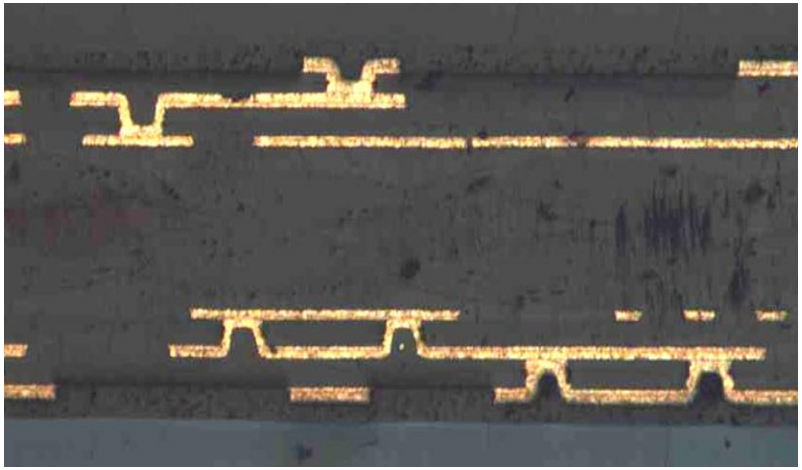
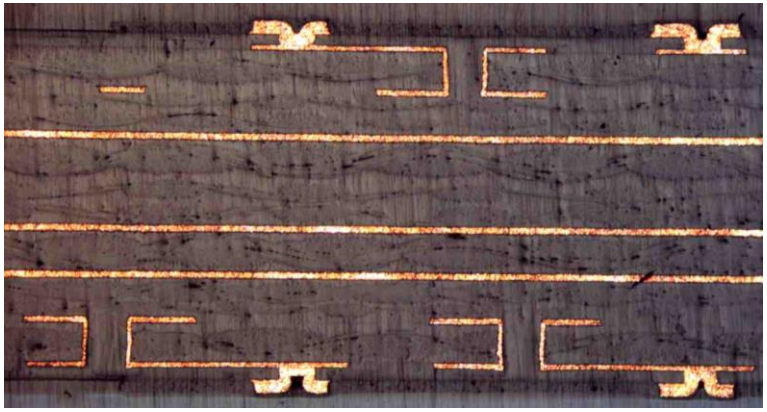
HDI Microsection



Lay up structure: 2+4+2



Lay up structure: 1+1+0+1+1

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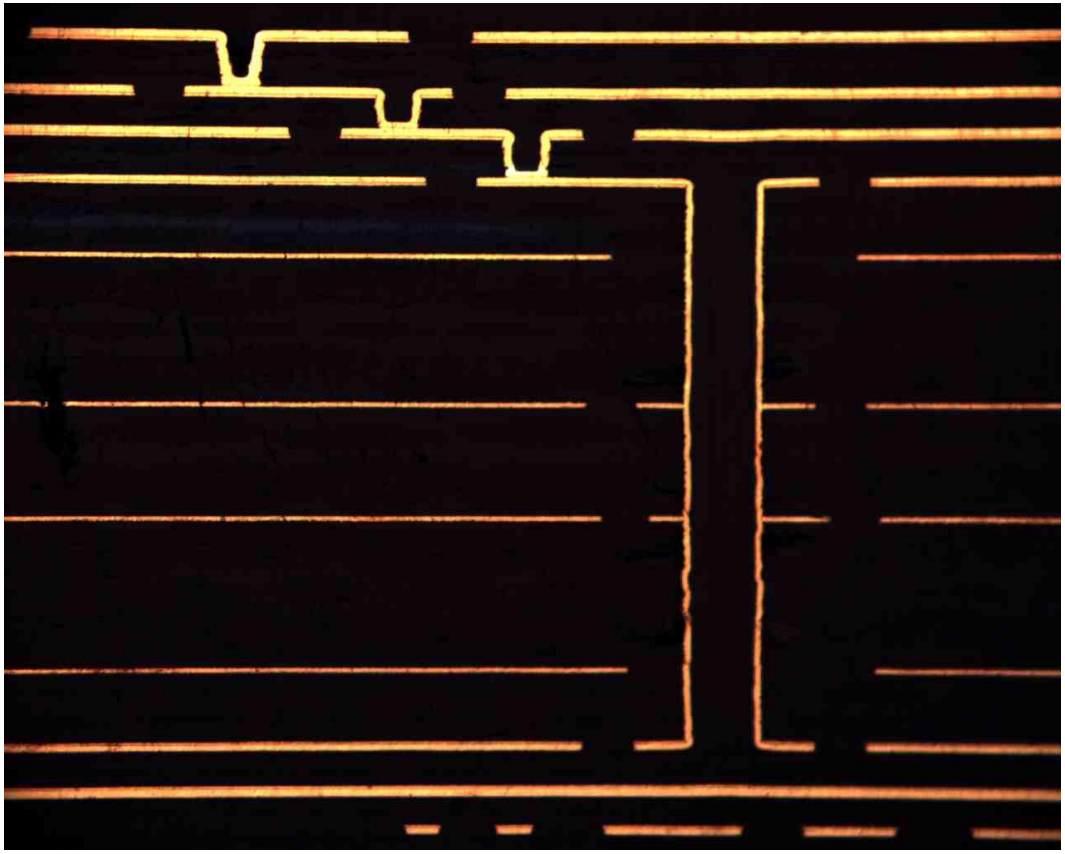
HDI Microsection



Lay up structure: 3 + 6 + 3

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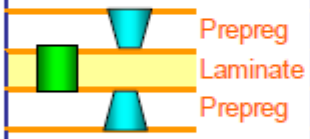
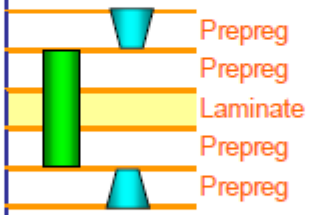
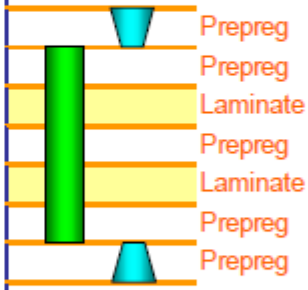
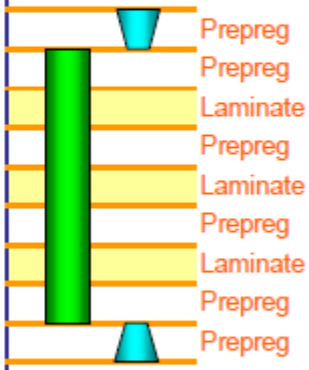
HDI Structure - 1

+1 Stackup

	1+2+1 HDI FCV	1+4+1 HDI FCV	1+6+1 HDI FCV	1+8+1 HDI FCV
				
Lamination	1	2	2	2
Pattern Etching	2	3	4	5
Plating	2	2	2	2
CFM / Laser drill	1	1	1	1
Mechanical drill	1	1	1	1
Buried via filling	1 (optional)	1 (optional)	1 (optional)	1

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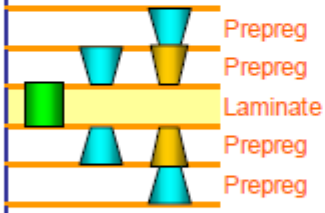
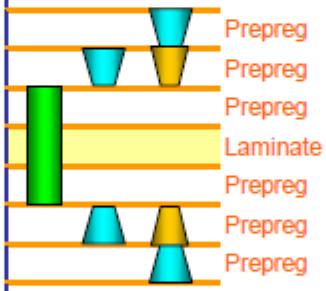
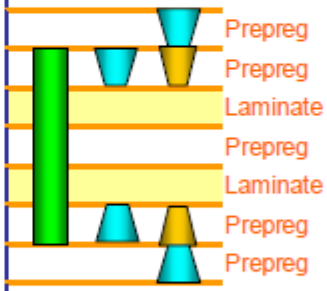
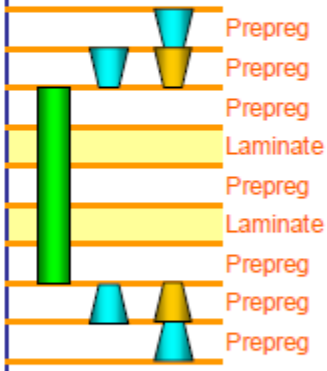
HDI Structure - 2

+2 Stackup

★ *main stream*

	2+2+2 HDI FCV	2+4+2 HDI FCV	2+4+2 HDI simple	2+6+2 HDI FCV
Solid via				
Lamination	2	3	2	3
Pattern Etching	3	4	4	5
Plating	3 (1 Solid via optional)	3 (1 Solid via optional)	2 (1 Solid via optional)	3 (1 Solid via optional)
CFM / Laser drill	2	2	2	2
Mechanical drill	1	1	1	1
Buried via filling	1 (optional)	1 (optional)	1	1

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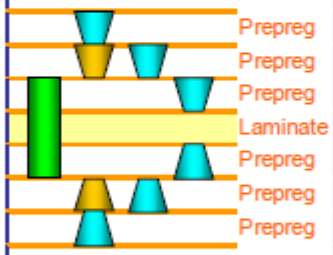
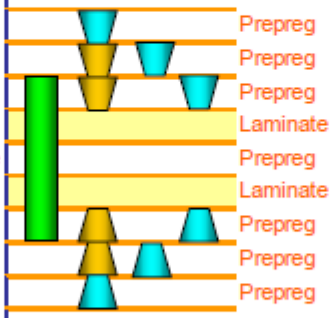
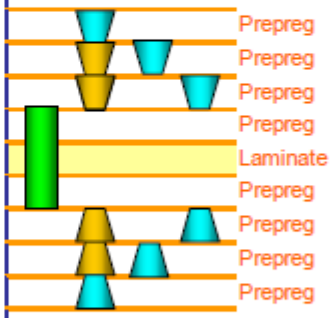
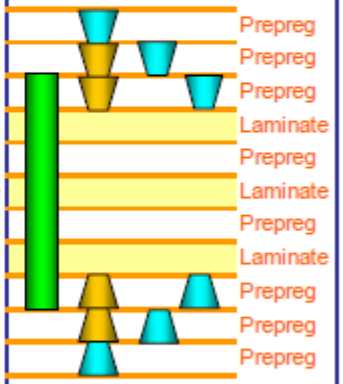
HDI Structure - 3

+3 Stackup

★ *main stream*

	3+2+3 HDI simple	3+4+3 HDI simple	3+4+3 HDI FCV	3+6+3 HDI simple
Solid via				
Lamination	3	3	4	3
Pattern Etching	4	5	5	6
Plating	3 (1 Solid via optional)	3 (2 Solid via optional)	4 (2 Solid via optional)	3 (2 Solid via optional)
CFM / Laser drill	3	3	3	3
Mechanical drill	1	1	1	1
Buried via filling	1 (optional)	1	1 (optional)	1

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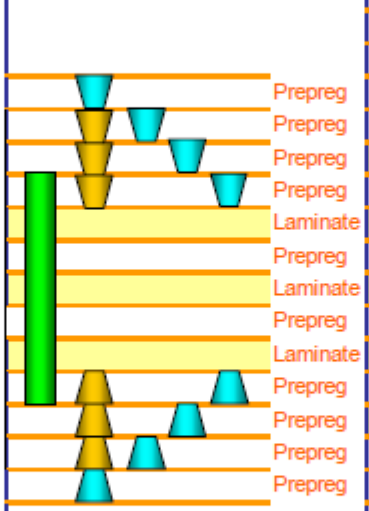
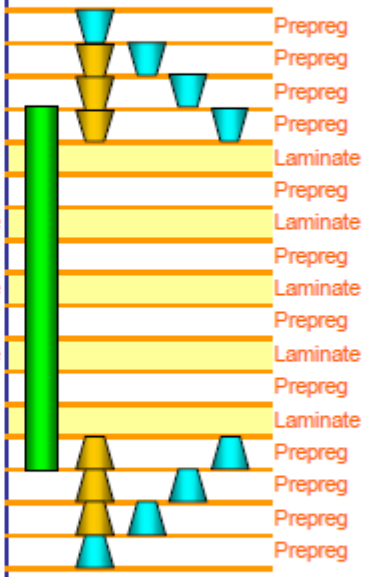
HDI Structure - 4

+4 Stackup

	4+6+4 HDI simple	4+10+4 HDI simple
Solid via		
Lamination	4	4
Pattern Etching	7	9
Plating	4 (3 Solid via optional)	4 (3 Solid via optional)
CFM / Laser drill	4	4
Mechanical drill	1	1
Buried via filling	1	1

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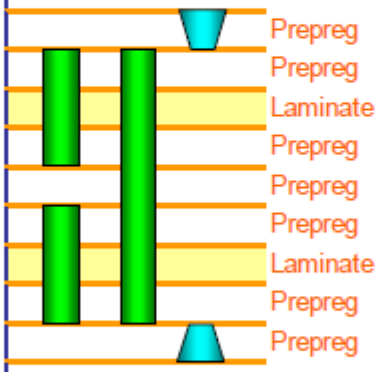
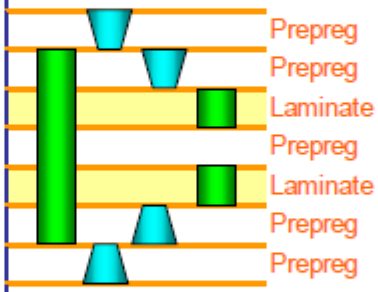
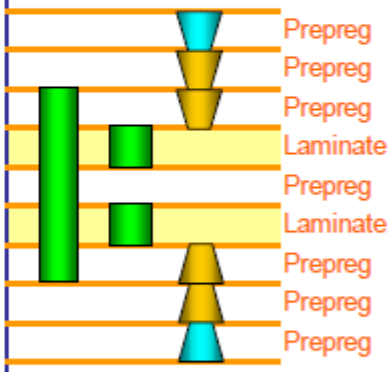
HDI Structure - 5

Multi-BVH Stackup

	1+4+4+1 HDI FCV	2+2+2+2 HDI	3+2+2+3 HDI
Solid via			
Lamination	4	2	3
Pattern Etching	6	4	5
Plating	4	4	5 (2 Solid via)
CFM / Laser drill	1	2	3
Mechanical drill	3	3	3
Buried via filling	1	1	1

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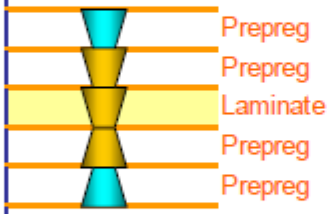
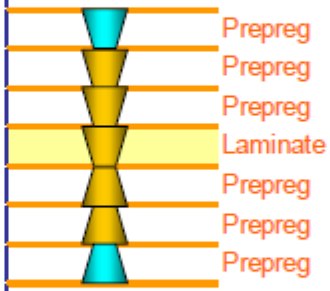
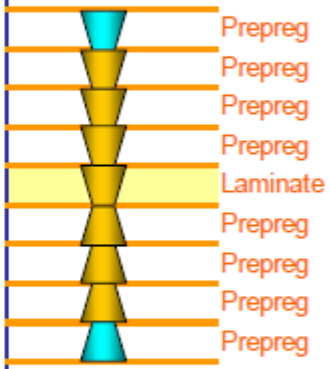
HDI Structure - 6

★ *main stream*

Anylayer Stackup	6L Anylayer	8L Anylayer	10L Anylayer
Solid via			
Lamination	2	3	4
Pattern Etching	3	4	5
Plating	3 (2 Solid via)	4 (3 Solid via)	5 (4 Solid via)
CFM / Laser drill	3	4	5
Mechanical drill	0	0	0
Buried via filling	NA	NA	NA
Board thickness	0.55~0.6mm	0.7~0.8mm	0.9~1.0mm

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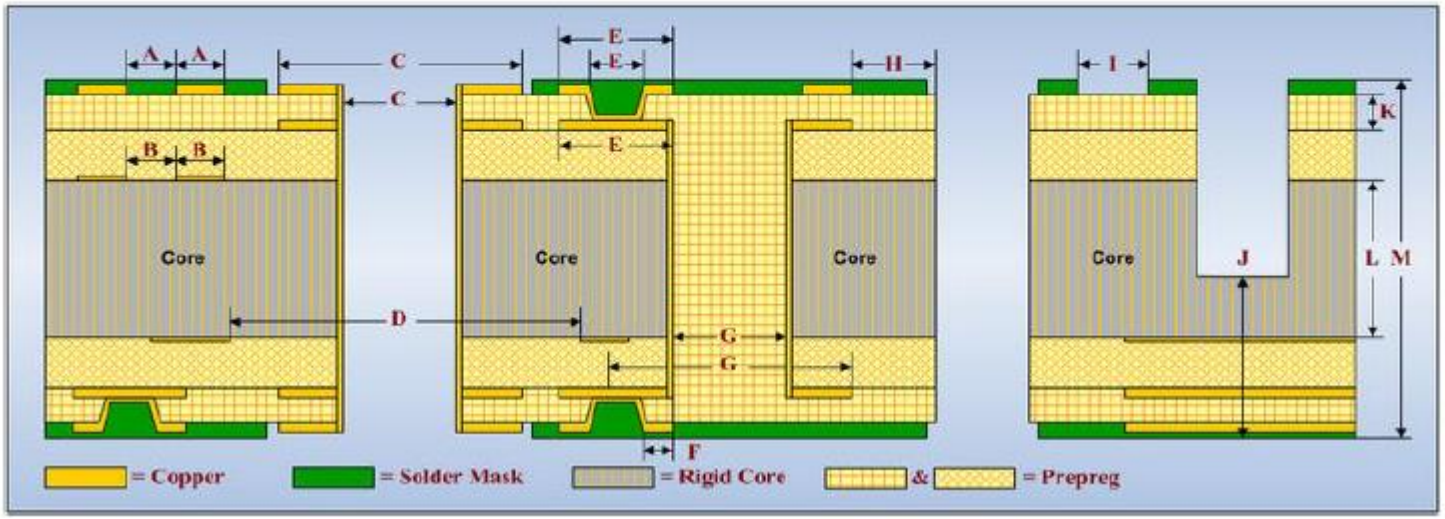
HDI PCB Design Guide



Sy.	Feature	Standard	Advanced
A	Min. LW/LS on plated layer	75/75	50/50
B	Min. LW/LS - Cu foil (18um)	75/75	50/50
C	Min hole/land - PTH	250/500	200/400
C1	Max. aspect ratio for PTH	6	8
C2	Max. aspect ratio for PTH - solid via	4	7
C3	POFV hole size (single hole size)	200~700	1000 Max.
C4	Max. aspect ratio for POFV	5	7
D	Plane clearance on inner layer	Fhs + 500	Fhs + 400
E	Min. laser via/pad (capture/target)	125/300	100/250
E1	Max. aspect ratio for HDI layers	0.6	0.8
F	Min. u via edge to buried via edge	150	125
G	Min. hole / land – buried via	200/400	150/350

Sy.	Feature	Standard	Advanced
H	Min. conductor to unplated hole	250	200
I	Min. soldermask opening size	200	150
J	Control Depth Rout/ tolerance	+/-100	+/-50
K	Max. HDI dielectric thickness	75	80
L	Min. core thickness - non-plated	75	50
L1	Min. core thickness - plated	75	65
M	Max. board thickness (mm)	2	2.4
M1	Min. board thickness (mm) - 1+2+1	0.4	0.35
-	SM registration	50	38
-	Max. layer count	14L	18L
-	Rout / V_cut outline tolerance	125	100

Unit: um

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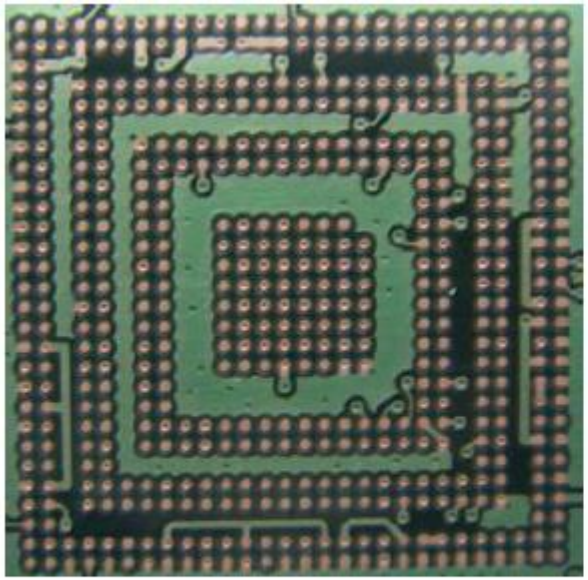
Design for Manufacture

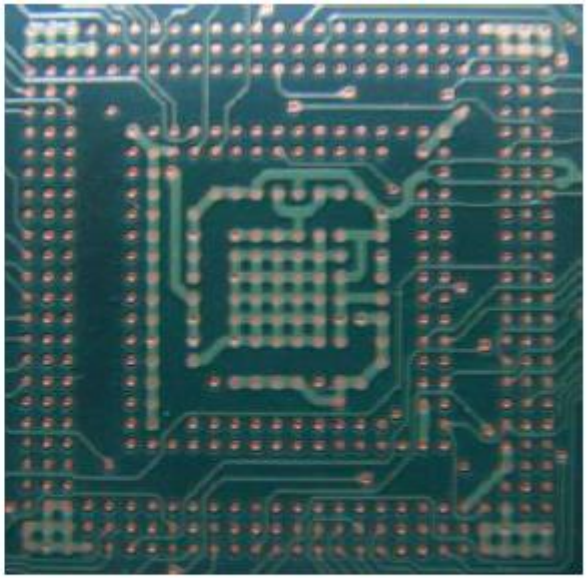
0.5mm pitch BGA

Do



- No trace go through BGA pads

Don't



- Trace go through BGA pads
- Smaller BGA pad size, tough PCB and SMT process control

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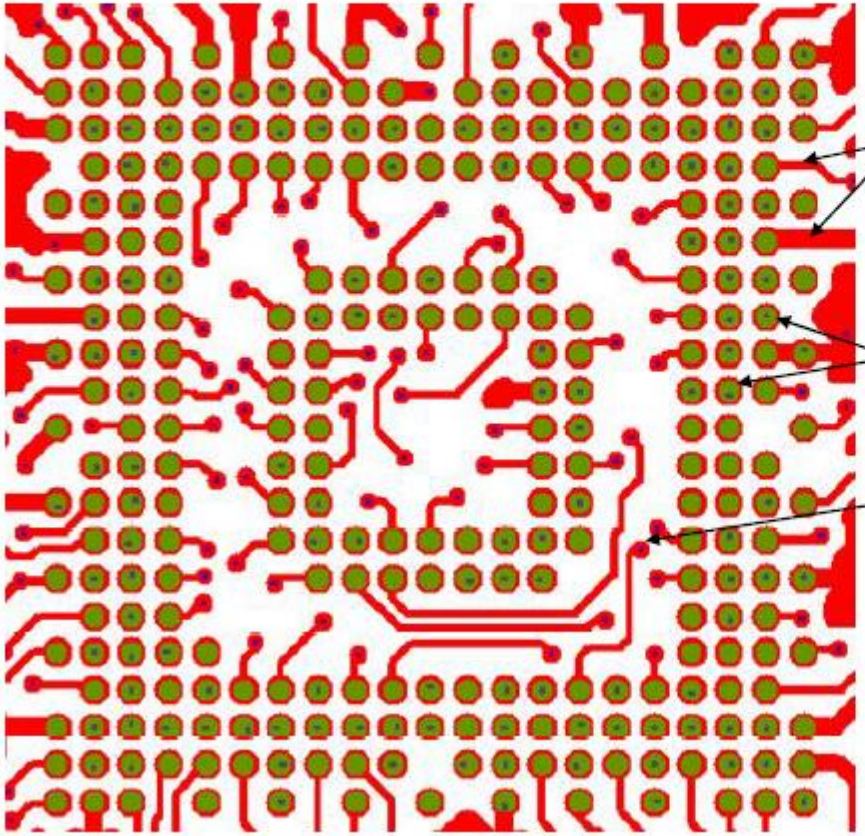
Design Suggestion for BGA Layout

- 0.5mm pitch BGA



No trace go through pads:

1. Remove dummy pad to go through the trace.
2. Use microvia to fan out inner row pad.
3. Leave empty row inside BGA area to fan out trace and microvia.

Red: pattern
Green: SM opening
Blue: micro via

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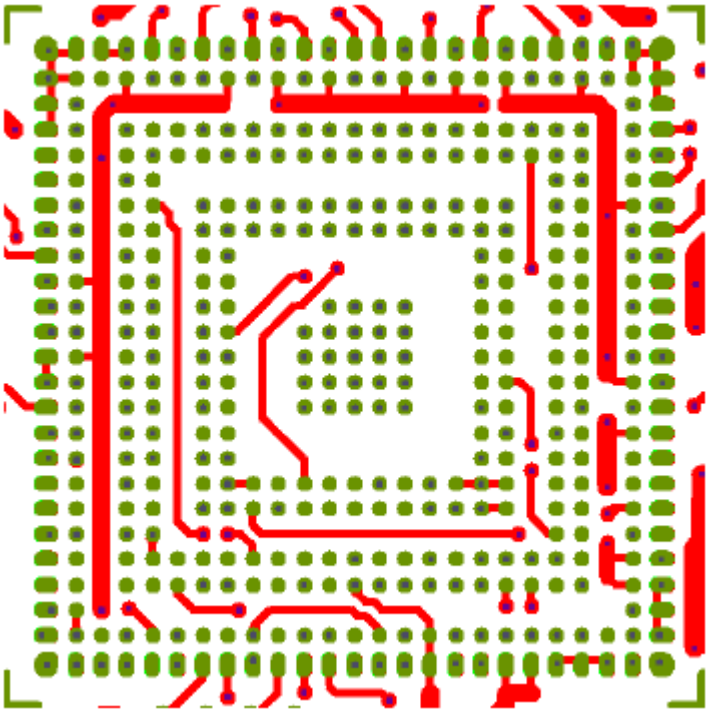
Design Suggestion for BGA Layout

- 0.4mm pitch BGA design



For Outer Layer :

1. Use solid via to improve the quality of solder joint.
2. No PTH via design to comply with solid via process & fine line control. (Tooling hole with via size bigger than 0.5mm isn't limited)
3. Avoid any trace pass through adjacent BGA pad.

For Inner Layer :

1. Avoid trace pass through adjacent pad to prevent 2 mil trace design, go to next layer.
2. Do 3/3mil LW/LS better.

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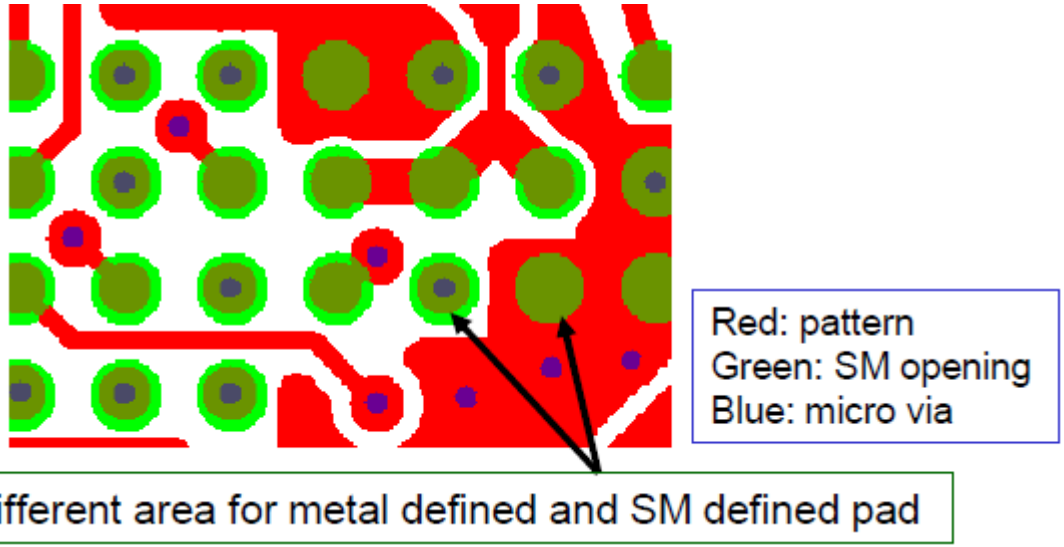
Design Suggestion for BGA Layout

- Size of BGA Ball Pad

1. Don't mix the Metal defined and SM defined on the same BGA area. This would cause different pad size and may have an impact when assembly. Better to shrink the SM open for ground ball pad to keep the same solder area.
2. Put the microvia on the center of the BGA pad (metal defined pad).



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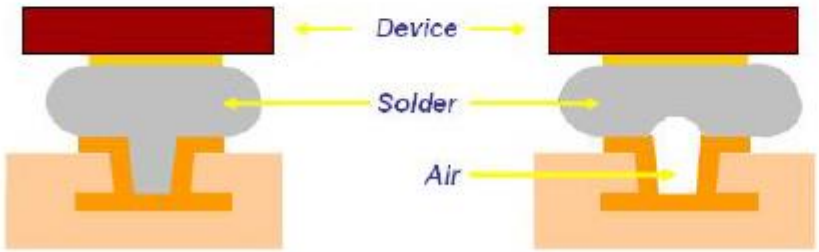
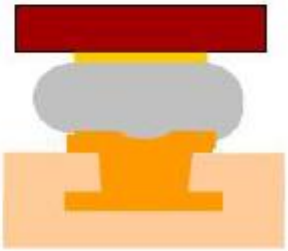
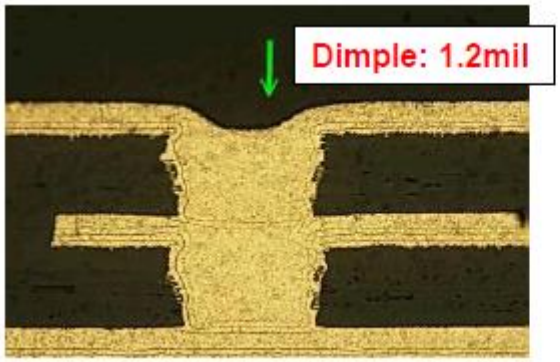
Design Suggestion for Outer-Layer Solid via

- Advantage for Assembly

The Copper filled via improves quality of solder joint.

Conventional microvia	Solid via
	



Via dent control: 30um Max.

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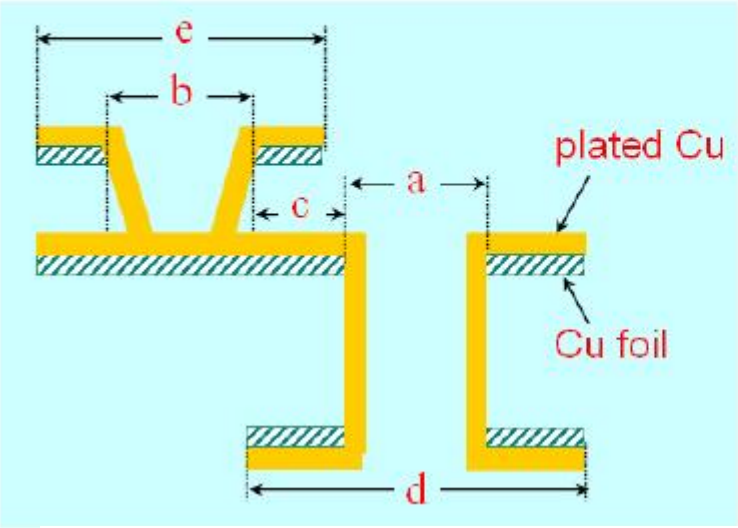
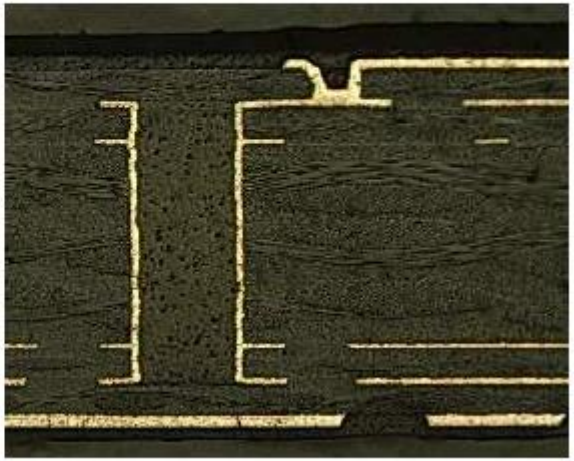
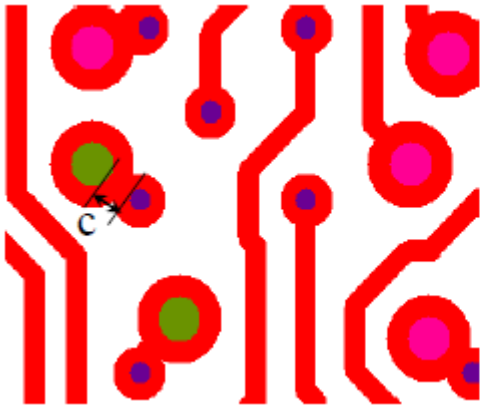
Design Suggestion for Staggered Microvia & Buried via







a: Buried via size : 200um (150um min.)
b: Microvia size : 125um (100um min.)
c: Distance between buried via
edge to microvia edge : **125um min.**
d. Buried via pad size: 450um (400um min.)
e. Microvia pad size : 300um (250um min.)

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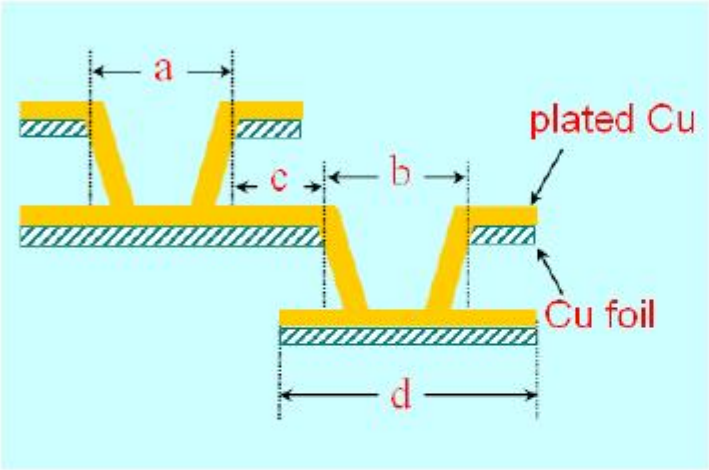
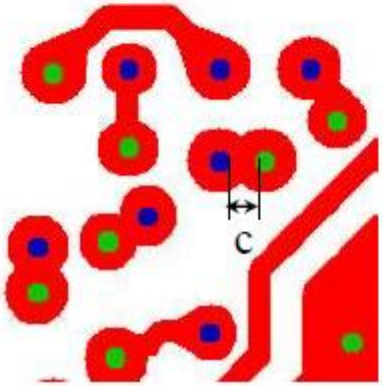
Design Suggestion for Staggered Microvia





a: Top layer microvia size : 125um (100um min.)
b: Bottom layer microvia size : 125um (100um min.)
c: Distance between microvia
edge to microvia edge : **100um min.**
d. Microvia pad size : 300um (250um min.)

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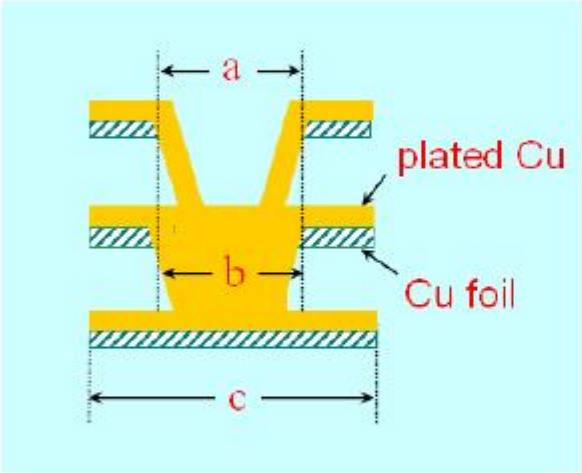
Design Suggestion for Solid Stacked Microvia



a: Top layer Microvia size : 125um (100um min.)

b: Bottom layer Micro via size : 125um (100um min.)

c. Microvia pad size : 300um (250um min.)

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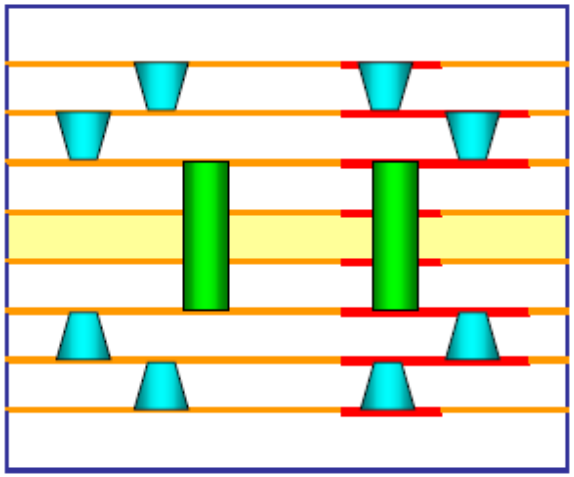
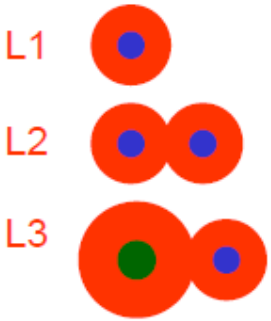
Advantage of Non-PTH Design

1. More space for layout usage on outer layer due to small pad size of microvia.
2. Shorten processes, reduce lead time.
3. Reduce inner layer short & hole breakout yield loss.
4. Better reliability level
5. Same level of grounding/shielding function.
6. Better surface Cu thickness control and more compliant with solid via requirement on outer layer.



e.g.: 2+4+2 structure
Remove PTH (for interconnection), use microvia + buried via instead of PTH.



LD pad: 250um min.

NC pad: 450um min.

LD pad size is much smaller than NC pad size

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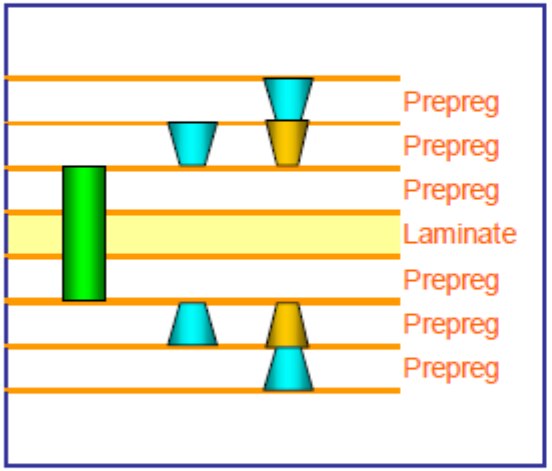
Design for Manufacture

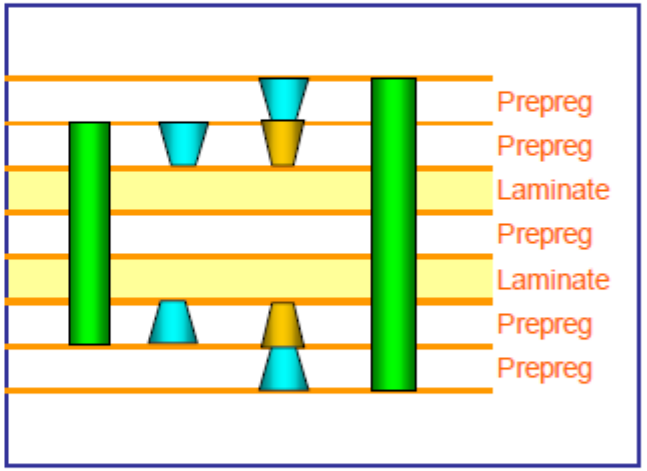
Structure

Do



- Microvia & mechanical drill fan out in different layer.
- More space for layout usage on L1/L2/L7/L8

Don't



- Microvia & mechanical drill fan out in the same layer.
- Align both buried via and microvia on L2/L7, align both through via and microvia align on L1/L8.

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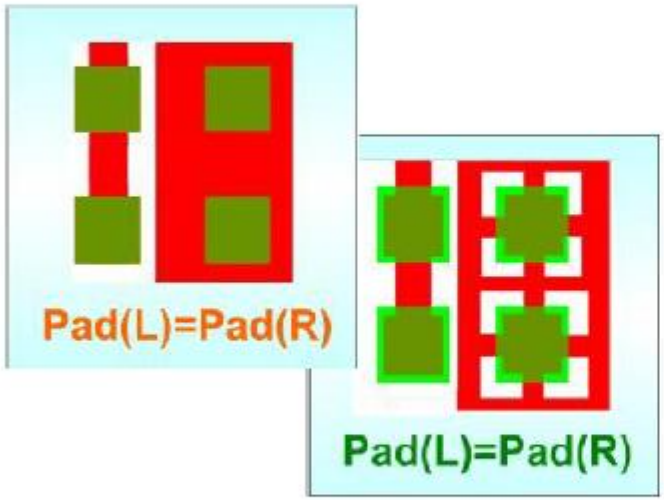
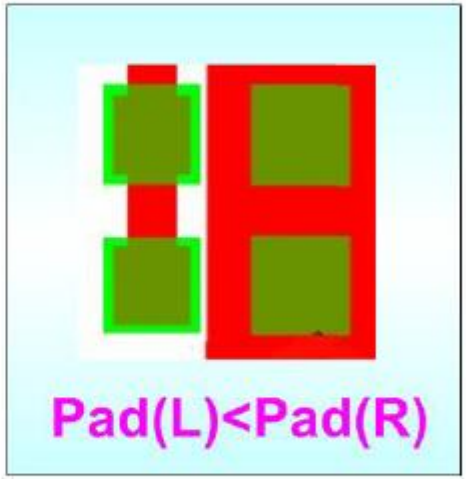
Design Suggestion for 0201 Chip Layout

Do *0201 Layout* **Don't**



- The SMD PAD with the same define (both pads with Solder mask define or copper define)



- The SMD PAD with different define (left pad with copper define, right pad with solder mask define)

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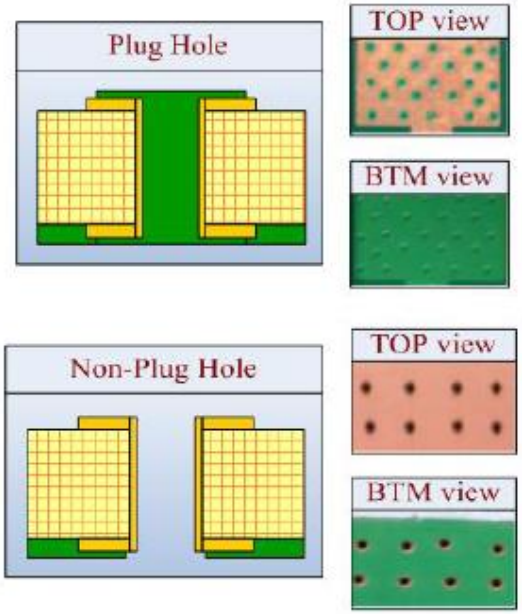
Design for Manufacture

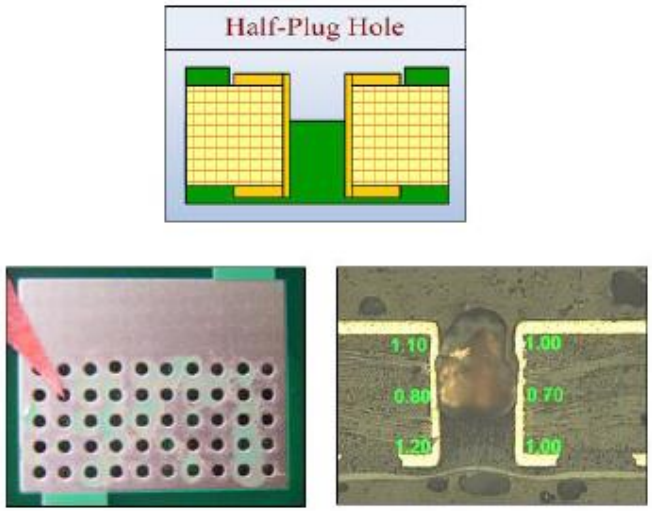
Plug through via

Do



- Exposed or Covered with S/M on both sides
- Ensure the via quality

Don't



- Covered with S/M only on one side
- Potential risk of S/M residual and chemical corrosion.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- Introduction to Flexible and FlexRigid PCBs

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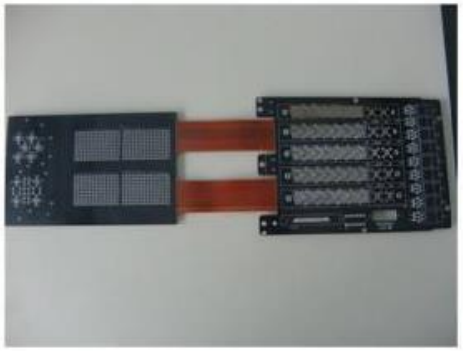

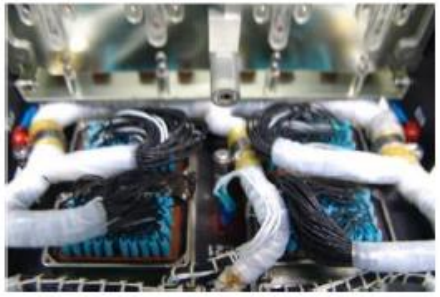

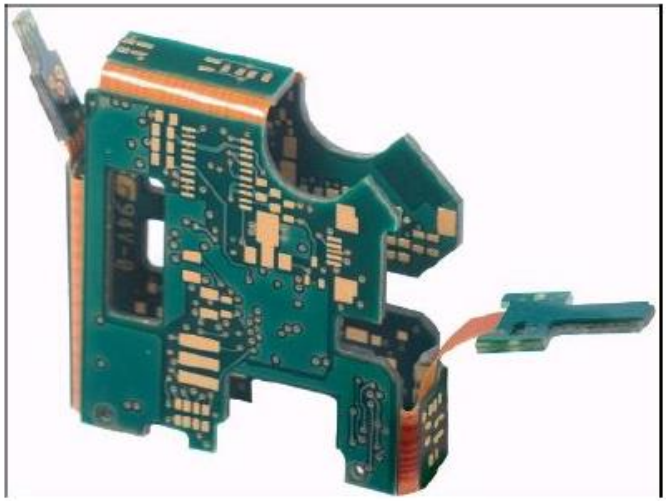

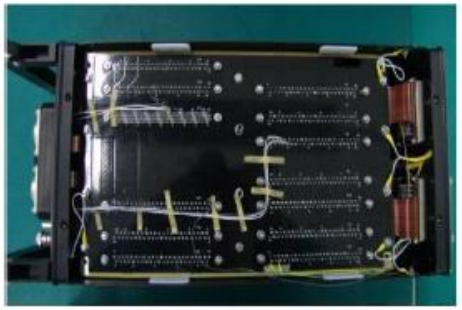

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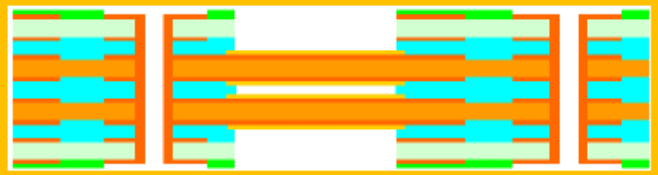
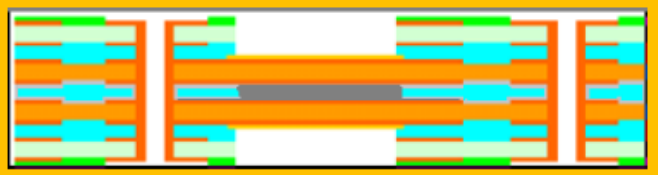
Symmetrical structure

Structure1 : Single FCCL Symmetry structure

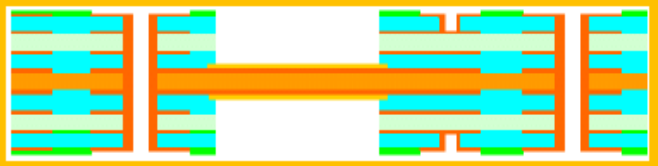
Structure2 : Book structure



Structure3 : Multi-FCCL Symmetry structure



Structure4 : HDI

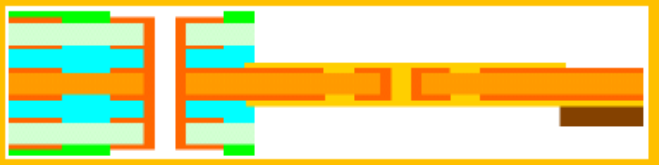


Unsymmetrical structure

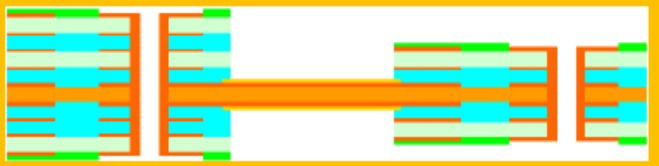
Structure5 : Unilateral Unsymmetrical structure

Structure6 : Vertical Unsymmetrical structure

Structure7 : Fly tail structure



Structure8 : Horizontal Unsymmetrical structure



Copper FR4 PI Coverlay No flow PP Adhesive Solder mask Stiffener

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Why Consider Flex?

- **Smaller**, smaller, smaller –A reduction in space within the design. This affects both size and weight of the overall assembly.
- By replacing hard wiring you increase the reliability and now deliver a robust design package.
- The assembly requires a dynamic flex cycle.
- Flex can be custom designed to achieve impedance requirements.
- You can improve heat dissipation and allow more air flow inside the box.
- Folding is required.
- Folding, forming and component assembly can take place all in one platform.

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Application Types

–Static: Not meant to flex

–Flex to Install or bend and stay:
Only meant to flex on limited basis. To install or replace and repair.

–Dynamic: Depending on flex construction and conditions this could result in >1M flex cycles**.**

Application Attributes

–Controlled Impedance, by altering material thicknesses you can achieve impedances typically in the 50 –100 ohm range, with a tolerance of 5 –10%. Depending on construction you can affect flexibility and limit the dynamic characteristics.

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Application Attributes Cont'd

–Single Sided Flex: This is a single copper layer/polyimide clad construction with a polyimide/adhesive coverlayer laminated to one side to allow access on one side only.

–Dual Access Flex: (Back Bared Flex) This is the same construction as single sided flex but openings are created in the base polyimide/adhesive layers to allow access to the copper on both sides.

–Double Sided Flex: This is a dual copper clad consisting of two layers of copper separated by adhesive and polyimide. Plated through holes (vias) complete the continuity from layer to layer.

–Multilayer Flex: This is a combination of single sided and double sided clads to achieve the total layer count desired. Vias are incorporated to connect all layers.

–Rigid Flex: This can be single or multiple layers of flex sandwiched between standard PCB materials to create rigid and flexible portions.

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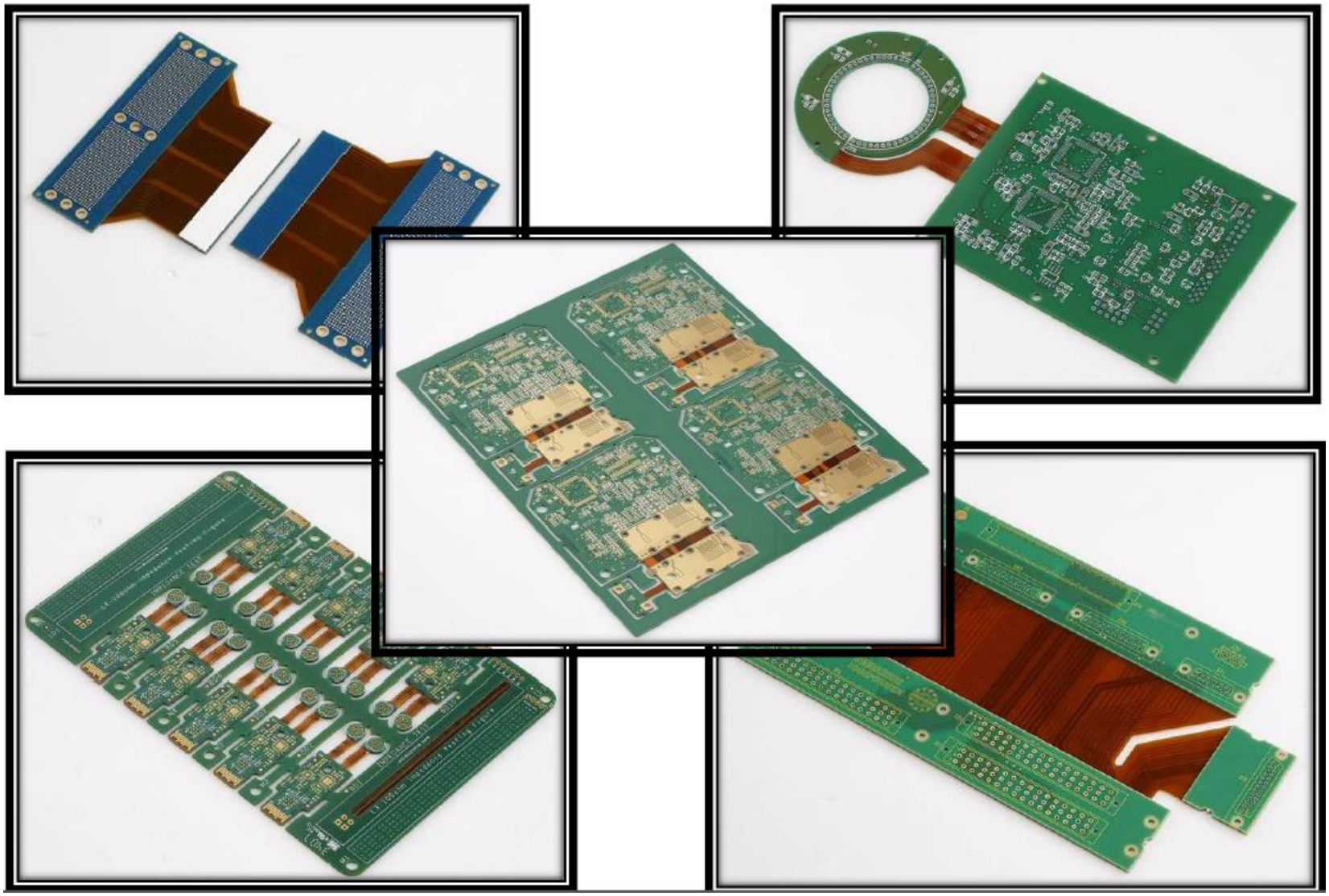

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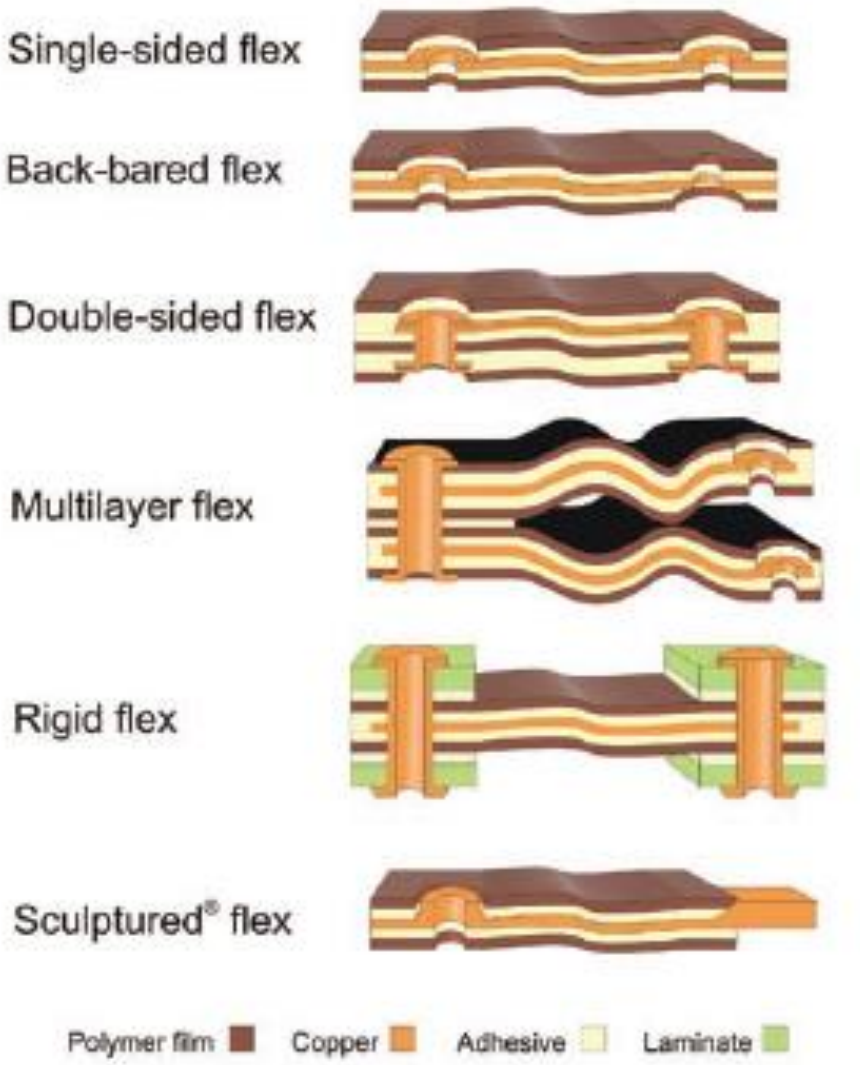
Application Attributes Cont'd



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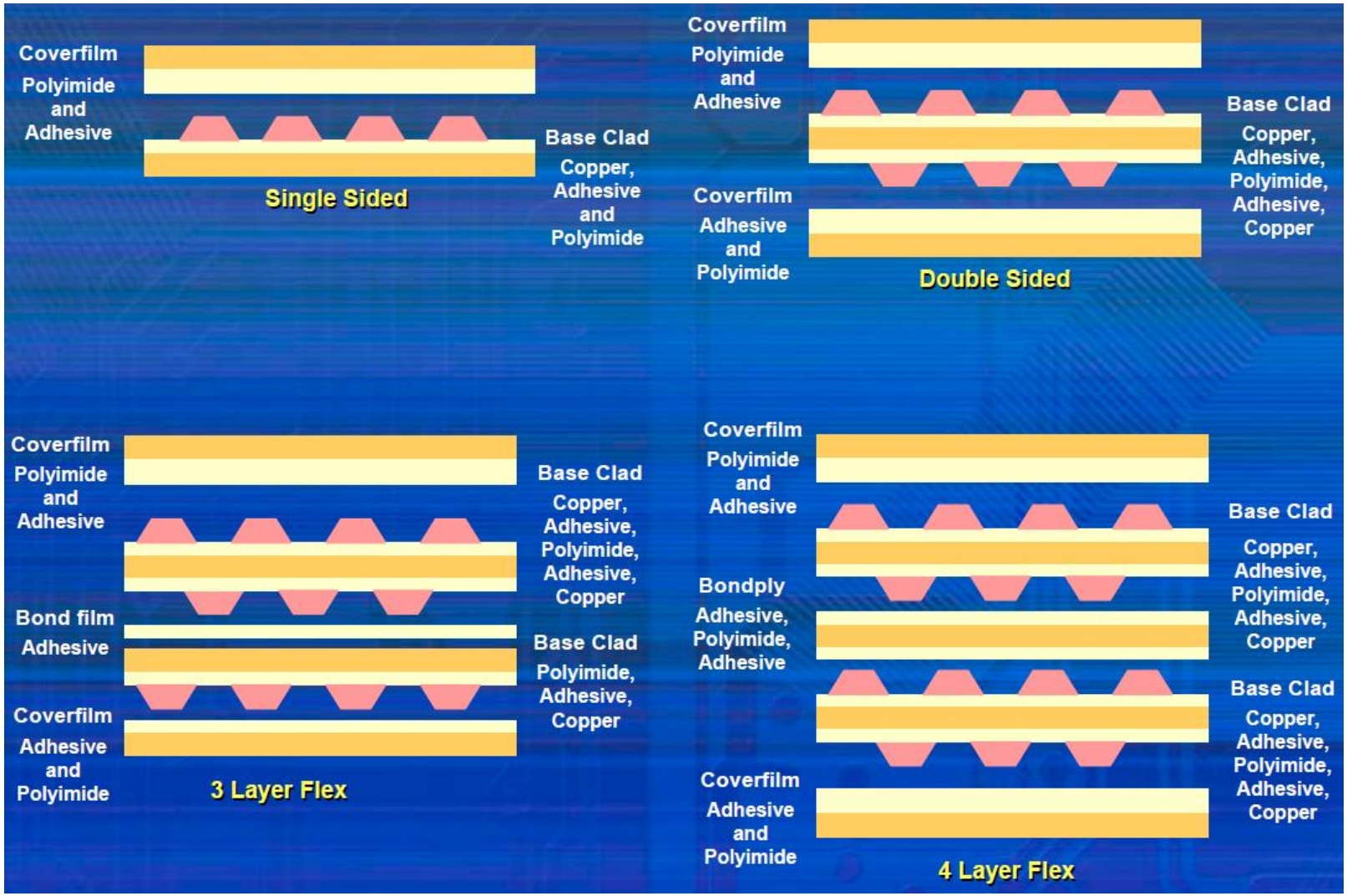

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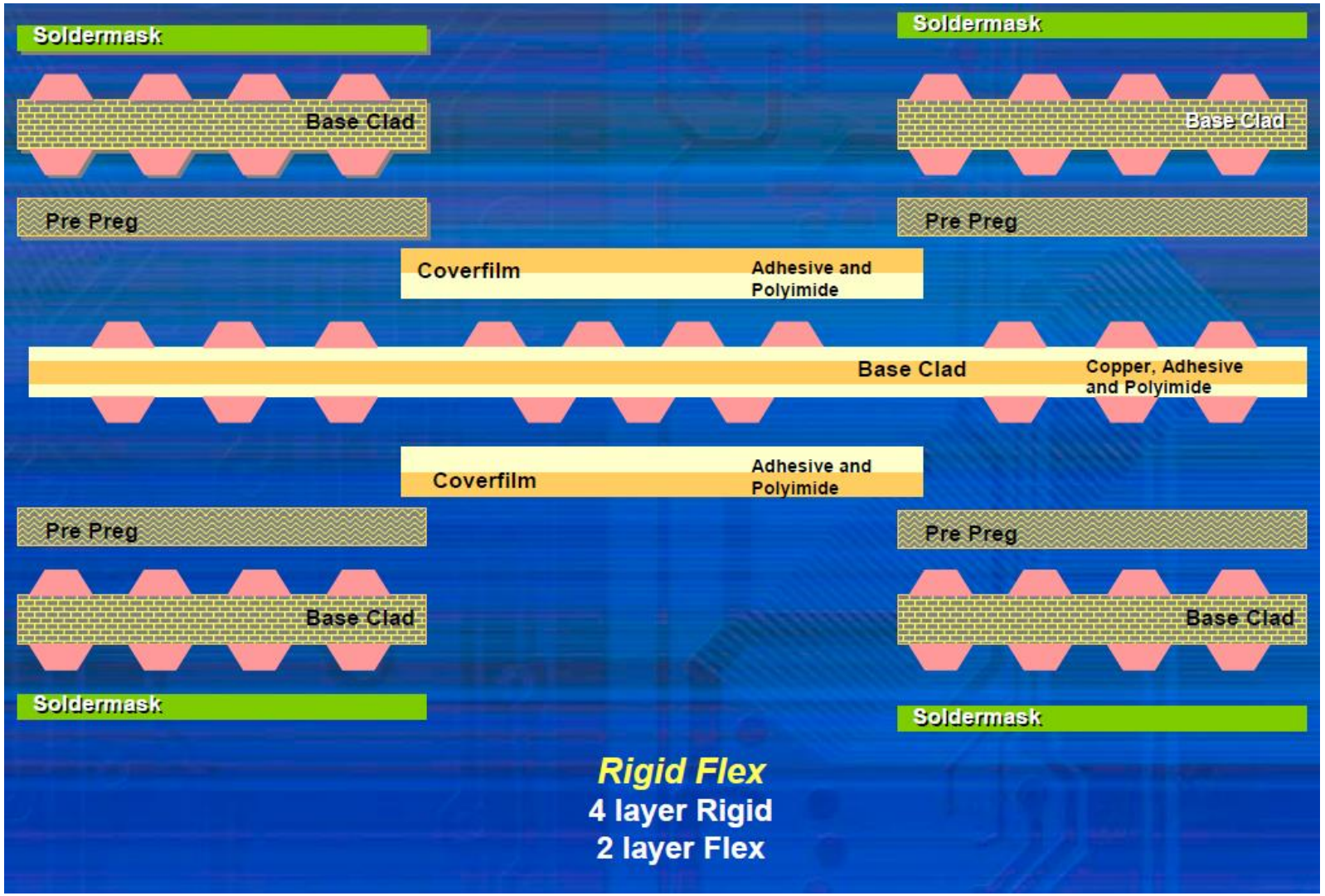

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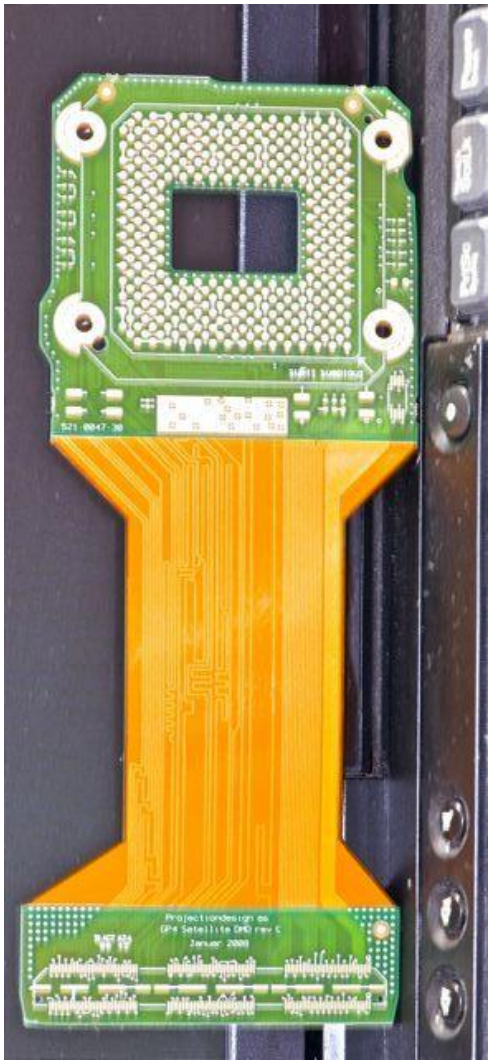
Total 5 (7) rigid layers And 3 flex layers



LAYER	SPECIFICATION	Tickness
1L	Copper foil	35,0 µm
	FR-4 CORE	500,0 µm
	No flow PRE-PREG	65,0 µm
	Coverlay	37,5 µm
2L	Base Cu	17,5 µm
	Base PI (Polyimide + Adhesive)	41,0 µm
	Bonding Sheet	25,0 µm
	Coverlay	37,5 µm
3L	Base Cu	17,5 µm
	Base PI (Polyimide + Adhesive)	94,0 µm
4L	Base Cu	17,5 µm
	Coverlay	37,5 µm
	No flow PRE-PREG	65,0 µm
	FR-4 CORE	500,0 µm
5L	Copper foil	35,0 µm

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Design Tips

- For first time designers and engineers it is a good idea to become familiar with all specifications that govern Flex Circuit manufacturing.
    - IPC (www.ipc.org)
    - IPC-2223 and IPC6013

- How do you want your flex to act or perform?

- Develop your schematic.
    - Layer counts and trace densities will be calculated
    - Identify power, signal and ground traces
    - Understand your current requirements
    - Calculate conductor width needs•

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Flex Circuit Related Specifications

–IPC-2223 Sectional Design Standard for Flexible Printed Boards
- This specification has the most comprehensive tips for creating your design. This presentation is based on this specification.

–IPC-600 Manufacturability and Acceptability of Printed Circuits

–IPC-FC-231 Flexible Bare Dielectrics for use in Flexible Printed Wiring

–IPC-FC-232 Adhesive coated dielectric films for use in cover sheets for Flexible Printed Wiring

–IPC-FC-233 Flexible Adhesive Bonding Films

–IPC-FC-241 Metal clad flexible dielectric for use in fabrication of Flexible Printed Wiring

–IPC-4562 Metal Foil for Printed Wiring Applications

–IPC-T50-D Terms and definitions definitions

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- **Material selection**
  - Attributes to consider flexibility, impedance, emi, to name a few.
  - Thinner material does not equate to cheaper. In most cases the thinner the copper and or polyimide/adhesive, the more expensive it is.

- **Component termination method**
  - Surface mount, through hole, etc…

- **Level of electrical testing needed to assure that your design is acceptable.**
  - Open and short test
  - Full functional test of all components•

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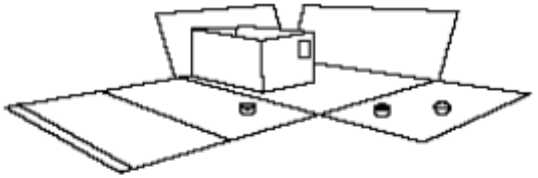
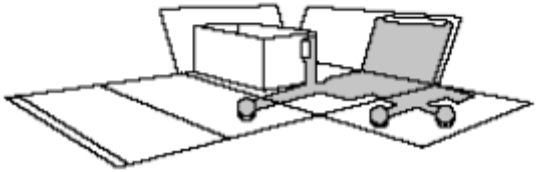
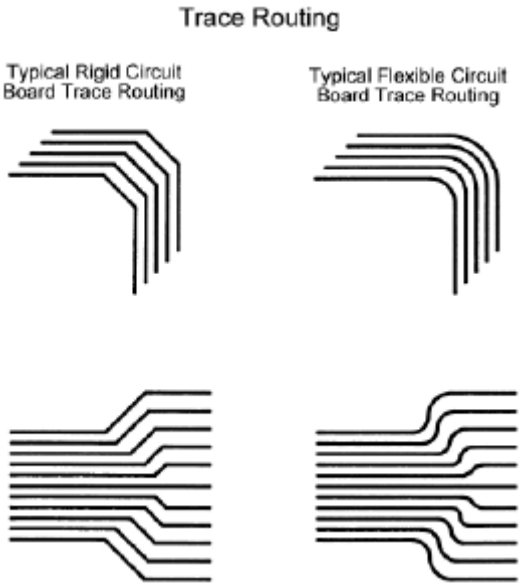


- Your ultimate design is a collaboration across multiple engineering disciplines, Electrical, Mechanical and CAD.



– **Paper Doll-** This term is used in conjunction with mechanical mock ups. This is a cost effective way of demonstrating form and fit and in most cases a good safety net to catch potential mechanical issues.



– **Trace/Space-** While this is one of the building block of your design, special care must be given to the actual trace structure. Care must be taken to avoid sharp corners more typical of a PCB design

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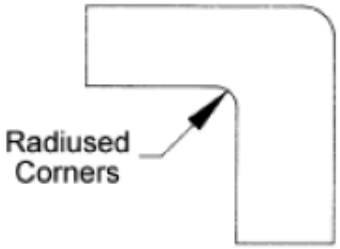
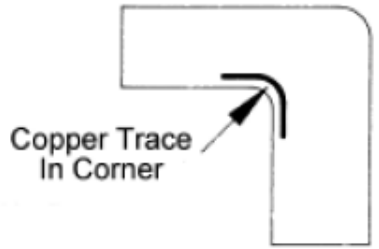
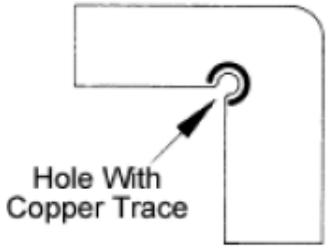
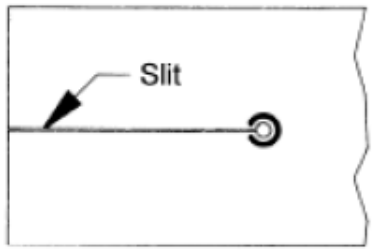
Tear Stops- All inside corners MUST have a radius. In these cases a tear stop should be incorporated into the design as an added safety feature to guard against tearing or cracks propagating across a flex circuit.





Shields and Planes- Cross hatching can be used to create a shield or plane when flexibility is still a requirement. Shields can be created using copper or they can be screened on using conductive silver epoxy.





Grain Direction- When designing dynamic flex the copper grain direction must be taken into account. Rolled Annealed copper has a specific grain direction. To maximize the copper life you must flex in the direction of the grain.

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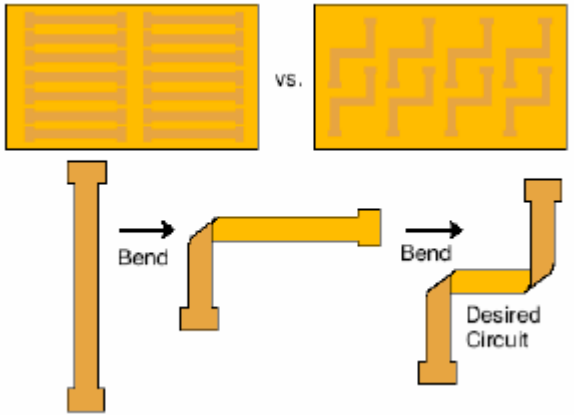
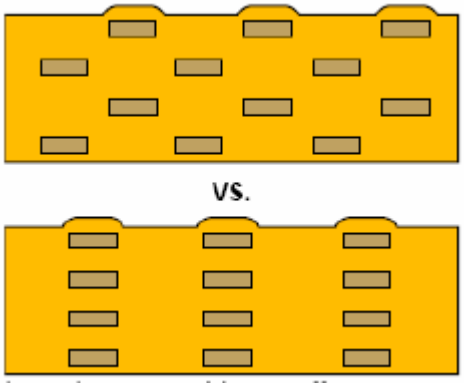
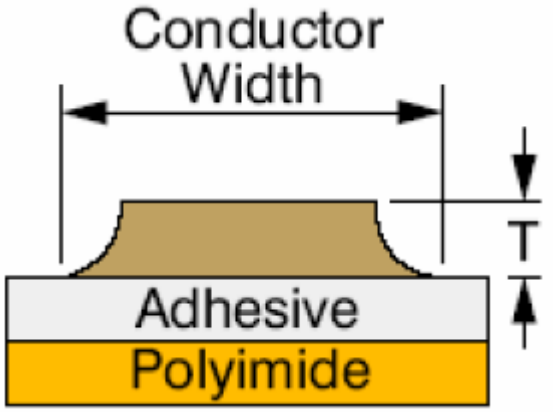


- **Material Utilization-** This is the number one cost contributor to your design. When running product, most shops use a panel format. The more up per panel the lower the cost.
  Your goal should be the smallest form factor as possible. This can be achieved several ways but one of the most creative ways is to incorporate folds into your design.



- **I-Beam-** When routing your conductor in a double sided flex it is best to stagger the conductors to prevent an I-Beam effect. With the conductors stacked you run the risk of compression issues when bending to install.



- **Conductor aspect-** In a perfect world that rule of thumb is 5 times the conductor thickness. This is a safe rule, however your design will be pushed to ever increasingly smaller trace and space geometries.

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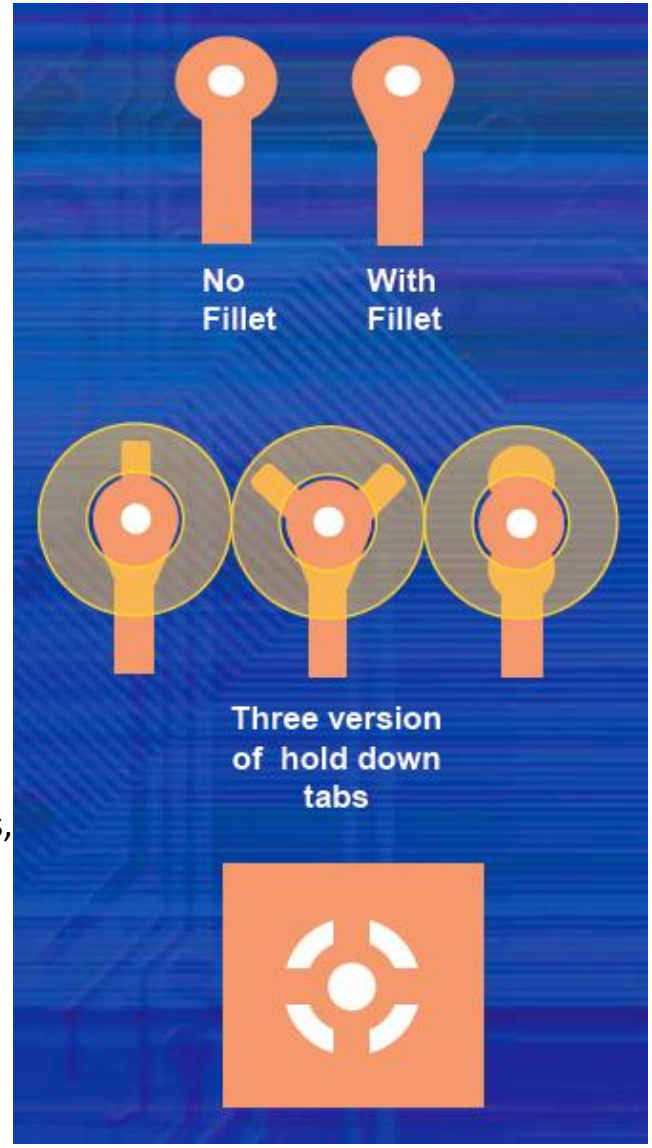
-Filleted pad/ Hold Down Tabs (Flex-circuits)

-A major location for failure in a flex circuit is the interface between the board trace and the pad at the end. It is extremely critical that these interface points have transitional areas more commonly referred to as fillets.
Hold down tabs add robustness to the copper pad. The additional hold down tab keeps the pad anchored during any subsequent assembly and rework.



- Solder Relief

-When placing pads in large copper traces or ground planes, solder relief pads should be created to allow for easier soldering of components. Large copper areas will sink heat away and cause cold or weak solder joints.

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Electrical Considerations

- Predictable electrical characteristics make flex boards an ideal choice for high-speed signal transmission.

- Uniform spacing between tracks and grounds, continuous shield layers, and repeatable geometries are features that help control impedance and reduce crosstalk.

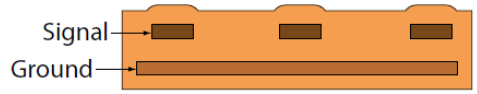
- With flex boards, you can eliminate connectors and other transitions that contribute to signal attenuation.

- Manufacturers can provide tight tolerances on track width, spacing, and distance to ground layers in order to meet your impedance requirements.

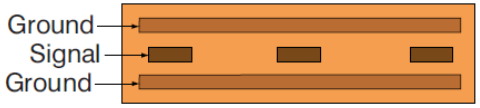
- Actual impedance will also depend on the board's shape after installation.

- Contact your manufacturer for advice on designing boards to specific electrical characteristics.

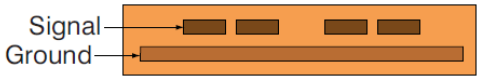
• Microstrip - a single ground plane beneath the signal lines.



• Stripline - dual ground layers above and below the signal lines.



• Edge coupled differential pairs – traces are adjacent to each other in the same plane with tightly controlled width and spacing, ground plane optional.



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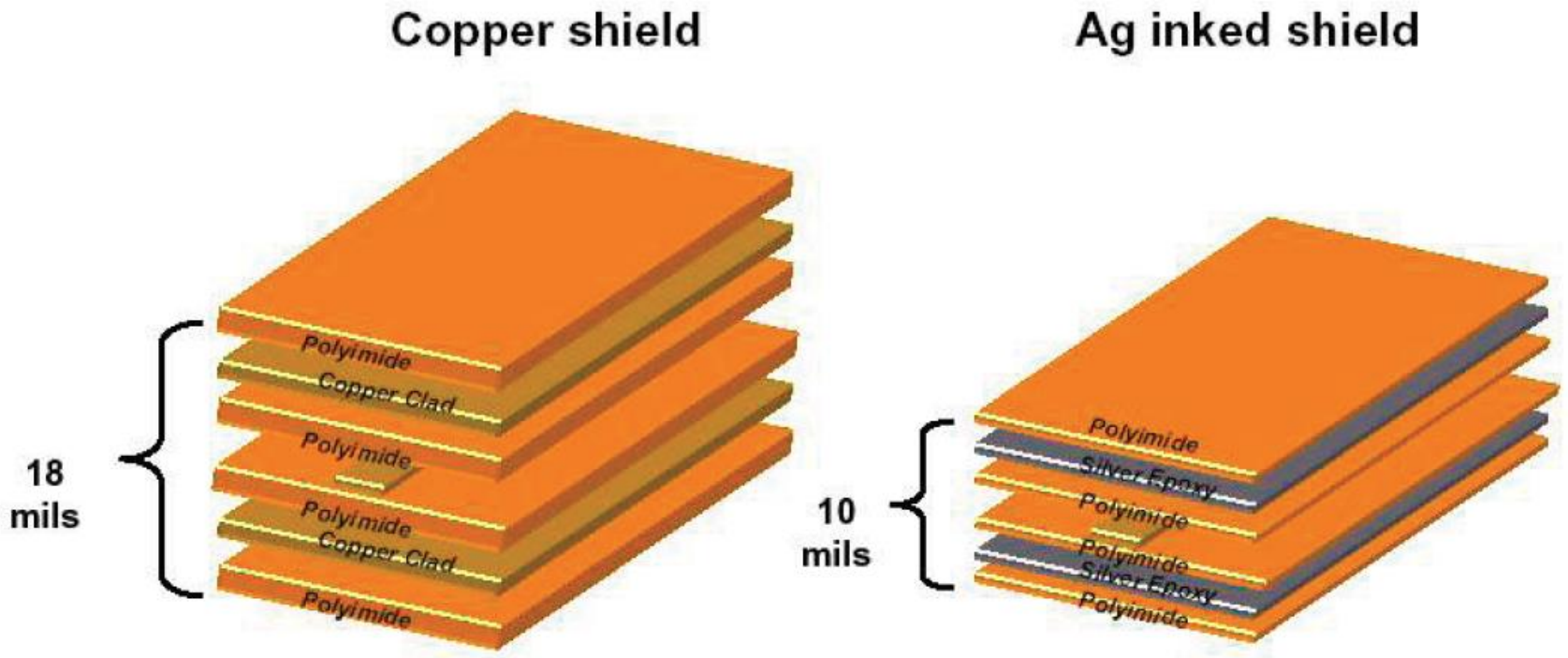
Copper vs. Silver inc. shilding



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Silver Ink Flex Design

- Lower cost

- May be used for economic shielding in EMI sensitive applications
  - May be used over two or three layer copper flex for additional shielding in Mil/Aero applications

- Single-Ended Applications
  - Use below 250 MHz

- Differential Applications
  - Use below 1 GHz (2 Gbps)

- Current carrying power and ground should be placed on copper layers

- Limited flexure cycles

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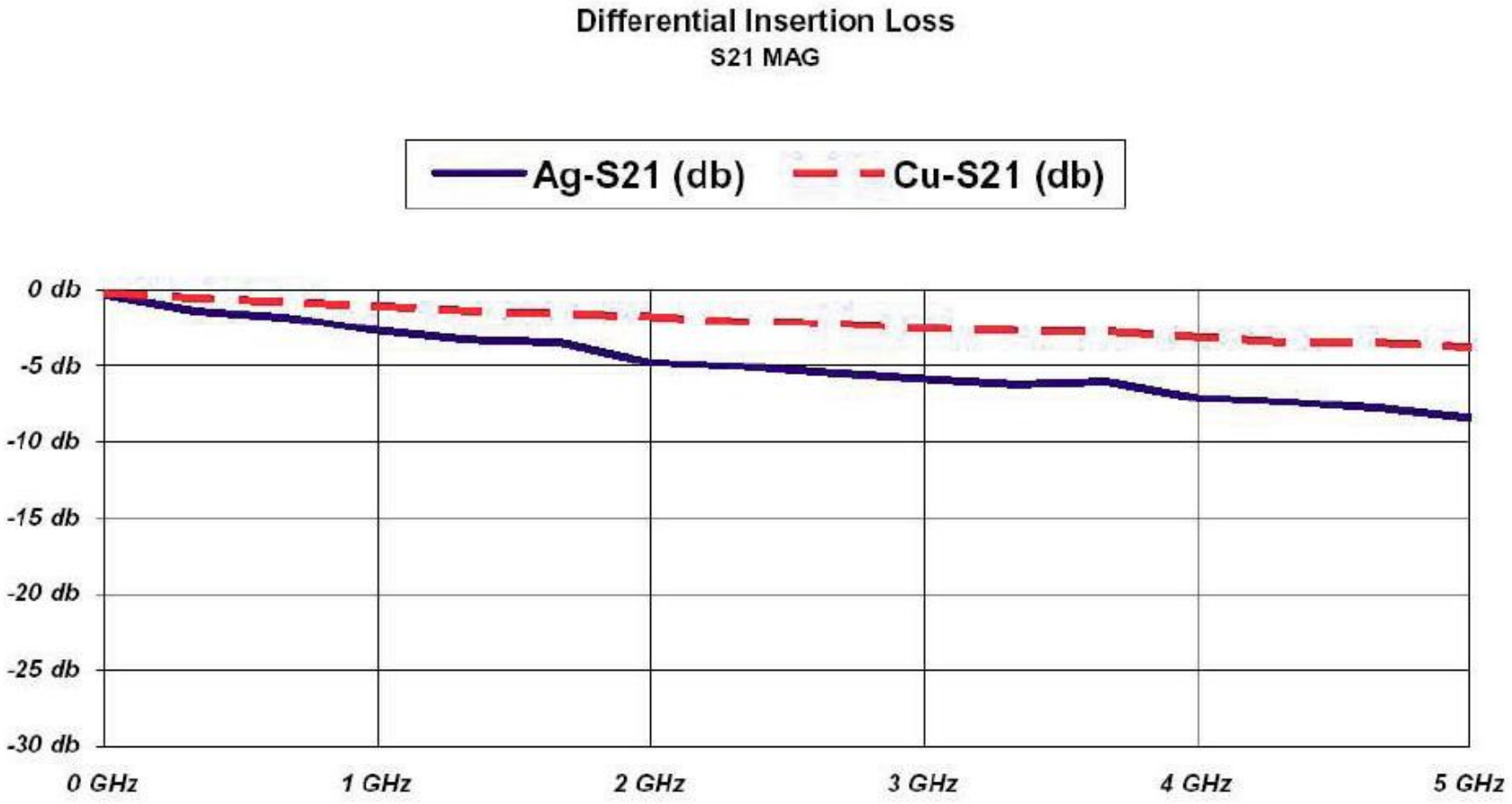
Insertion Loss ComparisonInsertion Comparison



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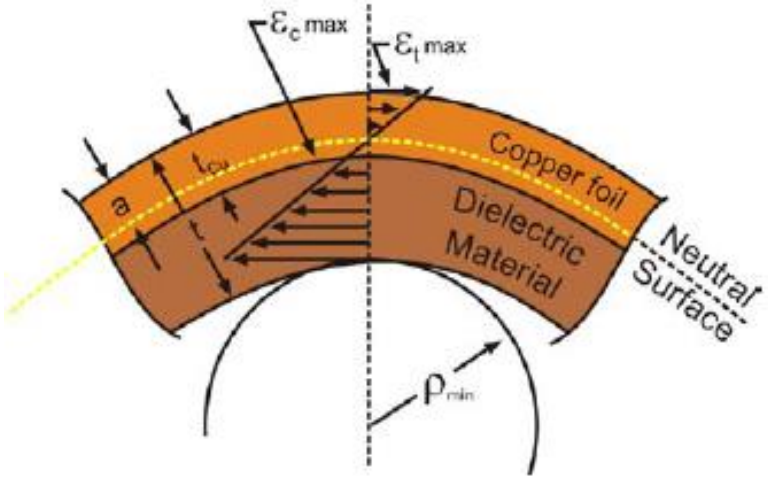
Bend Radius:

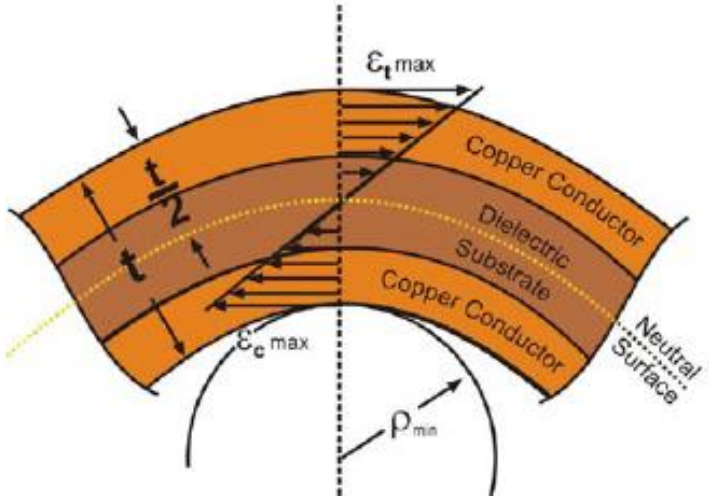
Single-layer: 06 × board thickness (minimum)
Double-layer: 12 × board thickness (minimum)
Multilayer: 20 × board thickness (minimum)

Circuit thickness is approximately 0.15mm per layer.
Sharper, permanent bends are common for bend and stay applications

Strain vs. Ductility:

The bending of flex boards causes deformation, strain, and stresses in the circuit materials. The strains and stresses are functionally related for each material via the stress-strain diagram. The forces necessary to cause flexural deformation are small; the flexural deformation is determined by the imposed bend geometry.





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Polyimide Films.

- This is the material used as the base layer for both the copper clad and the coverfilm.
  The most common thicknesses are: (**Red** is less common)
  0.0127mm - **0.025mm** - **0.050mm** - 0.075mm - 0.127mm

Adhesives

- Adhesives are used to bond the polyimide film to the copper layer or board layer it is exposed to.
  Some of the typical adhesive types are: Acrylic , Modified Acrylic , Phenolic Butyral ,
  Modified epoxy and PSA (*Pressure sensitive adhesives)* .
  The most common thicknesses are . 0.0127mm - **0.025mm** - **0.050mm**

- When it comes to temperature resistance, the adhesive is typically the performance-limiting element of a laminate, especially when polyimide is the base material.

- As with base films, adhesives come in different thicknesses. The thickness selection is typically a function of the application.

For example:
Different adhesive thicknesses are commonly used in the creation of coverlayers in order to meet the fill demands of different copper-foil thicknesses that may be encountered.

It is essential that you verify the chosen material availability from your manufacturer.

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LAMINATED COVERLAYERS

- Normally, a coverlayer is a two-layer material comprised of a base material and a suitable thermosetting adhesive. However, suitable homogenous thermoplastic films may also be used as coverlayers. The coverlayer serves to protect the conductors of the finished flex board and help enhance flexibility.

PHOTOIMAGEABLE COVERLAYERS

- Another type of coverlayer for use in flex manufacture is a photoimageable coverlay. This product is akin to dry film solder mask. It requires vacuum lamination to assure a good seal around the board traces.
  Just like a photoimageable solder mask, the material is exposed and developed to provide access to board component attachment features.

COVERCOATS

- The term covercoat is used to describe a range of thin coatings applied to the surface of conductors in lieu of a coverlayer. Although some suppliers of covercoat material have some impressive flex cycling data, covercoats are normally reserved for applications where no (or minimal) dynamic flexure is required.

  In manufacturing, covercoats normally are applied as a liquid by screen-printing and then either cured by heat or by exposure to UV radiation.

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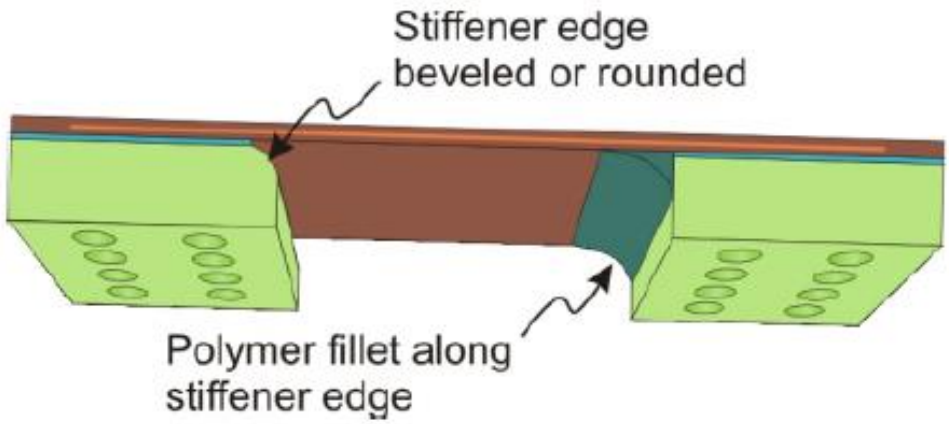
FILLET TRANSITION EDGE OF STIFFENER

- Filleting of the transition edge of a stiffener with a resilient adhesive or epoxy is another common method of strain relieving boards. The small bead of a suitable polymer will provide a simple means of transitioning strain from the stiffener to the flex board.



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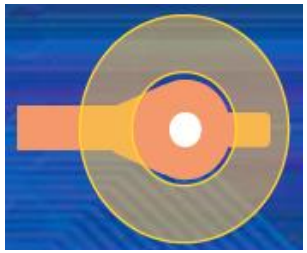
-Basic Glossary of Terms (see IPC-T50-D for complete list)

Adhesive

-Acrylic*, flame retardant, epoxy, epoxy prepreg, polyimide prepreg, phenolic
(* *most common materials used for manufacturing flex circuitsfor max flexibility*.)

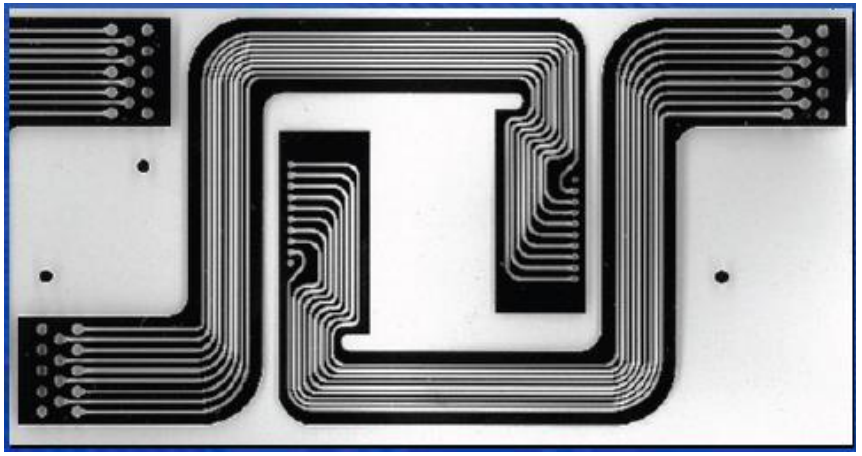


Annular Ring

- This is the exposed copper ring surrounding a through hole.

Artwork

- This is the tool used to define circuit features. Typically CAD generated.



Back Bared Pads

- This is a flex that is typically single sided in construction but has the copper accessed from both sides.

Back Side Access

- This is a flex that is typically single sided in construction but has the copper accessed from both sides.

Conductor / Track

- The metallic path that carries electrical current.

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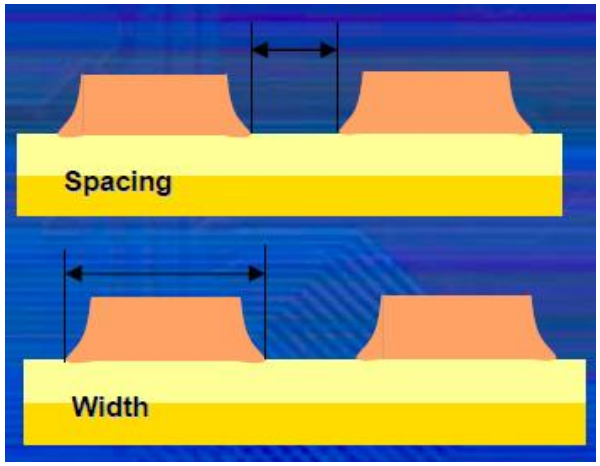

Track / Conductor Spacing

- This is the distance between tracks measured at the foot (widest point) of the track.

Track Conductor Width

- This is the width of the track measured across the base of the track.

Coverfilm

- This is the insulating material, usually in a film format, that is laminated to the flex board to define solderable areas. Can be drilled, laser cut or chemically removed to create complex geometries.

Dynamic

- This is the term used to describe the intended use of the flex. Repeated flexing, as in a disk drive, requires a dynamic flex circuit.

ED, Electro Deposited

-This is the means by which copper is deposited on polyimide to create an adhesiveless clad.

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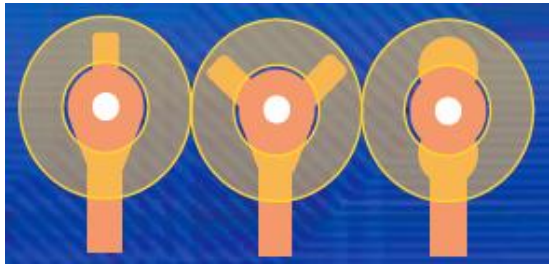
Hard Tooling

- A term used to describe tooling used to fabricate flex boards typically when tight tolerances and or high volumes are required.

HASL

-This is the acronym for a soldering process. Hot Air Solder Level. (Often not ideal to use on flex boards)

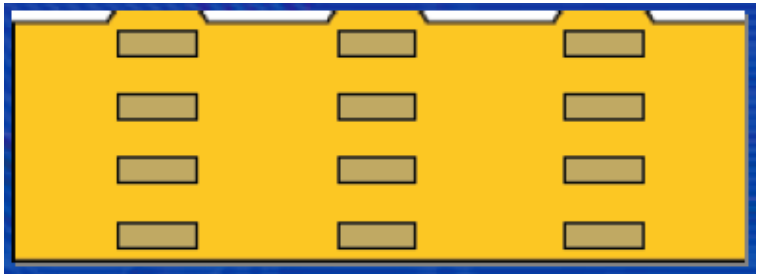


Hold Down Tabs

-These are extensions of the copper pad and are used to help anchor the pad during soldering processes both in assembly and rework.

I-Beam Effect

-This is the result of stacking your conductors during your design. Subsequent flexing induces stress and compression, causing cracking to occur.



Impedance

- Basically this is the total effective resistance to AC current. It can be altered by changing conductor spacing, signal spacing relative to ground, material thicknesses.

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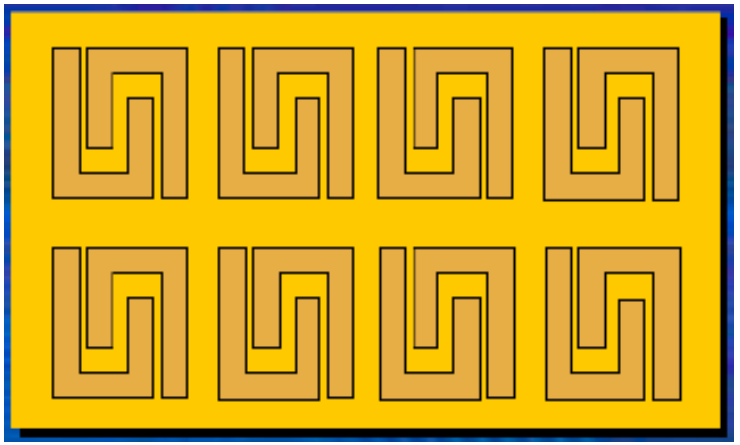
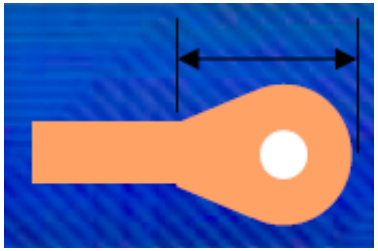


Nested Panel

- This is the process by which the individual board is maximized on a panel.



Pad

- The end of a conductor usually configured to accept a component or to be attached to a device.

PIC, Photoimagable Coverfilm

- This is another means of defining your solderable areas. This material is apply in a clean room environment, exposed with an artwork and then developed. This allows for complex geometries not available from routing or other soft tooling means.'

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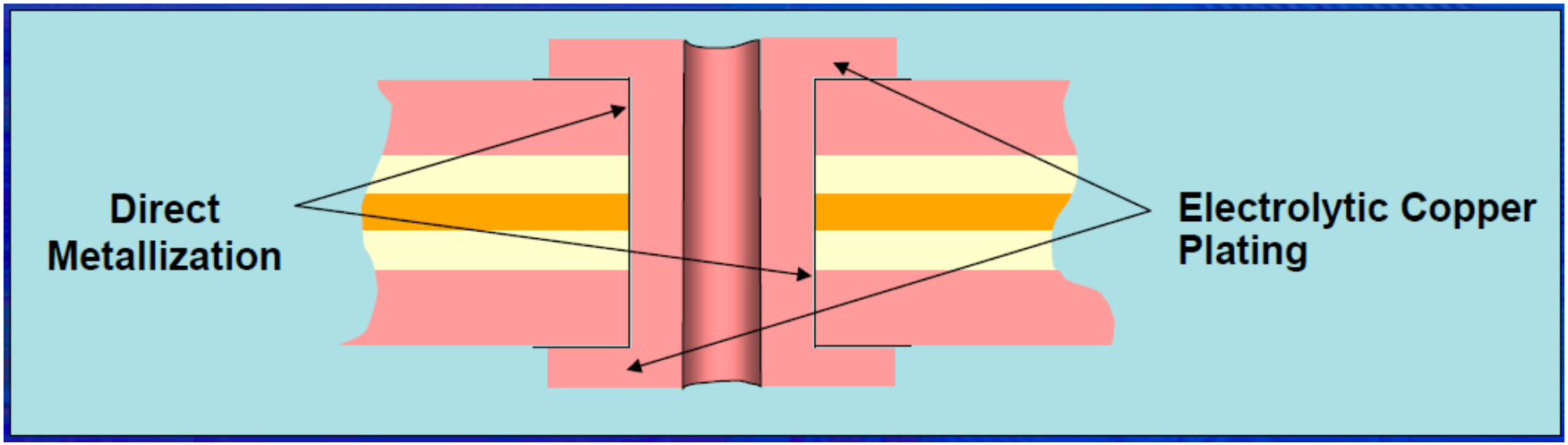
Pads only Plate (button plate)

-This is the process by which only the via and a small portion of the surrounding pad is plated in a double sided or multilayer flex.
This limits the amount of plating a panel will see and allows the double sided flex board to still be somewhat flexible.



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PSA (Pressure Sensitive Adhesive)

- An adhesive used to bond stiffeners to specific regions of the flex circuit.

RA (Rolled Annealed)

- This is a term used to describe the type of copper and it is actually the method by which the copper is flattened.

Through Hole/Vias

- A plated hole in the panel that can be accessed through the coverfilm or can be tented over with the coverfilm. There are numerous versions of these.

Blind Via

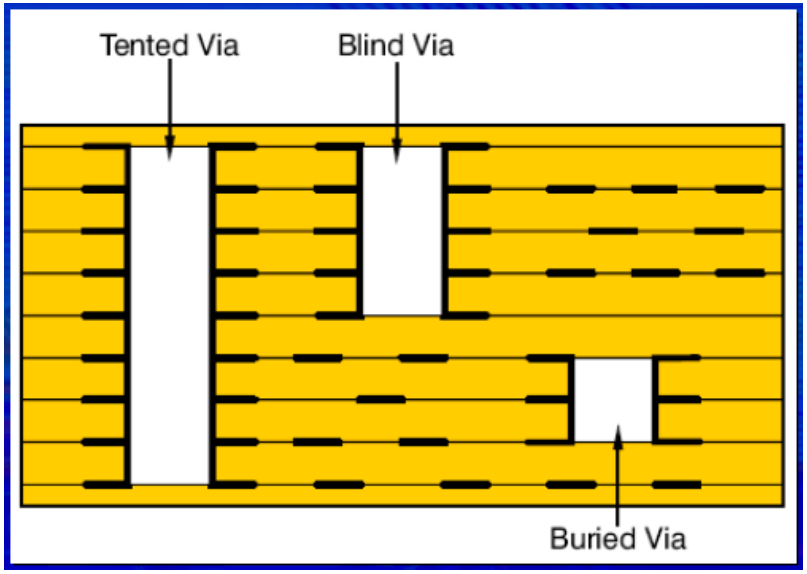
- Typically a via that penetrates to several layers below but is covered up by the coverfilm

Buried Via

- A via that is set deep inside a multilayer with no access to the coverfilm

Tented Via

- A via that goes completely though the flex, but is covered by the coverfilm on both end limiting access.



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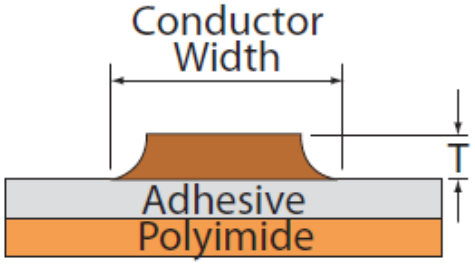
Panel size (is manufacturer dependent
- Single sided through multilayer construction, 12” x 18”

Drilled holes size
- Plated or non-plated 0.25mm diameter
- Tolerance of hole to hole is ± 0.1mm

Aspect ratio (ratio of hole depth/hole diameter)
- 10:1 maximum.



Track width /space
- Using ½ ounce (17um) thick copper, 0.1mm track/space
- Using 1 ounce (35um) thick copper, 0.15mm track/space

Conductor aspect ratio
- For best producibility, design traces to be at least four times as wide as they are thick.
  In tight situations it can be successful to achieve 2.5-3 : 1 ratio conductor widths.

Layer count
- 1 –10 layers
- Solid or cross hatched ground layers

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Stiffener

- Epoxy-glass (FR-4), polyimide-glass, polyimide, copper, aluminum.

Surface finishes

- ENIG
- Chemical Tin
- Chemical Silcer
- Hard Gold over Nickel
- HASL / LF-HASL ****
- OSP

Outline tolerances:

- SRD	0.38mm
- Laser / Hard tool	0.10mm
- CMD (chemical Milled die)	0.25mm

Shield layers

- Solid or grid patterned - copper foil or screened conductive ink.

**** Do not use it……..due to ”blowing in the wind” and extreme process temperature.

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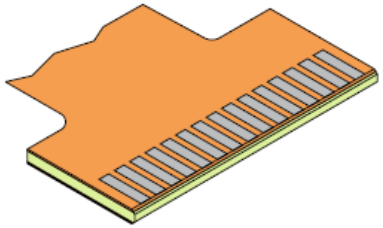
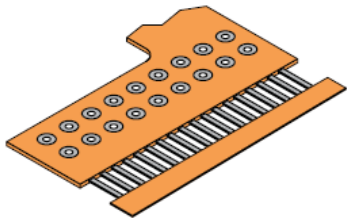
Fingers

- Supported: 0.20mm minimum, center-to-center;
- Unsupported: 0.50mm minimum, center-to-center.



Supported fingers



Unsupported fingers

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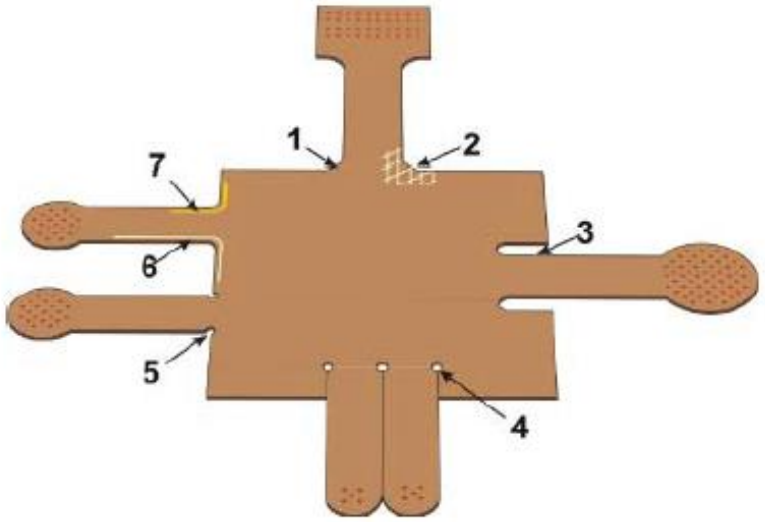
TEAR-RESISTANCE FEATURES IN FLEX DESIGN

- All flex board designs should be made as tear-resistant as possible. While the material may not be intrinsically tear-resistant, tear-resistance can be improved by employing certain features in the design.
There are several possible methods, described and illustrated below. All of the following techniques have been successfully used to help prevent tearing.
One or more of the following techniques can be used:

1) Radius All Internal Corners

The first line of defense against tearing is to make certain that all internal corners are provided with as generous a radius as possible. This design practice is the most important and simplest of all methods used to prevent tearing of the fle



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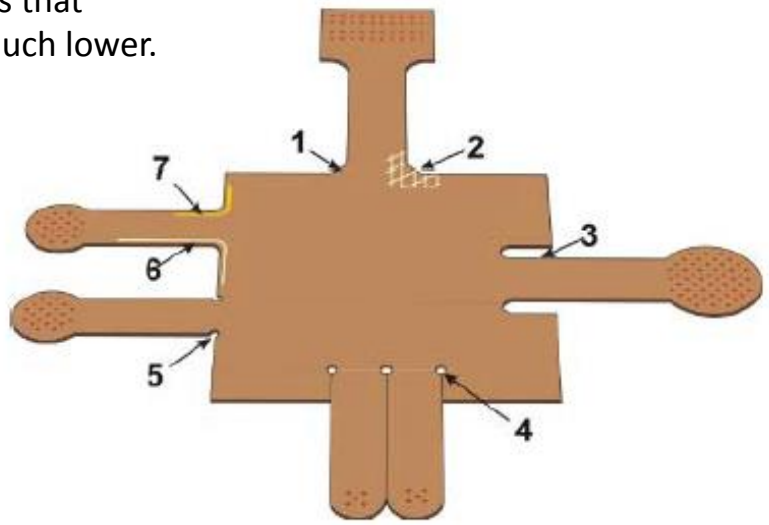
2) Laminate Glass Fabric in Corners

Glass cloths can be laminated into corners during the fabrication process. Though not flexible, this method has been shown to provide a very robust corner construction and has been favored in the past by military product designers. It is an expensive solution, however, because of the type of preparation required and should be used only after careful consideration of the alternatives.

Use Fluoropolymer Coverlayer

The use of fluoroplastics such as Teflon® as coverlayers helps to improve tear resistance by virtue of the high tear resistance of the polymer itself. This is due to the fact that fluoropolymer tends to stretch rather than tear, adding toughness to the substrate.

An additional benefit of using fluoropolymer coverlayers for those involved in high frequency design is that the dielectric constant of the coverlayer is much lower.



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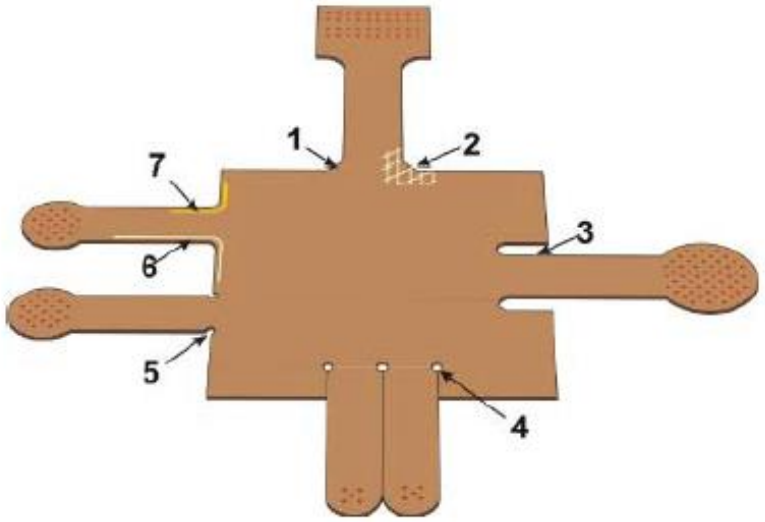
3) Use of Radiused Slots

The use of slots with ends that have a radius to access relieved board features also can serve to provide tear resistance. Normally, such features can easily be provided for during the punching operation or other board fabrication process.

4,5) Drilled Holes at Corners or Ends of Slits

Drilled or punched holes in corners or at the ends of access slits have been used with success when flexible appendages must be spaced close together.

This method allows the greatest use of material, but the hole size chosen will impact tear resistance. If the hole is very small, the overall robustness will be reduced.



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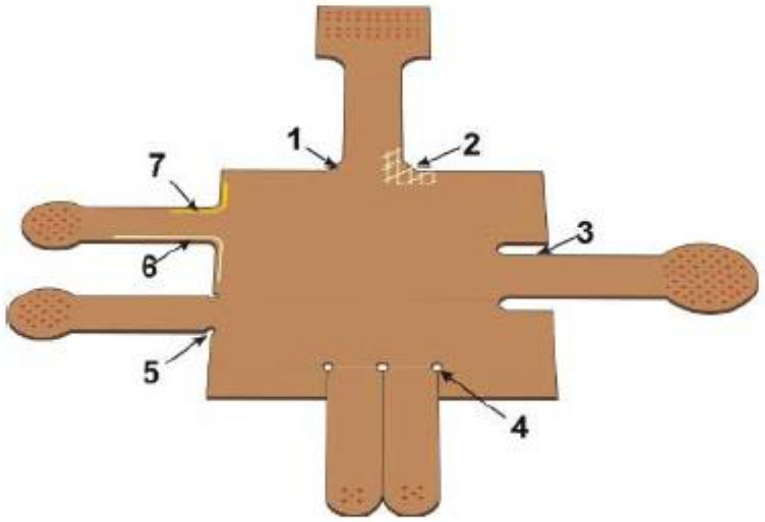
6) Aramid Fibers Inside Cut Line

As an alternative to glass cloth, the use of aramid fibers routed through corners or along the entire outline of the flex board is a unique method to stop tearing. The thin polymer fibers have very high strength and are very pliable, minimally affecting flexibility. However, this is a labor intensive method and should only be specified with the knowledge of cost impact.

7) Leave Metal in Corners

The board design should, if possible, have small areas of copper provided for at internal corners to serve as tear stops at the inside of corner radius. This serves to prevent further or imminent propagation of a tear through the polymer, should a tear in the material start.



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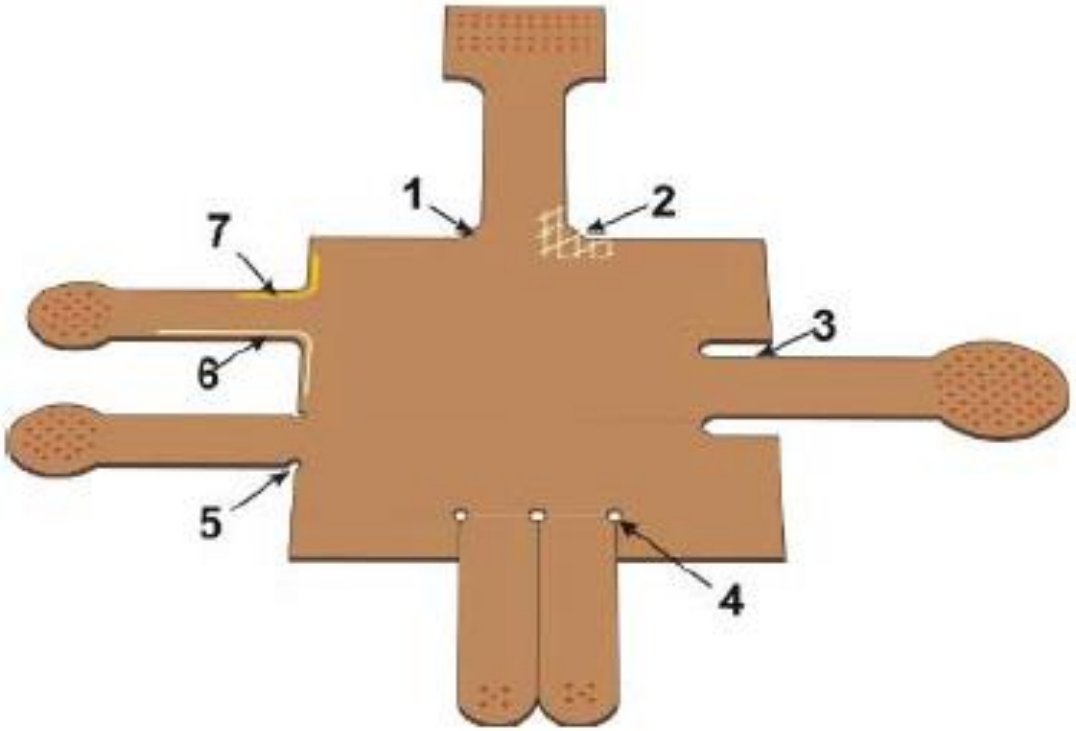

(1) Large radius in corner

(2) Embedded glass cloth

(3) Radiused slot

(4) Hole in slit

(5) Drilled hole at corner

(6) Embedded aramid fiber

(7) Extra copper in corner

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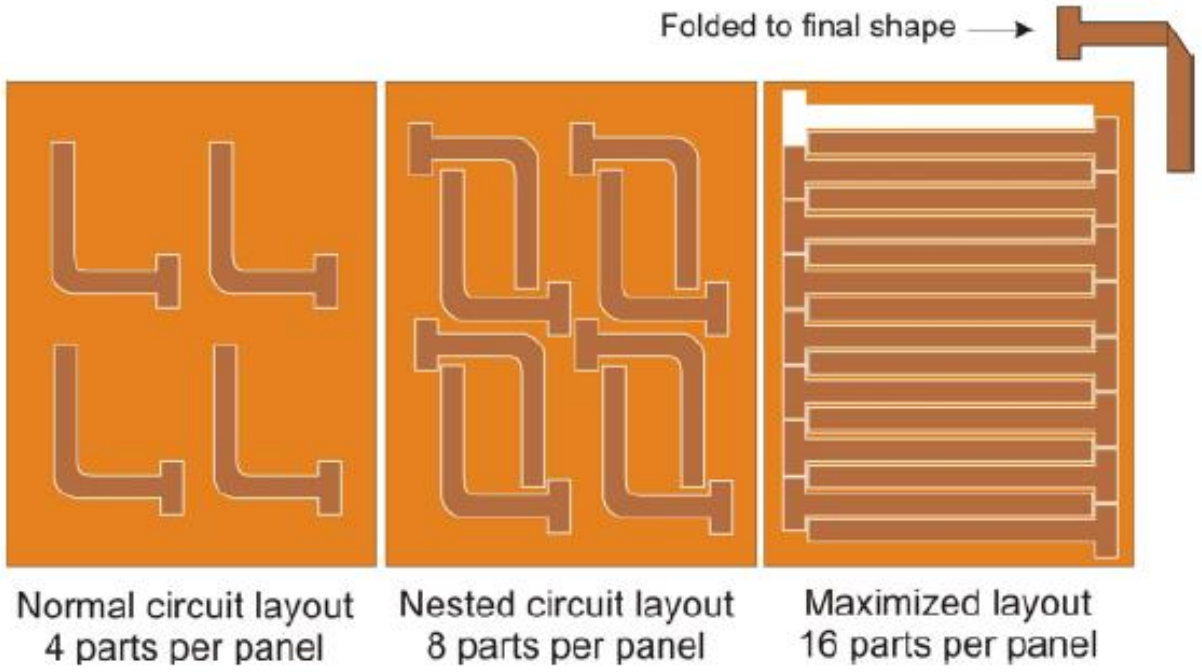

Proper circuit nesting can greatly improve panel yield and lower overall cost.
If folding can be tolerated as an assembly operation, yield can be maximized.

For dynamic flex board designs, the grain direction requirement may impact layout.

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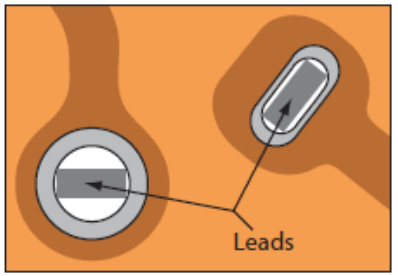
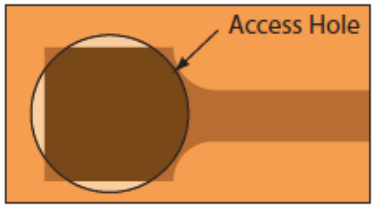
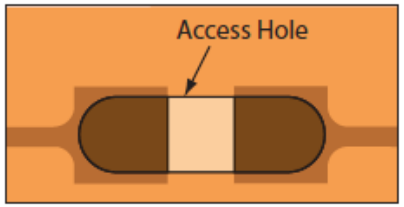
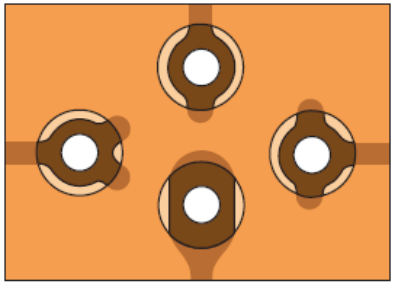
It is best to specify round (instead of slotted), through-holes. This will reduce drillingtime and cost.







Whenever possible, design pads larger than the access holes. If space is critial, use hold-down tabs. Hold-down tabs are especially important for single layer boards, because a single layer board does not have the added strength of plated through-holes. A variety of hold-down tab designs are available.



Pad fIllets improve etched yield and material strength. Fillets are appropriate when the pad diameter is greater than the connecting strand width. Acute angles at the interface between traces and pads are to be avoided by using fillets to minimize the concentration of stress at the interface.

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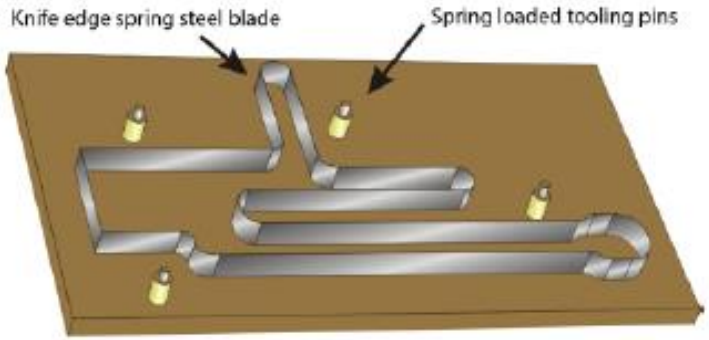
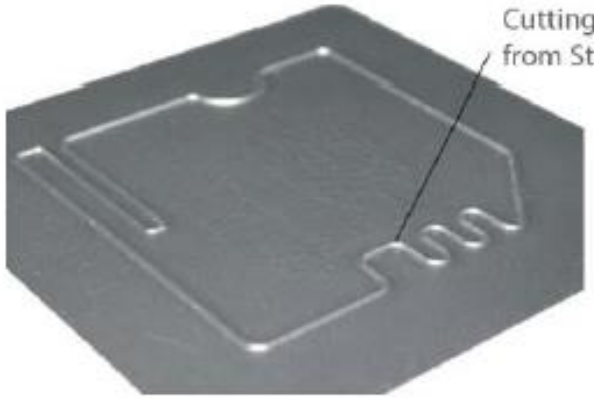


The steel rule die is a cost-effective tool for punching flex boards from their panel.

Class-A tooling for flex circuit punching offers both high precision and long tool life.

Class A two part Male/Female die punch set



Example of an etched punch die tool

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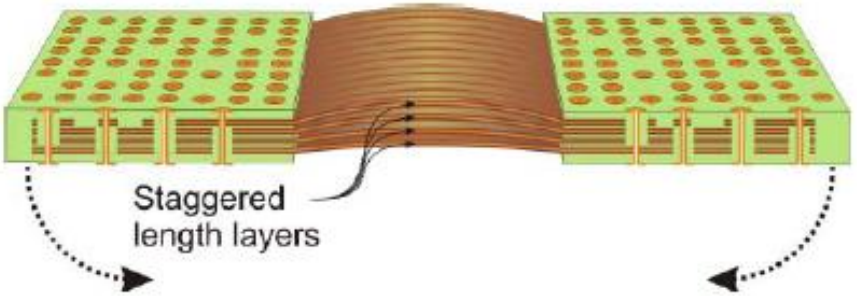
STAGGERED LENGTH BOARDS (BOOKBINDER CONSTRUCTION)

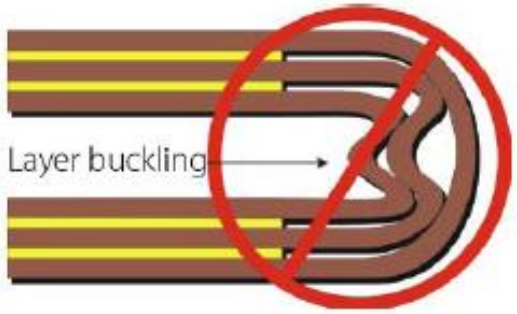


For ease of flexing multilayer and rigid flex designs, the use of staggered length design is commonly employed.

The technique is accomplished by adding slightly to the length of each succeeding flex layer, moving away from the bend radius.

A common rule of thumb is to add length equal to roughly 1.5 times the individual layer thickness.

Staggered length designs facilitate bending of the flex board. The circuit can only be bent in one direction by design.



Without staggered lengths, layer buckling occurs.

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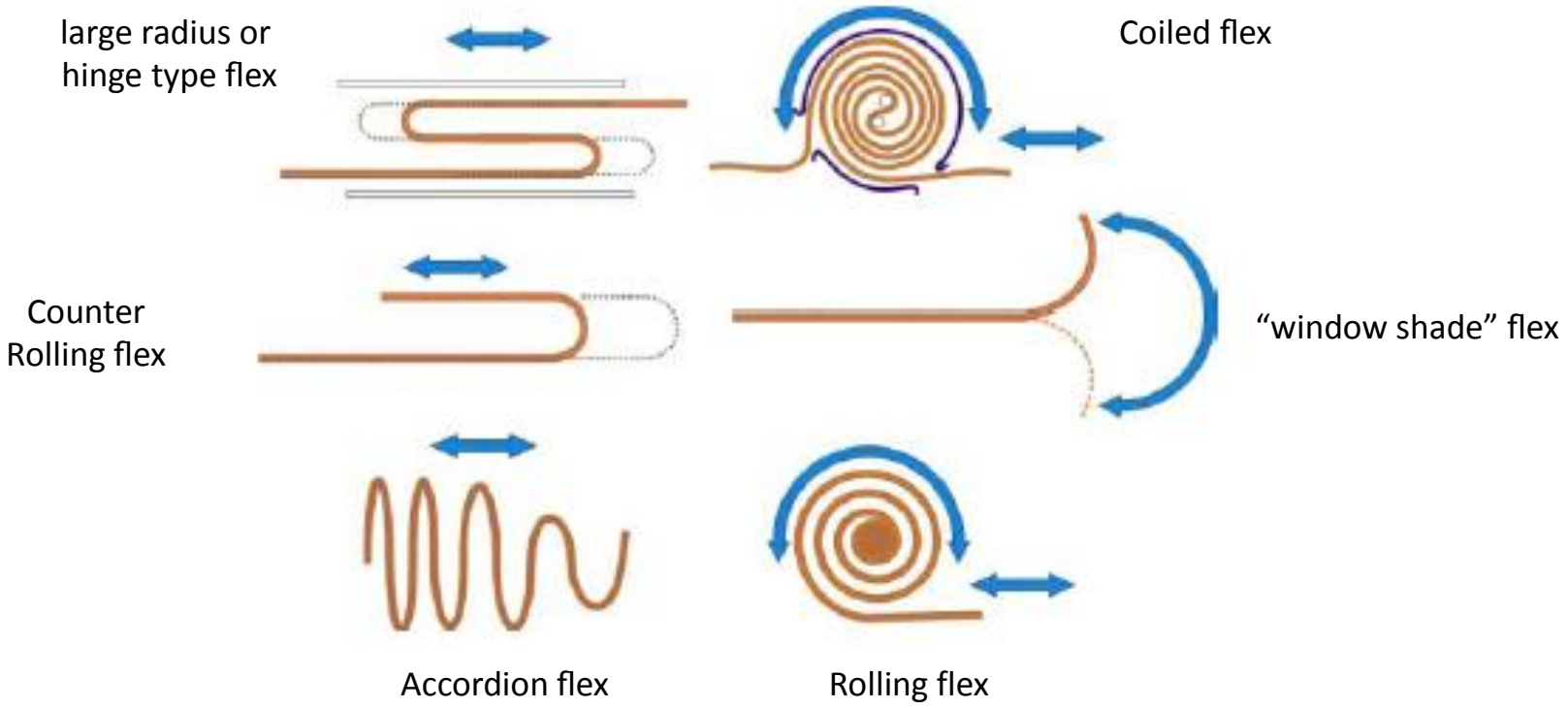
- Design issues ….cont'd

Various flexing and bending methods



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Example materials for various requirements

Flexible applications

Name	Reinforce-ment	Resin	Comment	Examples	Cost factor (reference: FR4 standard) ***
Polyimide with acrylic adhesive	---	---	For dynamic flexible applica-tions, adhesive has a very large CTE(z)	Pyralux® LF/FR se-ries**; DuPont	5
Polyimide with epoxy adhesive	---	---	For semi-dynamic and static flexible applications	Teclam® series*; DuPont Akaflex® series*; Krempel	3
Adhesive free polyimide	---	---	For dynamic flexible applica-tions, good thermal perform-ance	Espanex series*; Nippon Steel AP se-ries®**; DuPont	5-6
LCP (Liquid Crystal Poly-mer)	---	---	For dynamic, flexible applica-tions, very good thermal per-formance, low water absorp-tion, also suited for HF applica-tions in the high GHz range	R/flex®3600, R/flex®3850; Rogers	8-10

There is no universal base material for printed circuit boards. Whether for standard applications, HF, high temperature or other applications: A large number of substrate types is available.
For further technological questions concerning circuit boards, please contact your Elmatica team.

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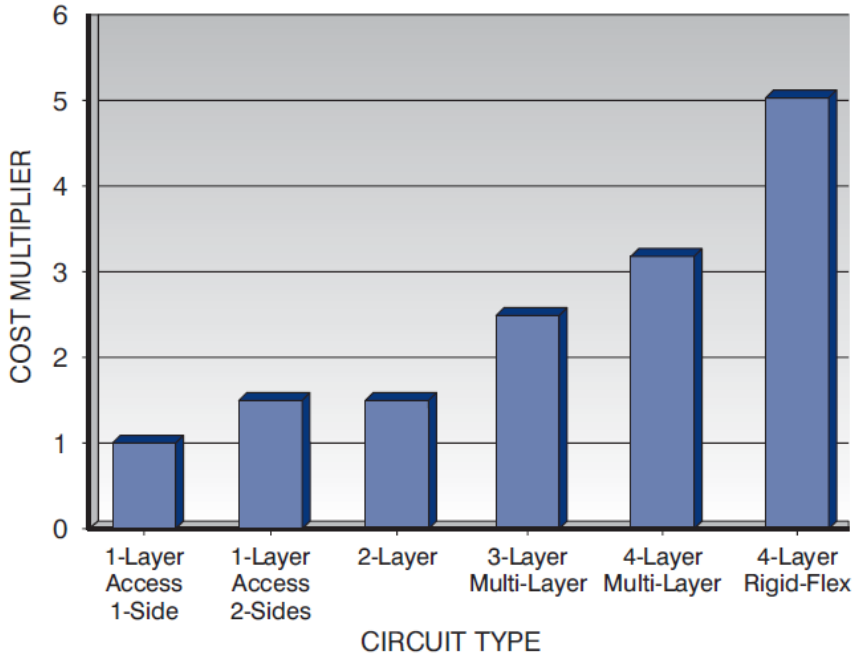
The information for the chart are taken from a sample of circuits built with standard materials.

This chart is not intended to be used as a price guide. However, it does showthat circuit cost generally rises with layer count.
It is in your best interest to consider all options to minimize cost.



For example, use two circuits to do the job of one.
Two double-layer circuits may be less expensive than one four-layer circuit.
But the cost savings of the circuit may be offset by additional assembly requirements.

Circuits can also be folded in order to save space and layers.

Each situation is unique.
A rela-tively small amount of time invested in project assessment canresult in significant savings overall.’

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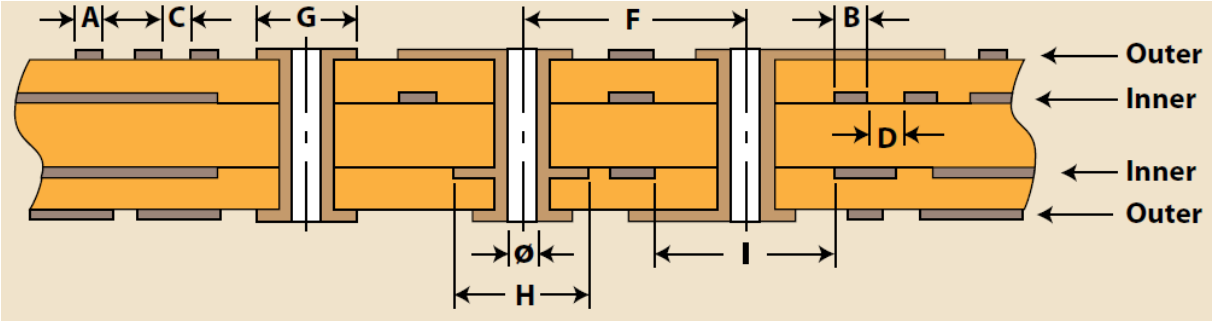
General FLEX PCB Design Guidelines

Dec-2011josse

Attribute	Detail	Minimum	Nominal Preferred
Track Width – Outer Layers	A	0.100mm	0.127+ mm
Track Width – Inner Layers	B	0.075mm	0.100+ mm
Track to Track Space – Outer Layers	C	0.085mm	0.100+ mm
Track to Track Space – Inner Layers	D	0.075mm	0.100+ mm
PTH Diameter – Drilled	Ø	0.150mm	0.200+ mm
PTH to PTH Pitch – Center to Center	F	Ø+ 0.200mm	Ø+ 0.250mm
PTH Pad Diameter – Outer Layer	G	Ø+ 0.300mm	Ø+ 0.400mm
PTH Internal Land Dia. – Inner Layers	H	Ø+ 0.300mm	Ø+ 0.400mm
PTH Clearance Dia. – Inner Layers	I	Ø+ 0.350mm	Ø+ 0.400mm

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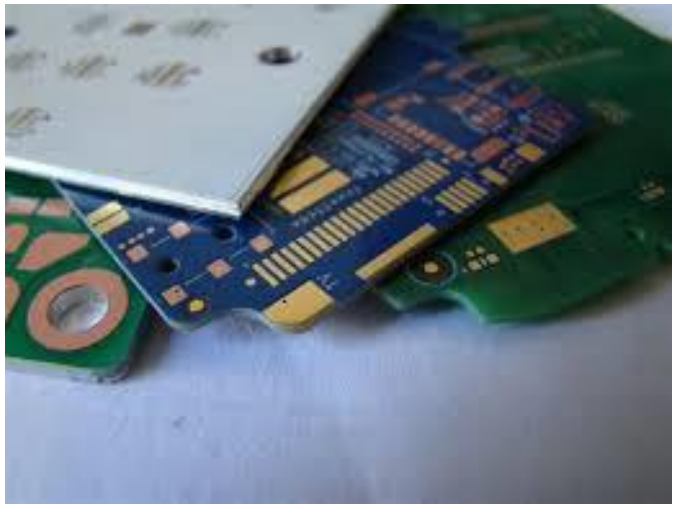

Introduction to MB PCB Metal Back PCB's. Aluminium for Power and LED applications.

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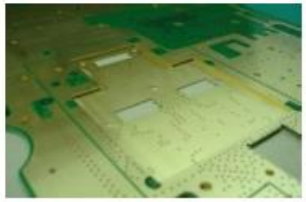
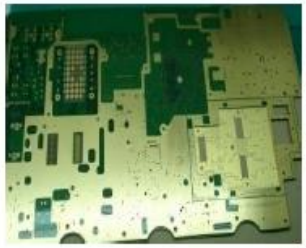
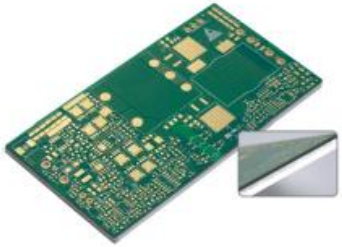
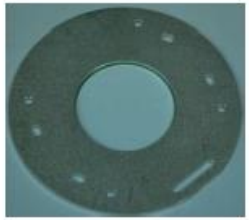
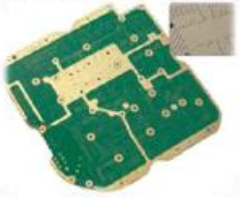
Metal Back Technologies

	Single side	Multi-layer	Double side	Partial Hybrid	Aluminum
Sweat -solder					
Post-bonding					
Pre-bonding					
Coin Inside					

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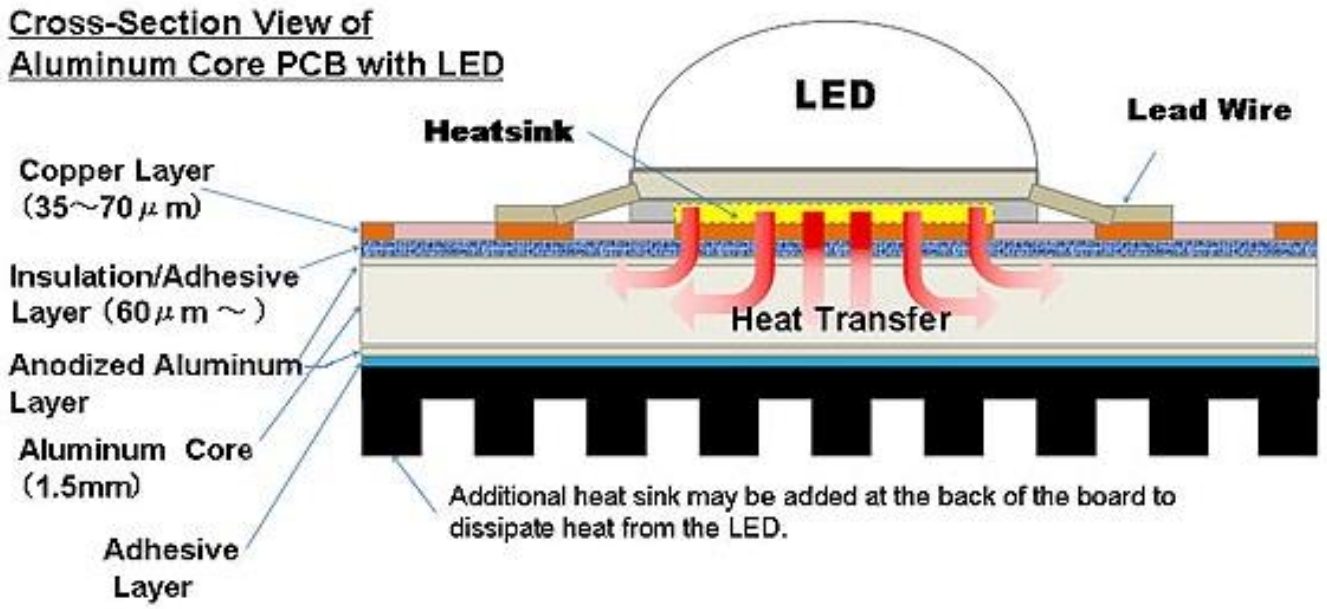
Aluminum Core PCB for LED application



Aluminum is superior in heat conduction, corrosion resistance, lightweight and cost.

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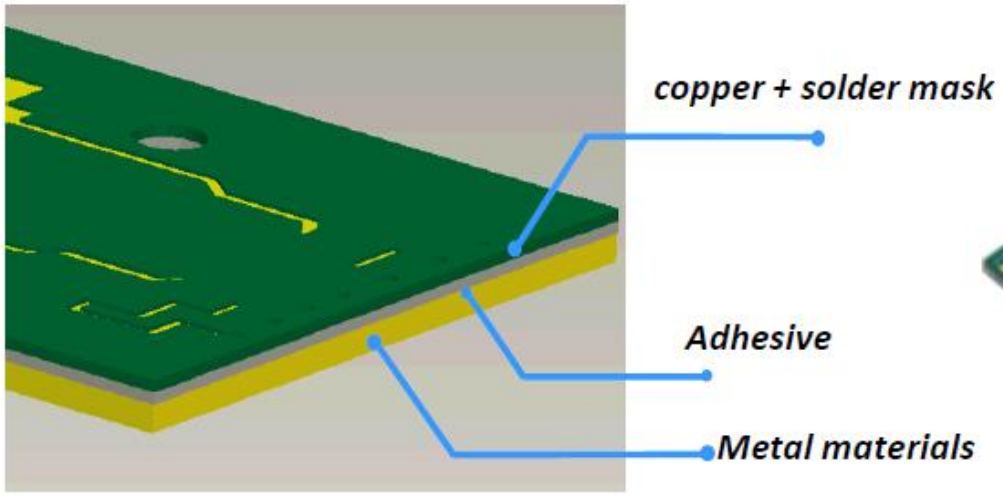
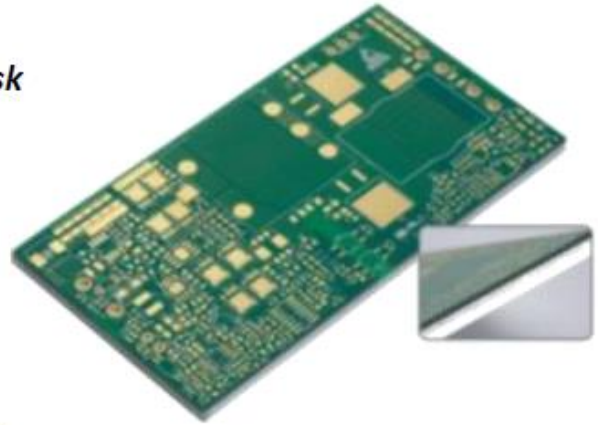
Metal Back Technologies Types





Pre-bonding Structure:

1. Cu + Solder Mask
2. Adhesive（PTFE、Thermal resin）
3. Metal (Aluminum or Copper)

Pre-bonding is only used for single side PCB .Metal base can choose aluminum or copper.

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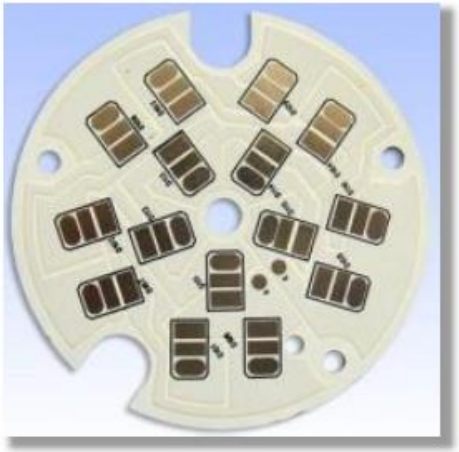
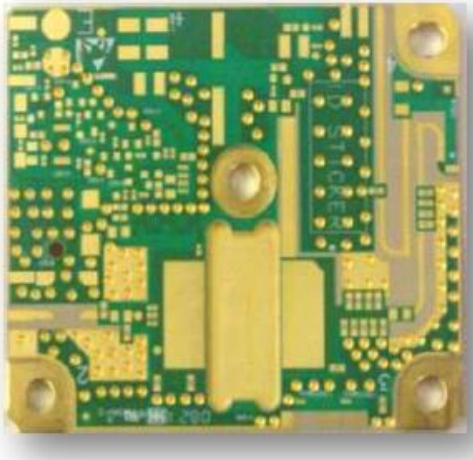
Metal Back Adhesive



Adhesive: Thermal resin

Supplier	Type	Tg	Thermal constant
Polystar	TCB	130℃	2.0/2.7 w/m.k
Laird	LLD/T-Lam	165℃	2.0/2.7 w/m.k
Bergquist	Thermal Clad	90℃	1.3 w/m.k
Totking	QB-AL	130℃	1.5/2.5/4 w/m.k



Adhesive: PTFE material

Supplier	ROGERS
	TACONIC
	ARLON

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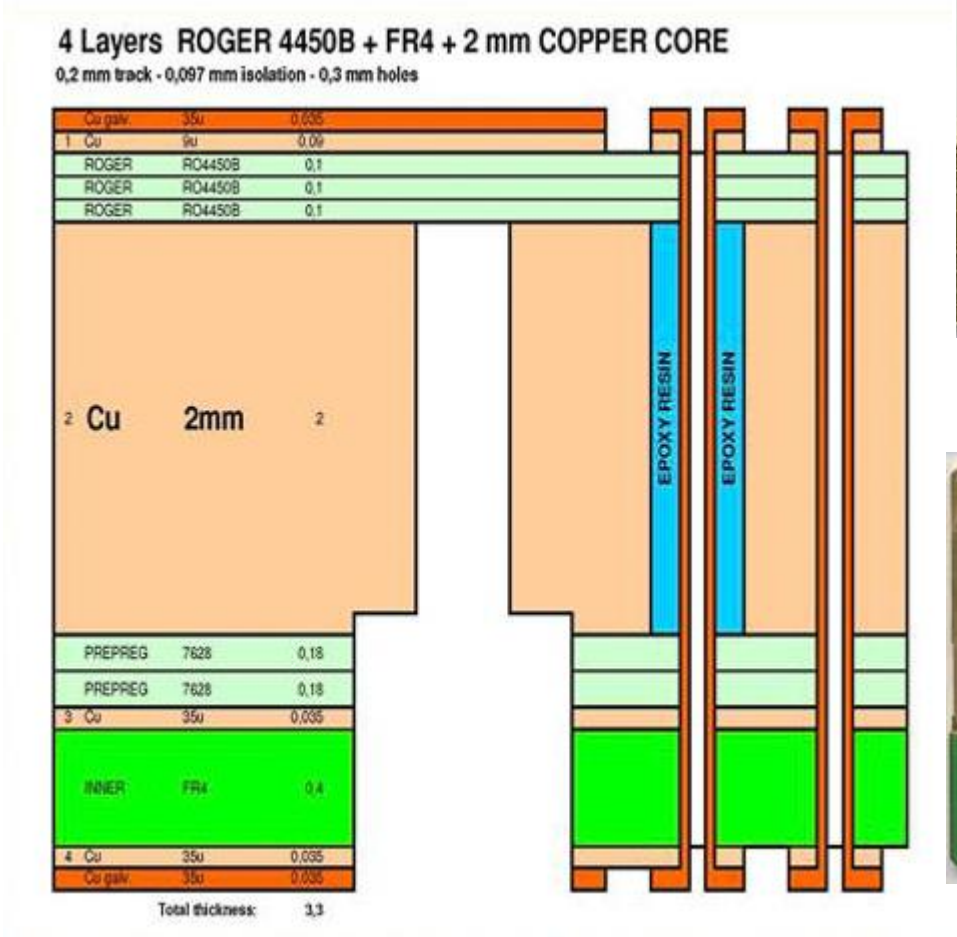
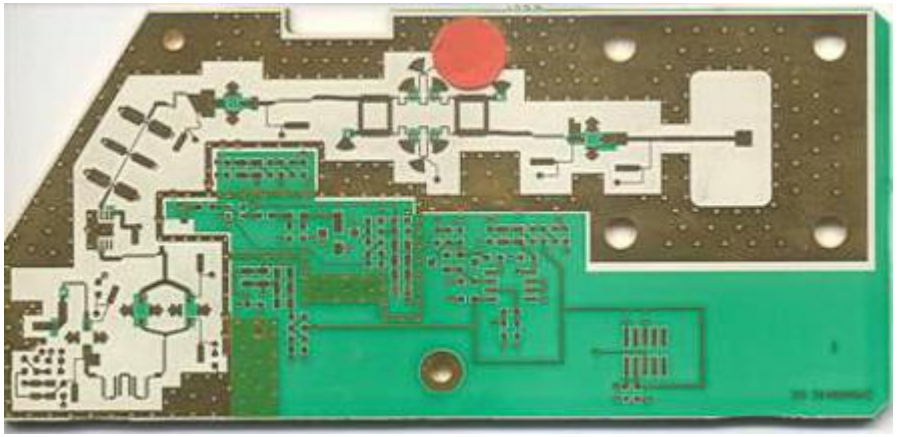
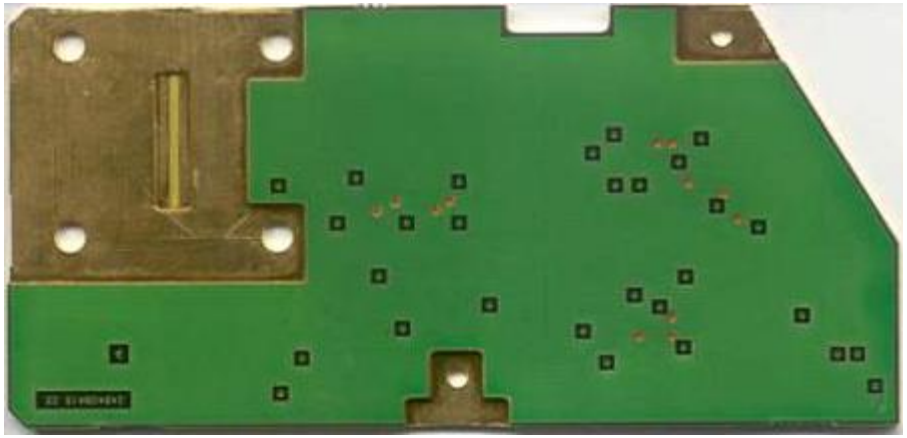
Metal Core







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