UiO : Department of Physics
University of Oslo

FYS4260 2018

Microsystems, electronic packaging and interconnection technologies

Lecture 6 – Finalizing your design, checks and verifications.

UiO : Department of Physics
University of Oslo

Checklist for final delivery

1. Verify mechanical layout.
   - Connector placement, testpoints, mounting holes.
   - 3D modelling? (optional, limited nr of licenses)
2. Verifiy your decoupling capacitor placements.
3. Verifiy schematic and pcb design integrity.
4. Visual inspection of each layer.
5. Check all design rules and routing completion.
   - In CadSTAR and/or optionally in PREditor
6. Cleanup silkscreen and other notations.
   - Add own text; Name, project, etc

See the following slides for detailed instructions.

UiO : Department of Physics
University of Oslo

Verify mechanical layout

- First, verify your layout with respect to the mechanical and user constraints you have desided on. That can be for for example:
  - Connector placement
  - Placement of LEDs and/or display.
  - Mounting holes (optional)
  - Adjust the board size, rounding corners or similar.
  - Etc…
- Have you included testpoints, at least your design must have one ground testpin.

UiO : Department of Physics
University of Oslo

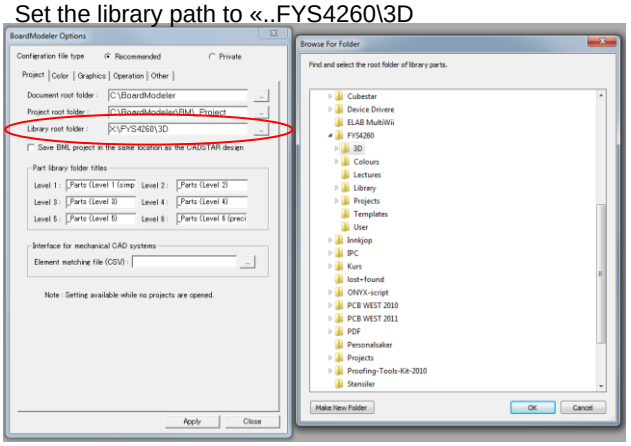
3D modelling

- CadSTAR can create a 3D modell of your design using BoardModeler from the tools menu.
- To set-up Board Modeler start Board Modeler from Windows Start menu
- Then select Tools -> Options

UiO : Department of Physics
University of Oslo

Boardmodeller Set-up

- Set the library path to «..FYS4260\3D

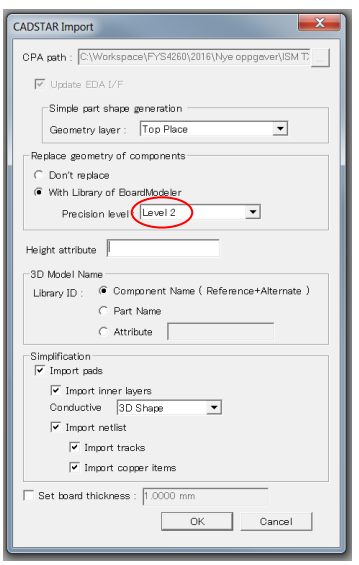


- Close Boardmodeller

UiO : Department of Physics
University of Oslo

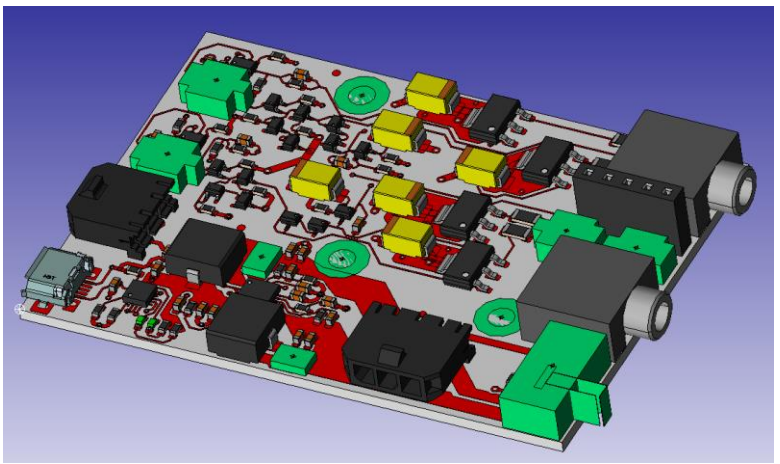
3D Model

- Start BoardModeler from the Tools tab in CadSTAR
- Select Yes/OK on all questions.
- The last dialog as shown ->
  - Geometry layer: Top Place or Top 3D
  - Precision level: 2



UiO : Department of Physics
University of Oslo

- This will give you something like this
  - We are missing some models, these parts will be shown as green boxes indicating their outer boundaries and height.

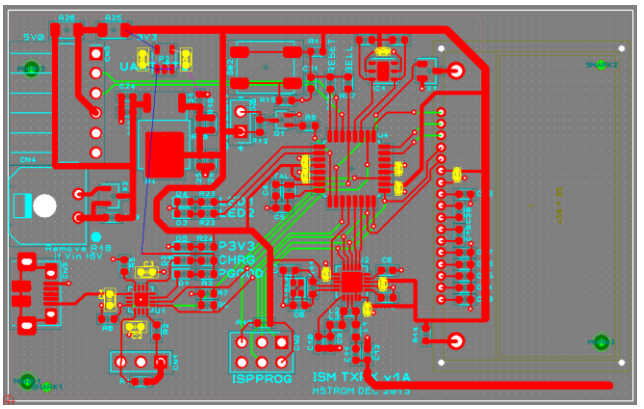


UiO : Department of Physics
University of Oslo

Verify decoupling capacitors

- All decoupling capacitors should be placed, to the best of whats possible, close to each power pin in the design.

Highlight all decoupling capacitors to get an easy view for verification. If you have named your decoupling capacitors CBx you select them by writing CB* <enter>.



UiO : Department of Physics
University of Oslo

Verify schematics and pcb integrity

- Make sure you have 100% match between your schematic and pcb designs.
- This can be done using a simple ECO update as we have used earlier.
- Or by running the «Design Comparison» report from the Report tab in CadSTAR.
  - Select the correct scm or pcb depending on which design you have open (you run the check between the active design and a scm or pcb file)
  - This will give you a report of any differences.

UiO : Department of Physics
University of Oslo

Visually inspect all layers

- Visually inspect all layers one by one.
  - In CadSTAR use the dropdown list on the view tab to select each layer.
  - Or in PREditor use CTRL+J/K to move between layers for inspection.
  - Recomend to do this in PREditor as it is easy to do simple changes right away.
- This is an easy way of cleaning up your design.

UiO : Department of Physics
University of Oslo

Design rule checking

- Design rules can be checked in both CadSTAR and PREditor.
- First, make sure you have the updated design rules.
  1. On the design tab, click Assignments and the Design Rules tab.
  2. On the right side there is a button labeled «Load DRC File».
  3. Load the «FYS4260 2017 DRC_vx.drc» file. You find this file in the FYS4260/DRC folder on FELT

     (same place as you have mapped your libraries, eg

     ..\FYS4260\DRC\FYS4260 2017 DRC_vx.drc

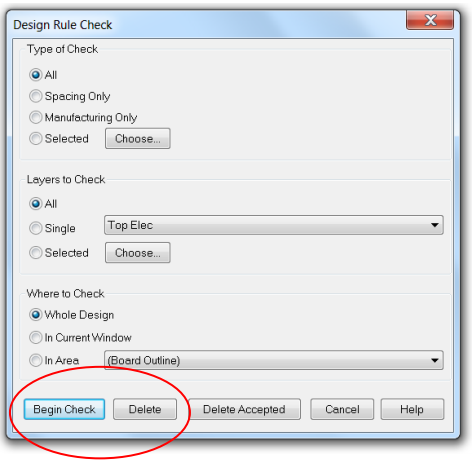
UiO : Department of Physics
University of Oslo

Check design rules in CadSTAR

To check for design rule errors in CadSTAR run Design Rules Check from the Report tab.

- Leave settings as shown
- Critical errors include all errors relating to spacing and widths for pads, tracks, vias and copper.
- Others can be non critical, for example
  - Route offset (RO)
  - Component placement (AA)

  These errors can be accepted if you are 100% sure they are ok.
- To delete errors use «delete» on the same menu.

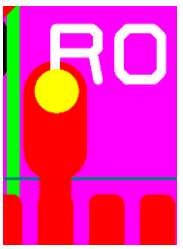


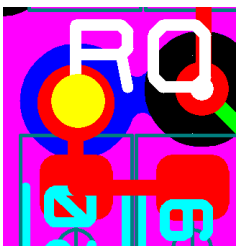
UiO : Department of Physics
University of Oslo

The Route offset error

- The RO (Route Offset) error indicates routes that are offset to another object, typically a via or other route segments.
- As long as the offsets are small this is not a problem and these errors can be neglected. Visually inspect all errors before accepting them.
- Typical causes are via grids set to 0.0254 when routing millimeter based components.
- Tips to avoid route offsets are to route in the other direction, change the via grid in Routing setup, and to use route widths that are thinner than the outer via diameter.

1mm wide route on a 0.7mm via, with a little offset. Routing the whole segment with a 0.6mm route will remove the error.





Here there is a larger route segment on top of a via, with a little offset. Remove the larger route segment to get rid of the error.

UiO : Department of Physics
University of Oslo

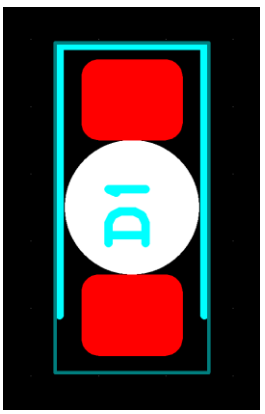
A special case – the reverse mount LED

- The reverse mount LED used for the touchbuttons in the FM Transmitter design will throw a Pad-to-Pad error.

The hole for this LED is in CadSTAR defined as a pad, and hence CadSTAR will throw two Pad-to-Pad (PP) errors on this component.

Since this hole is non-plated, it is fully manufacturable, and the error can be accepted.

Ideally, we would like to add some spacing between the hole and the pads, but to maintain solderability, this is the best compromize.



UiO : Department of Physics
University of Oslo

Verify 100% routing completion

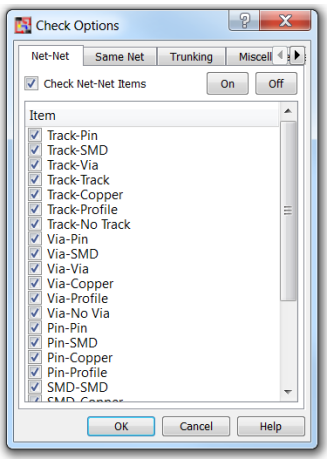
- Unrouted connections will give a design rule error during design rule checks (error code IR), but can also be run as a separate report.
- Run Routing completion from the report menu, this will give you a link to the unrouted segment if it is difficult to find.
- All connections shall be fully routed, even though you can see that the copper tracks are overlapping!

UiO : Department of Physics
University of Oslo

Routing Check in PREditor

PREditor can also be used to verify the design.

- First, set the type of check from
  - Configure->Utilities->Checks
- Uncheck the top checkbox on all other tabs than Net-Net.
- Routing check can now be performed in PREditor from
  - Utilities -> Checks -> Routing Check
- Mark the area you want to check
- Errors will be highlighted in white, and you will get an active report.



UiO : Department of Physics
University of Oslo

PREditor Same-Net check (optional)

- Checking the Same-Net checkbox will do the same error checking within a net.
- A spacing violation within a net does not tell you that you have a real electrical error, but indicates that the spacing between two copper items on the same net are smaller than the allowed spacing, and as such may be a manufacturing issue.
- Can be usefull for indicating «bad» areas in your design, but there is no need to remove all these errors.
- Same-net errors will be indicated using lower case letters for the error codes in the design and the report, while «real» errors will use upper case letters.

UiO : Department of Physics
University of Oslo

Slikscreen Cleanup

- Silkscreen printing on pads will ruin the solderability, so we need to move all text away from pads or other solder areas.
  - Select the Silkscreen Cleanup view from the views deopdown box, and move all text away from pads and vias, while it still clearly identifies the correct footprint for each chip. (When you move component text, CadSTAR will highlight the part so you know which part the text belongs to.)
  - Do this for both the top and bottom layers.

UiO : Department of Physics
University of Oslo

Add Custom text

- Add text to your board in copper and/or silkscreen.
- This can be
  - A project name for the board
  - Your name, Date, Version
  - Connector identifiers, user info
  - …
- As a minimum include name and project so it is easy to identify your board on the assembly day.
- If you add text in copper make sure to repour copper and do a new design rule check!

UiO : Department of Physics
University of Oslo

Generate production files

- To make sure all production files have the same format, we will do this step for you, but for you information:
  - The manufacturer can not read «our» CadSTAR specific pcb files, we need to convert them to a more generic format.
  - Mostly used are gerber files, which is basically an ascii file for each layer.
  - These are generated in CadSTAR from the manufacturing tab, either layer by layer or using a batch process.

UiO : Department of Physics
University of Oslo

Project files delivery

- As usual we want the .pcb and the corresponding .scm file.
- Make sure you have the correct filenaming convention:
  - Username – projectname – version

- Deadline Wednesday March 21st!