```
entity XXX is
  port (Clock : in  Std_logic;
  Reset : in  Std_logic;
  Enable: in  Std_logic;
  Load  : in  Std_logic;
  Mode  : in  Std_logic;
  Data  : in  Std_logic_vector(7 downto 0);
  X     : out Std_logic_vector(7 downto 0));
end;
```

Enable	Load	Mode	X
0	0	0	
0	0	1	
0	1	0	
0	1	1	
1	0	0	
1	0	1	
1	1	0	
1	1	1	

TASK

Fill in what X is based on the input signals (in the table)

How many FF's are created here?

What type of circuit is this / What does it do?

```
architecture doulos_model_solution of XXX is
  constant nibble_max  : Unsigned(3 downto 0) := "1111";
  constant decade_max  : Unsigned(3 downto 0) := "1001";
  constant zero_nibble : Unsigned(3 downto 0) := "0000";
  constant zero_byte   : Unsigned(7 downto 0) := "00000000";
  signal Q             : Unsigned(7 downto 0);
begin
  process (Clock, Reset)
  begin
    if Reset = '0' then
      Q <= zero_byte;
    elsif RISING_EDGE(Clock) then
      if Enable = '0' then
        if Load = '0' then
          Q <= Unsigned(Data);
        elsif (Mode = '0' and Q(3 downto 0) /= nibble_max) or
              (Mode = '1' and Q(3 downto 0) /= decade_max) then
          Q(3 downto 0) <= Q(3 downto 0) + 1;
        else
          Q(3 downto 0) <= zero_nibble;
          if (Mode = '0' and Q(7 downto 4) /= nibble_max) or
             (Mode = '1' and Q(7 downto 4) /= decade_max) then
            Q(7 downto 4) <= Q(7 downto 4) + 1;
          else
            Q(7 downto 4) <= zero_nibble;
          end if;
        end if;
      end if;
    end if;
  end process;
  X <= Std_logic_vector(Q);
end;
```