```
entity XXX is
  port (Clock : in  Std_logic;
  Reset : in  Std_logic;
  Enable: in  Std_logic;
  Load  : in  Std_logic;
  Mode  : in  Std_logic;
  Data  : in  Std_logic_vector(7 downto 0);
  X     : out Std_logic_vector(7 downto 0));
end;
```

Enable	Load	Mode	X
0	0	0	
0	0	1	
0	1	0	
0	1	1	
1	0	0	
1	0	1	
1	1	0	
1	1	1	

TASK
Fill in what X is based on the input signals (in the table)

How many FF's are created here?

What type of circuit is this / What does it do?

```
architecture prioritized of XXX is
  signal Q: Unsigned(7 downto 0);
begin
  process (Clock, Reset)
    constant decade_max  : Unsigned(3 downto 0) := "1001";
    constant zero_nibble : Unsigned(3 downto 0) := "0000";
    constant zero_byte   : Unsigned(7 downto 0) := "00000000";
    variable next_Q      : Unsigned(Q'range);
  begin
    next_Q := Q + 1;
    if (Mode = '1') then
      if (Q(3 downto 0)) = decade_max then
        next_Q(3 downto 0) := zero_nibble;
        next_Q(7 downto 4) := Q(7 downto 4) + 1;
        if Q(7 downto 4) = decade_max then
          next_Q(7 downto 4) := zero_nibble;
        end if ;
      end if;
    end if;
    next_Q := Unsigned(Data) when not Load;
    next_Q := Q when Enable;
    Q <= zero_byte when not reset else next_Q when rising_edge(Clock);
  end process;
  X <= Std_logic_vector(Q);
end;
```