

TASK

Fill in what X is based on the input signals (in the table)

How many FF's are created here?

What type of circuit is this /
What does it do?

```
entity XXX is
  port (Clock : in Std_logic;
        Reset : in Std_logic;
        Enable: in Std_logic;
        Load  : in Std_logic;
        Mode  : in Std_logic;
        Data  : in Std_logic_vector(7 downto 0);
        X     : out Std_logic_vector(7 downto 0));
end;
```

Enable	Load	Mode	X
0	0	0	
0	0	1	
0	1	0	
0	1	1	
1	0	0	
1	0	1	
1	1	0	
1	1	1	

```
architecture mixed of XXX is
  constant zero_byte: std_logic_vector(7 downto 0) := "00000000";
  function dec_count(input: Unsigned) return Unsigned is
    constant decade_max : Unsigned(3 downto 0) := "1001";
    constant zero_nibble: Unsigned(3 downto 0) := "0000";
    variable output      : unsigned(input'range);
  begin
    output :=
      input + 1
      when input(3 downto 0) /= decade_max else
      (input(7 downto 4) + 1) & zero_nibble when input(7 downto 4) /= decade_max else
      unsigned(zero_byte);
    return output;
  end function dec_count;
begin
  process(Reset, Clock) is
    variable Q : Unsigned(7 downto 0);
  begin
    if Reset = '0' then
      X <= zero_byte;
    elsif rising_edge(Clock) then
      Q :=
        unsigned(X)      when Enable   else
        unsigned(Data)   when not Load else
        unsigned(X) + 1  when not Mode  else
        dec_count(unsigned(X));
      X <= std_logic_vector(Q);
    end if;
  end process;
end;
```