Guest lecture in FPGA development

Thursday 7 April
@12:15-14:00
OJD, seminarrom C

EmLogic
a part of the TechSeed group

Do you consider working as an FPGA or ASIC designer?
If so – this guest lecture could give you a major advantage.

1. The good, the bad and the ugly

The way you implement your FPGA design and write your code has a huge impact on your development efficiency and product quality. The strange thing is that even many experienced designers tend to write both bad and ugly code. But – does it really matter if the code is ugly if it works in the lab?
- Yes, definitely! Bad and ugly code often results in errors that may be difficult to find and terrible to correct. This presentation will show some examples of bad and ugly code, how they result in inefficiency or bugs, and also suggest some remedies and suggestions for improvements – in order to write good code.

2. Design, Verification and some general views on becoming a good FPGA or ASIC developer

Selected excerpts from our design and verification courses and comments on these both in general for the industry - and some special considerations for students.

Presentations by Espen Tallaksen, Founder and CEO of EmLogic,
already a leading design centre for FPGA development in Scandinavia.
(Espen was also the founder and CEO of Bitvis)