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Guest lecture in FPGA development

Thursday 7 April
@12:15-14:00
OJD, seminarrom C

EmLogic
a part of the TechSeed group

Do you consider working as an FPGA or ASIC designer?
If so – this guest lecture could give you a major advantage.

1. The good, the bad and the ugly

The way you implement your FPGA design and write your code has a huge impact on your development efficiency and product quality. The strange thing is that even many experienced designers tend to write both bad and ugly code. But – does it really matter if the code is ugly if it works in the lab?
- Yes, definitely! Bad and ugly code often results in errors that may be difficult to find and terrible to correct. This presentation will show some examples of bad and ugly code, how they result in inefficiency or bugs, and also suggest some remedies and suggestions for improvements – in order to write good code.

2. Design, Verification and some general views on becoming a good FPGA or ASIC developer

Selected excerpts from our design and verification courses and comments on these both in general for the industry - and some special considerations for students.

Presentations by Espen Tallaksen, Founder and CEO of EmLogic,
already a leading design centre for FPGA development in Scandinavia.
(Espen was also the founder and CEO of Bitvis)

Source Presentations

Bugs and problems
- worst disasters

Bugs and Problems
– And how to avoid them

Intended for the industry

The electronics industry
is suffering from bad priorities
in the university education

Norcas, Oslo, 27. Oct. 2015

Intended for Academia

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We are recruiting…

- A Design Centre yields a major competence and experience kick-start
- We are 10 FPGA designers – (5 Principals and 2 Seniors)
  - The most experienced Design centre in Norway on FPGA
  - Major growth and experience also on ESW, HW and DSP
- EmLogic offers significant ownership to all employees
  - More and at a lower cost than anybody else in our business
- 'Fair' and 'Teamwork' are keywords in EmLogic
  - ➔ No individual benefits/extras
  - ➔ Paid overtime, and Paid additional travel time
  - ➔ 1/3 of the result given as bonus (prop. salary)
  - ➔ People help each other
- We specialise on Embedded only – HW, ESW, FPGA and DSP
  - Allows more focused methodology, competence, culture, and professional pride

Customers – so far

KONGSBERG

FPGAs often result in a better product

- One device does “everything”
- Extreme Flexibility
- May significantly improve performance
- May significantly reduce power consumption
- May significantly improve Quality and MTBF
- May significantly improve LCC

Great opportunities, but....

- Exploding functionality
- Massively Parallel
- Interfaces and functionality are buried
- More than just design for functionality
- Timing is often really complex
- Requires advanced methodology and tools
- **Requires structure - everywhere**

How do we handle these challenges?

- We structure our design, - but not sufficiently
- We exploit the parallelism
  - and make a "mega multi thread" system...
- We integrate, test and debug a lot
  - Patching and leaving an unstable product...
- We do analyse timing
  - But far from good enough...
- We know about clocking problems
  - But very few know how to handle them properly...
- We do document, but very far from sufficient
- We do simulate, but we don't like it - and it shows…
- **We are not structured at all!**

Consequences
- of not being sufficiently structured

- Project Delays
  - → Bad estimates
  - → Wasting time
- Quality of end product
  - → Takes forever to get sufficient quality, or
  - → Problems pop up at later stages

Safe and efficient reuse?

Experience shows that
Quality often comes at the cost of Schedule

Experience also sometimes shows that
Quality and Efficiency **<u>may</u>** go hand in hand...

Resulting **product delays** - selected examples from the industry

- 2 m … test
- 1 ye… (pa… …ng, …)
- 6 m…
- "Sta… 1-3… …roblems

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Resulting **product deficiencies** - selected examples from the industry

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FPGA knowledge and experience

- There are many excellent FPGA designers,
  - but far too many have insufficient FPGA knowledge or experience
  - and - are all "excellent" FPGA designers really that excellent....?
- Most FPGA-projects …
  - … have insufficient team experience - resulting in severe bugs
  - … make terrible testbenches – wasting a lot of time
- Proper FPGA development **requires**:
  - proper knowledge of **HW, FPGA-technology and Digital design**
  - **Structure** for **Design and Verification**
  - And **Sufficient time** to structure Design and Verification
  - **Quality** Assurance **at the right level**
  - A proper **Methodology**

Fresh graduates are ticking bombs

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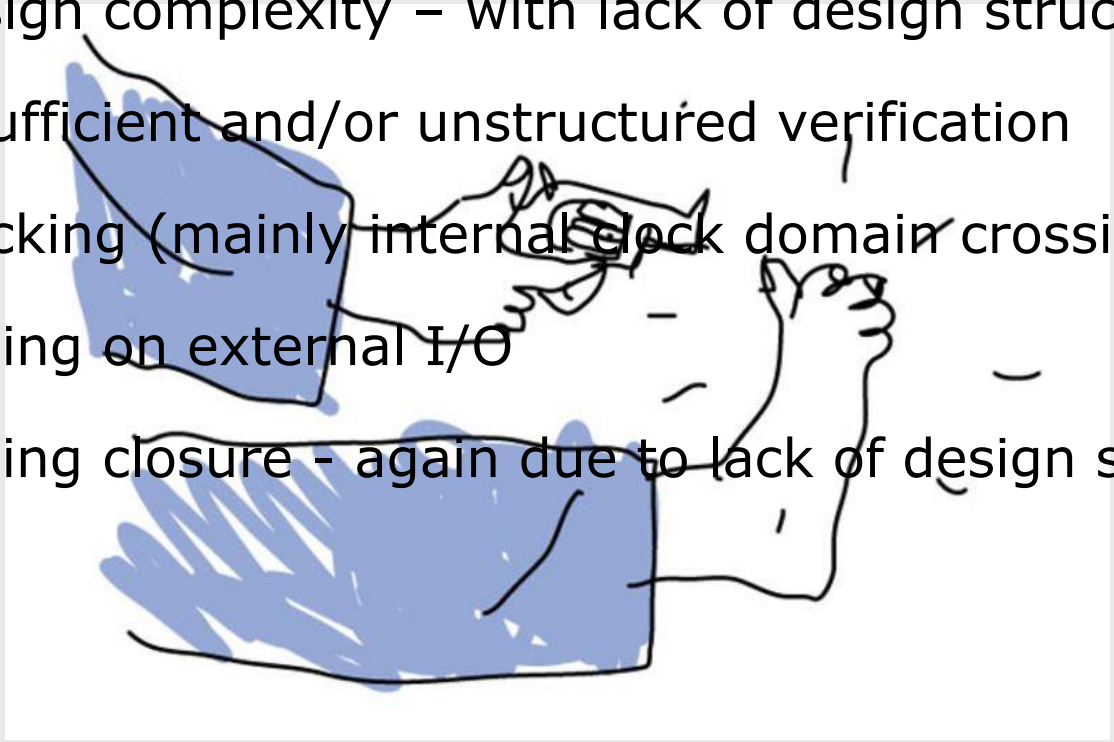
Main Problem Areas

- Most serious "self inflicted" quality and efficiency problems arise from four main problem areas
  - Design complexity – with lack of design structure
  - Insufficient and/or unstructured verification
  - Clocking (mainly internal clock domain crossing)
  - Timing on external I/O
  - Timing closure - again due to lack of design structure



The "architecture paradox"

We KNOW a good architecture is essential

We KNOW a good block diagram is essential

➔ **Overview, Readability, Maintainability, Extensibility, Reuse**

➔ **Specification, Design, Modification, Sparring, Reviews, ...**

BUT - we don't do it properly!

→ For Design - Not just at top level,
but also Micro Architecture - all the way down

→ For Verification - Should be as for Design

WHY don't we do this properly?

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Severe Consequences ???

- Some designs have a really simple implementation
- Sometimes you are just lucky
- Sometimes Murphy hits you hard
- Often you are unknowingly hit
  - Delays are assumed normal?
  - Late bug detection is assumed normal?
  - Problems are treated as unfortunate exceptions?
  - Problems are not reported?
  - End customer accepts rare bugs?

What is the industry doing about this today?

- Major difference from one company to the other
  - Mostly from nothing to almost nothing
  - A very small minority handle this properly
- Most companies believe they address risk issues properly
  - ISO certification
  - QA procedures

  ➔ Normally a waste of time for real development improvements
- Most companies are not aware of their challenges
  - Little awareness of current status
  - Often no awareness of their improvement potentials

Lack of industry awareness

- Very many companies only have a single FPGA designer
  - or just a 50% FPGA designer
- Lots of companies have 2-3 FPGA designers
  - Sometimes with some methodology coordination
  - Companies with more FPGA designers - not necessarily better
  - Mainly dependent on local "champions"

Companies with one single FPGA designer do not necessarily have simpler FPGAs...

- Very few companies have a good follow up for inexperienced designers in a project
- Almost no company has a training programme for inexperienced designers
- There is very little awareness in the industry on FPGA development challenges.

A typical management pitfall (or attitude problem?):
- " We have developed complex FPGAs before...."
- "This doesn't apply to us"

Why is this important for students?

- You are the **main** ticking bombs
  - but not only you
  - Some designers with long experience may also not have the **right** experience…
- It is important to be aware of to understand that
  - you lack important experience
  - you need to ask experienced designers
  - some areas are more critical than others
- You could improve your knowledge
  - By checking out relevant books, webinars, etc
  - Some stuff available from EmLogic:
    - 4-part webinar on design and verification via Aldec starting 28 April
    - Blog for Siemens EDA 'How to avoid delays in FPGA … projects'
    - The most error prone FPGA corner cases, Webinar for Aldec
    - UVVM The main benefits of the world's #1 VHDL Verification Methodology, Webinar for Siemens EDA
    - Check out our web-site for more on UVVM:

Unique training in EmLogic

- We have experienced designers who want to help novice designers
  - Mentors and Sparring partners
- We run all fresh designers through
  - our FPGA design course & our FPGA verification course
  - real cases on how to specify, architect, code, synthesize and verify an FPGA
  - Similar is being done for SW and HW
  - Last internal FPGA training session Q4, 2022
    - 2 Designers
    - 3 Months
    - 3 Different modules
    - Specification, Architecture, Implementation/coding, Verification, Synth/P&R
    - Huge improvement from first to last design
  - An alternative is to have a Mentor in a real project

Who else does this…?

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Feel free to connect

I publish quite a bit on LinkedIn, so feel free to connect:
https://www.linkedin.com/in/espentallaksen/

Check out articles on us in Magasinet Elektronikk (Norwegian only):
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