# Oblig 5
# VHDL Subprograms and packages - Functions and Procedures, Packages and Libraries

IN3160/4160

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In this exercise, we will explore VHDL functions and learn to create VHDL packages. We will also start to build a self-checking testbench with Cooctb.
Optionally, a2) will highlight some architecture features in FPGA design.

**a)** Simulate the attached code in **pargen.vhd** and **tb_pargen.py** (the given **Makefile** may be used). Here two 16-bit vectors *(indata1* and *indata2)* are read in and a parity signal *(par)* is generated.
Create a PNG-image of the simulation result.
(gtkwave: File->Grab to file)

**b)** Modify the code in **pargen.vhd** to encapsulate the two different methods in separate functions for creating parity calculation.

**c)** Move the functions in b) to a subprog_pck package. Modify **pargen.vhd** from part b of the exercise to use the functions from the subprog_pck package.

**d)** Modify the given **tb_pargen.py** and complete change the function *stimuli_generator()* so that it generates randomized stimuli for *indata1* and *indata2*.
- Complete the function *compare()* to verify that the output *par* is correct. (Use assertions)
*Hint: output par updates only on rising_edge(mclk).*
- You may use the provided functions *parity(value)* and *parity_predict(dut)* to calculate the expected value of the output *par*.

Hint #1: Type conversions can be a bit tricky in VHDL. Going from integer to std_logic_vector requires deciding on whether you will use signed data or not. Here is an example on how to convert from integer to an arbitrary length std_logic_vector using numeric_std and std_logic_1164 libraries:

```
my_var := std_logic_vector( to_unsigned(i, my_var'length) );
```

## Approval:

- Simulation result (png)
- VHDL source file for the individual questions.
- Modified tb_pargen.py
- Optional: Answers to optional questions (below).

a2) (optional addition after a))

Create a project using the pargen.vhd file *before* modifications) in Vivado. (Remember to select VHDL 2008 for both sources).
Open the *RTL-analysis->Elaborated Design*, and look at the schematic generated. Zoom in and compare the paths of the parity_toggle and the XOR_Parity (RTL_REDUCTION_XOR).

- How many gates is required for each path?
  (Not counting inverters, only (N)AND/ (N)OR/ X(N)OR).
- If we would implement this schematic in a full custom ASIC, which version would be favorable? (consider how many gate delays they will induce)

Synthesize the design, and open the synthesized design schematic. Note that the differences you will see compared to the RTL schematic are mostly due to the FPGA architecture consisting of logical blocks having mostly look-up tables (LUTs) and flip-flops.

Does it seem to make any difference whether our code indicates the use of multiplexers or reduction XOR if we implement it on a Xilinx Zynq-series FPGA?