Front page

Written Home Exam in IN3170/4170

Spring 2012

Duration: 2-June 9:00 to 2-June 13:00

It is important that you read this cover page carefully before you start.

General information:

- Important messages during the exam are given directly from the course teacher on **the course's MS Teams channel (team name: 'IN3170/4170 Spring 2021', new channel: 'Exam')**. It is therefore important that you check this channel regularly. If anything is not clear during the exam you may post questions as direct **personal messages to the lecturer only (!)** on Teams, i.e. to Philipp Häfliger (Go to 'Chat' in Teams, click on the 'new chat' symbol (a square with a dash in the upper right corner) and type in 'hafliger' as the recipient). Anwers will appear on the 'Exam' channel. Do not post anything on any other Teams channel during the exam!
- Your answer should reflect your own independent work and should be a result of your own learning and work effort.
- All sources of information are allowed for written home exams. If you reproduce a text from books, online articles, etc., a reference to these sources must be provided to avoid suspicions of plagiarism. This also applies if a text is translated from other languages.
- You are responsible for ensuring that your exam answers are not available to others during the exam period, neither physically nor digitally.
- Remember that your exam answers must be anonymous; do not state either your name or that of fellow students.
- If you want to withdraw from the exam, press the hamburger menu at the top right of Inspera and select "Withdraw".

Collaboration during the exam:

It is not allowed to collaborate or communicate with others during the exam. Cooperation and communication will be considered as attempted cheating. A plagiarism control is performed on all submitted exams where text similarities between answers are checked. If you use notes that have been prepared in collaboration with others before the exam, this might be detected in a plagiarism control. Such text similarities will be considered an attempt at cheating.

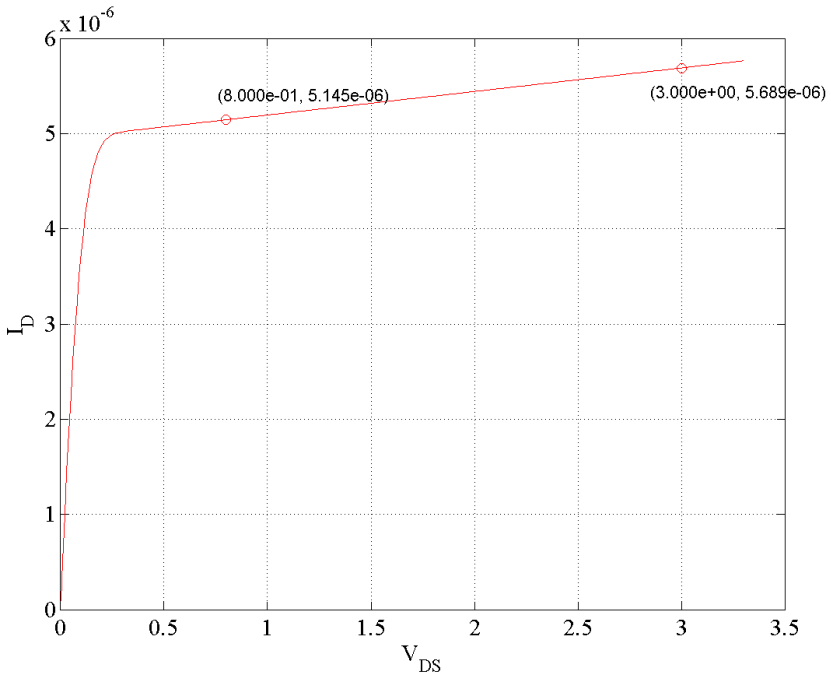
Cheats:

Read about what is considered cheating on UiO's website.

Digital hand drawing / file upload:

You have been given 30 min. extra time for uploading files (e.g. digital hand drawings). Check out how to submit digital hand drawings

Contact information: User support exam



From the i_D vs v_{DS} graph shown and the marked points, compute the parameter λ.

Give all answers with at least three significant digits accuracy! Note the specific units that the answers should be given in (i.e. do not overlook any 'micro-', 'milli-', 'mega-' or similar prefixes)!

$\lambda =$ [ ] $\frac{1}{\mathrm{V}}$

Maximum marks: 1

2 nFET large signal model

An nFET is to be operated in the saturation region/active region at a current of 20μA. It's $k_n' \frac{W}{L} = 70 \frac{\mu \mathrm{A}}{\mathrm{V}^2}$ and its threeshold voltage $V_{tn} = 650\mathrm{mV}$. (You may assume parameter $\lambda = 0$). What is its required gate to source voltage v_{GS} and minimum drain to source voltage $v_{DS,min} = V_{sat}$?

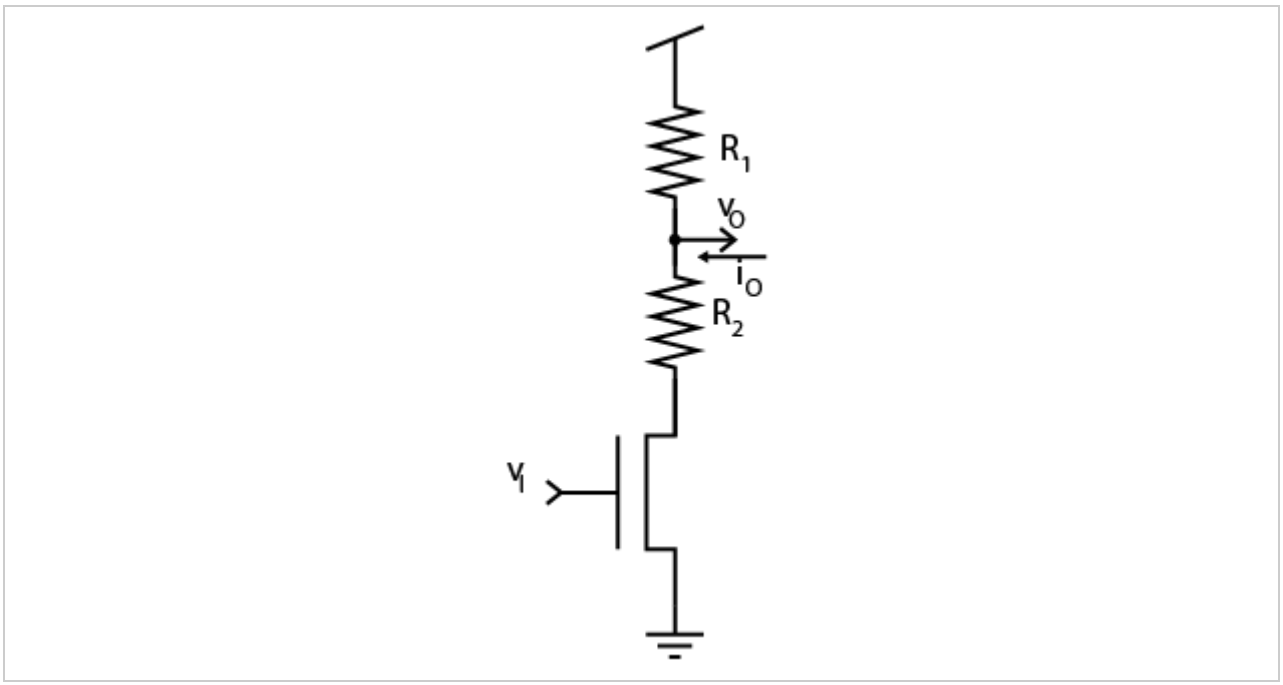
Give all answers with at least three significant digits accuracy! Note the specific units that the answers should be given in (i.e. do not overlook any 'micro-', 'milli-', 'mega-' or similar prefixes)!

$v_{GS} =$ [ ] V

$V_{sat} =$ [ ] V

Maximum marks: 1

3 Small signal analysis



For the circuit in the schematics perform a small signal (!) analysis and find an expression for the total output resistance $R_O = \frac{v_o}{i_o}$ and the total transconductance $G_M = \frac{i_o}{v_i}$ and the gain $A = \frac{v_o}{v_i}$! To form your expressions you may use the small signal variables g_m, r_o of the transistor as well as the resistors R_1, R_2. In other words express these terms as functions of those four variables (or a subset of them).

$R_O = f_1(g_m, r_o, R_1, R_2) =$

$G_M = f_2(g_m, r_o, R_1, R_2) =$

$A = f_3(g_m, r_o, R_1, R_2) =$

Maximum marks: 1

4 Intrinsic gain

Given process parameters:
$\mu_n C_{ox} = 280 * 10^{-6} \frac{\mathrm{A}}{\mathrm{V}^2}$, $\frac{1}{\lambda * L} = \frac{V_A}{L} = V_A' = 5 * 10^6 \frac{\mathrm{V}}{\mathrm{m}}$, $V_{tn} = 0.5\mathrm{V}$, for an NFET of length $L = 0.4\mu\mathrm{m}$, $V_{OV} = 0.15$, and opperated at a drain current $i_D = 80\mu\mathrm{A}$, find transconductance, drain resistance in the active/saturation region, intrinsic gain and transistor

width: g_m, r_o, A_0, W!

Give all answers with at least three significant digits accuracy! Note the specific units that the answers should be given in (i.e. do not overlook any 'micro-', 'milli-', 'mega-' or similar prefixes)!

$g_m =$ [ ] $\frac{\mu\mathrm{A}}{\mathrm{V}}$

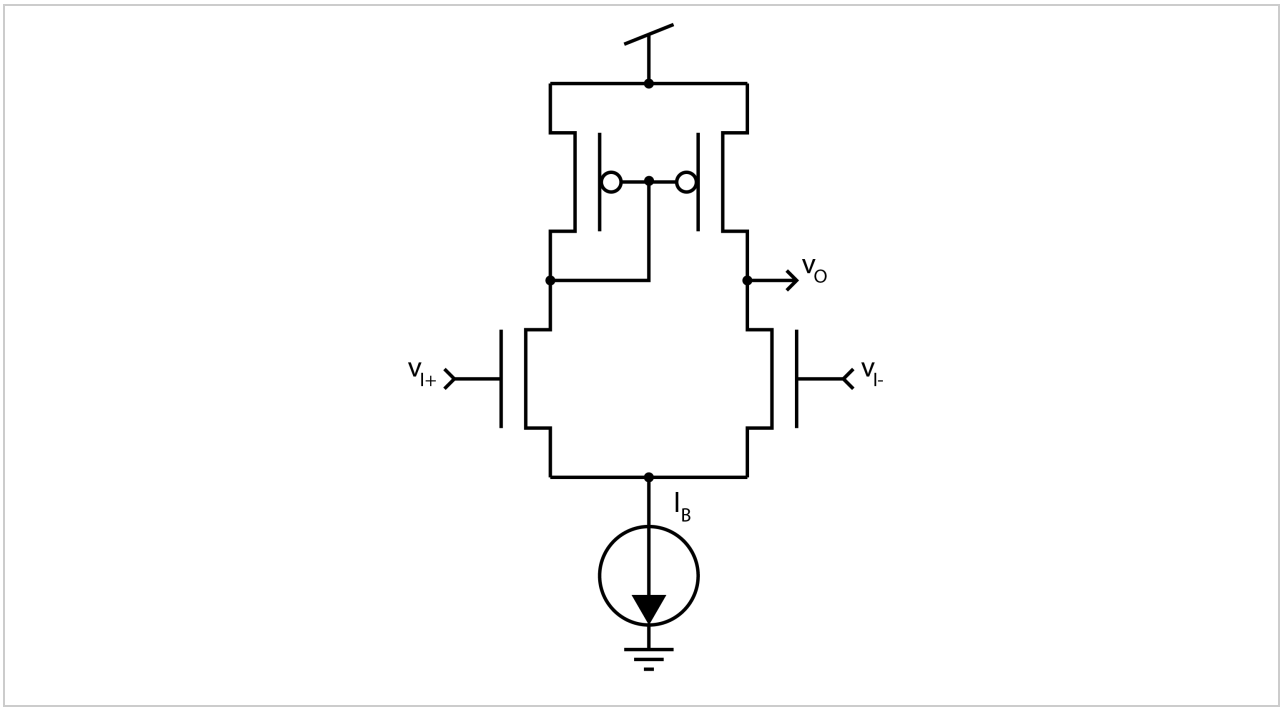
$r_o =$ [ ] Ω

$A_0 =$ [ ] $\frac{\mathrm{V}}{\mathrm{V}}$

$W =$ [ ] $\mu\mathrm{m}$

Maximum marks: 1

5 Current mirror loaded differential pair



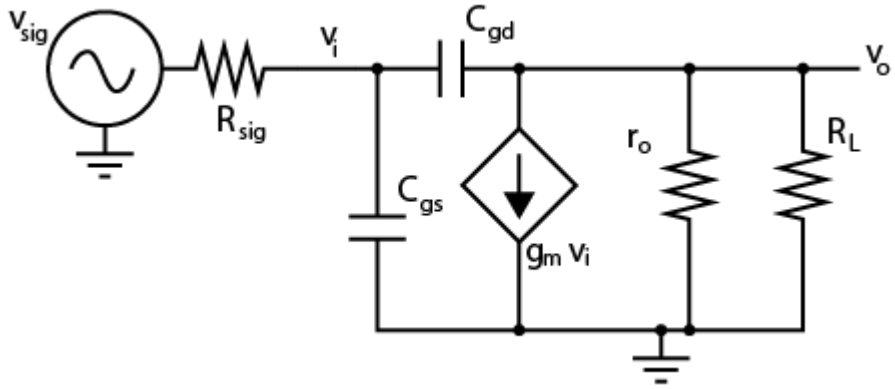
An nFET differetial pair is loaded with a pFET current mirror and an ideal current source provides a bias current I_B of 100μA (i.e. this is a current mirror loaded differential amplifier, see illustration). Compute its differential small signal gain $A = \frac{v_o}{v_{i+} - v_{i-}}$ if $k_n = k_n' \frac{W}{L} = 500\mu\mathrm{A}$ and $k_p = k_p' \frac{W}{L} = 300\mu\mathrm{A}$ and the Early voltage $V_A = \frac{1}{\lambda} = 20\mathrm{V}$ for both type of transistors is.

Give all answers with at least three significant digits accuracy! Note the specific units that the answers should be given in (i.e. do not overlook any 'micro-', 'milli-', 'mega-' or similar prefixes!

$A =$ $\frac{\mathrm{V}}{\mathrm{V}}$

Maximum marks: 1

6 CS gain stage and Miller capacitance



The illustration shows the small signal model of a CS gain stage. Given that $g_m = 1\frac{\mathrm{mA}}{\mathrm{V}}, r_o || R_L = 30\mathrm{k\Omega}$, $R_{sig} = 4.8\mathrm{k\Omega}$, $C_{gs} = 100\mathrm{fF}$ and the -3dB cut off is $\omega_{-3\mathrm{dB}} = 100\mathrm{Mrad}$, what is the DC gain A_{DC} and C_{gd}?

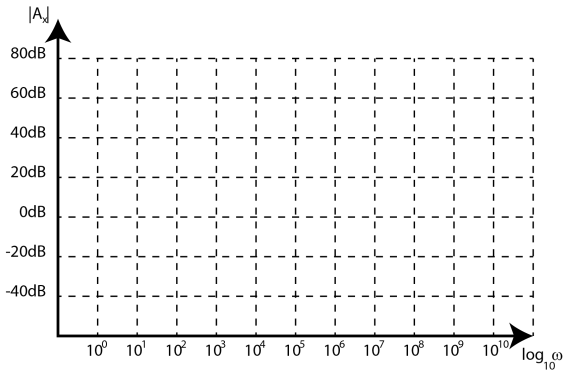
Give all answers with at least three significant digits accuracy! Note the specific units that the answers should be given in (i.e. do not overlook any 'micro-', 'milli-', 'mega-' or similar prefixes)!

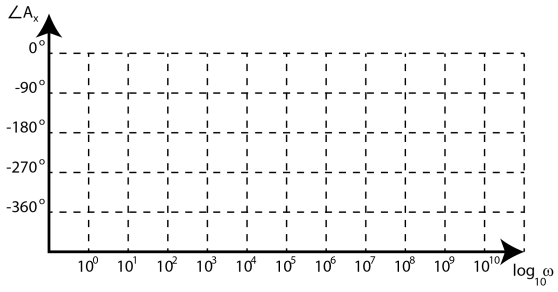
$A_{DC} =$ $\frac{\mathrm{V}}{\mathrm{V}}$

$C_{gd} =$ fF

Maximum marks: 1

7 Draw Bode plot





Draw the Bode plots (both magnitude and phase!) for the following two transfer functions A_1 and A_2. The x-axis should extend at least 1 decade beyond the highest pole or zero frequency. Use a grid like the one in the illustration! Draw the plots as 'piece-wise linear' approximation of the real graphs, like on the lecture slides: for phase transitions use either $\pm$one decade (like in FYS3220) or $\pm$half a decade (like in the graphs on the lecture slides) around the respective pole or zero to complete the full phase shift. For cut-off frequencies in the magnitude plots make an abrupt transition/knee point at the respective pole or zero to change the slope of the magnitude.

$$A_1 = A_{DC1}\frac{(1+\frac{s}{\omega_{z11}})}{(1+\frac{s}{\omega_{p11}})(1+\frac{s}{\omega_{p12}})}$$

where $A_{DC1} = 10^3, \omega_{p11} = 10^3\text{rad}, \omega_{p12} = 10^8\text{rad}, \omega_{z11} = 10^6\text{rad}$

$$A_2 = A_{DC2}\frac{(1+\frac{s}{\omega_{z21}})(1-\frac{s}{\omega_{z22}})}{(1+\frac{s}{\omega_{p21}})(1+\frac{s}{\omega_{p22}})(1+\frac{s}{\omega_{p23}})}$$

where
$A_{DC2} = 10^4, \omega_{p21} = 10^3\text{rad}, \omega_{p22} = 10^7\text{rad}, \omega_{p23} = 10^9\text{rad}, \omega_{z21} = 10^5\text{rad}, \omega_{z22} = 10^7\text{ra}$

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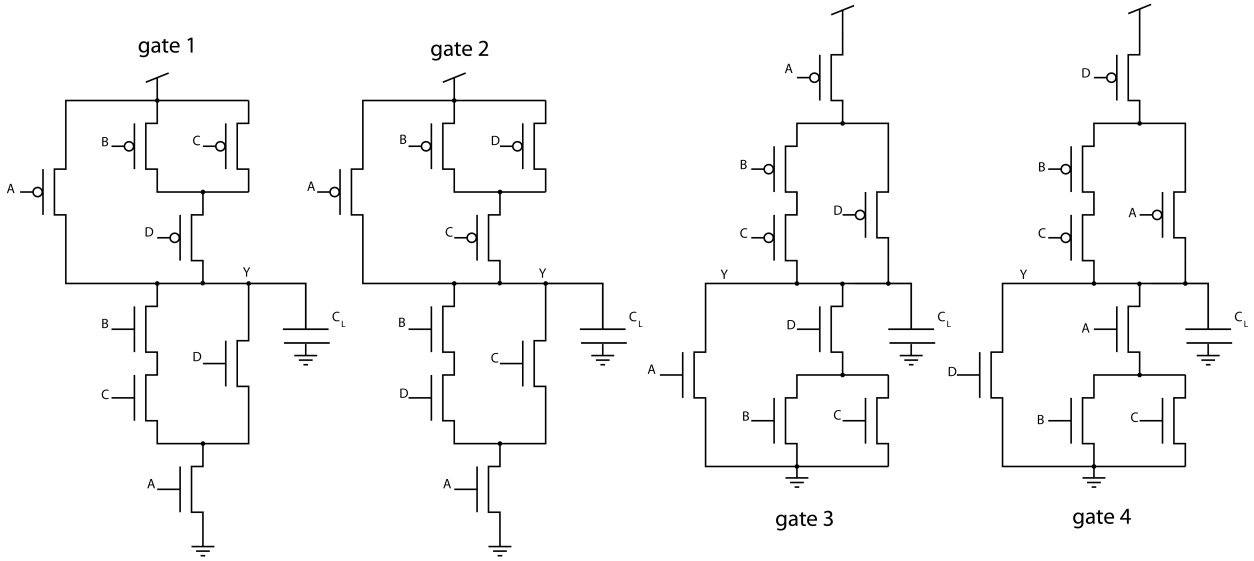
Maximum marks: 1

8 Propagation delay



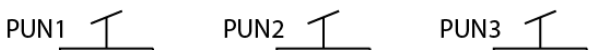
Please order these digital gates by their propagation delays (fastest on top, slowest on the bottom) in a particular situation: specifically the delay for output signal Y to switch after the input signal A switches from low to high while input signals B and C are, and remain, high and signal D is ,and remains, low. The transistors have all the same W/L ratio and C_L is the same for all gates. Should two gates have the same delay, just order them next to each other and it does not matter which one you place before the other.

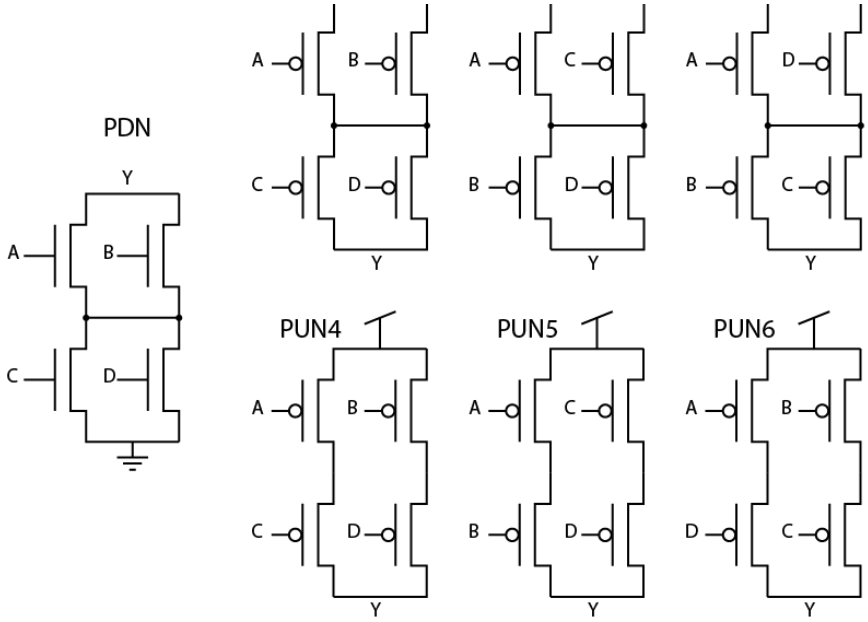
Please match the values:

	gate 1	gate 2	gate 3	gate 4
fastest transition, smallest delay	○	○	○	○
2nd fastest	○	○	○	○
2nd slowest	○	○	○	○
slowest, longest delay	○	○	○	○

Maximum marks: 1

9 Complementary PUN/PDN





Which of these pull up networks (PUN) would complement the pull down network (PDN) shown. Multiple answers may be possible.

Select one or more alternatives:

- [ ] PUN1
- [ ] PUN2
- [ ] PUN3
- [ ] PUN4
- [ ] PUN5
- [ ] PUN6

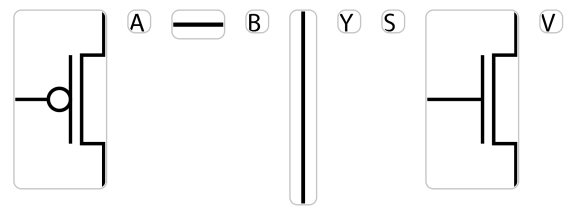
Maximum marks: 1

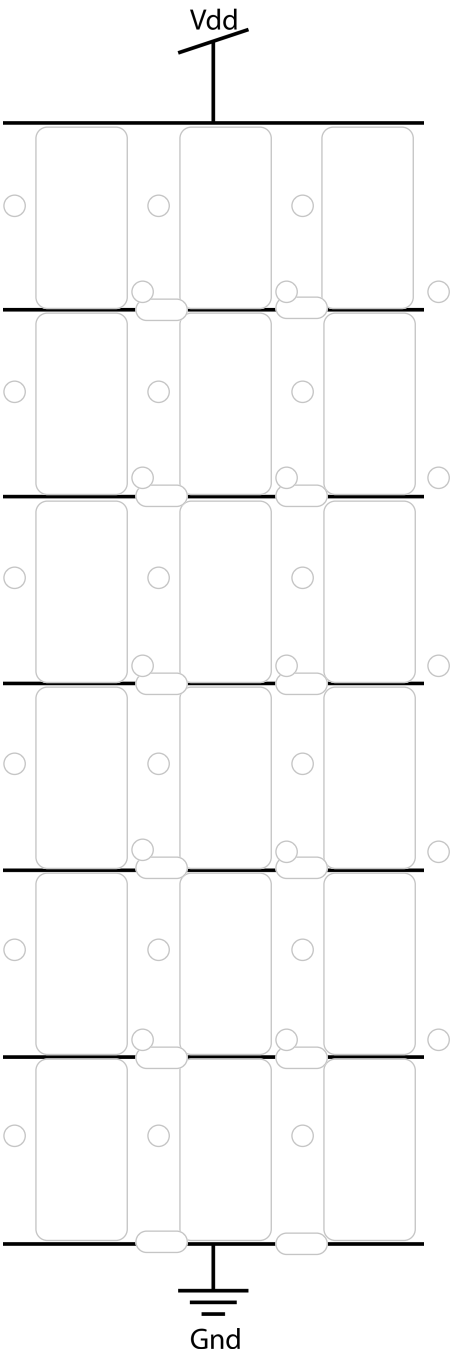
10 AND gate circuit diagram

Implement a static two input AND gate (Note: not a nand gate like in the test exam!) with complementary PUN and PDN and input signals A and B , possibly internal signals S and V and output signal Y. Place appropriate transistor symbols into the vertical rectanglular fields where needed. You may also place vertical shorts into those fields, and horizontal shorts into the small horizontal rectangular fields where needed. The appropriate signal names go into the smallest fields. Note that if you happen to place the same signal name in two places, these nodes are

assumed to be shorted. **HINT:** this way you can connect source/drain nodes to gate nodes.

Help





Maximum marks: 1

11 Draw NP Domino Logic

Draw an NP Domino logic schematic implementing the following expression. Use nFETs and pFETs, a Vdd and Gnd power supply and static (!) input signals and their inverse $A, \bar{A}, B, \bar{B}, C, \bar{C}$, as well as a clock signal and its inverse $\phi, \bar{\phi}$. The precharge phase happens when ϕ is low and the evaluation phase when ϕ is high. Use footed logic gates! Mark the output node Y! The function Y with three input variables shall not be implemented with a single logic gate with three inputs, but **connect multiple gates with just two inputs each together**. You might want to use the de'Morgan theorem to transform some of the expression into a form that lends itself more easily to be implemented in NP Domino logic.

The expression is:
$Y = (A \vee B) \wedge C$
where $\wedge$ is the AND operation and $\vee$ is the OR operation.

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Maximum marks: 1

12 Surveillance control system

Design a simple synchronous (i.e. there is a CLK signal that you do not need to represent explicitly, and state transition only occure synchronously with the rising edge of that clock signal) Moore-type finite state machine (FSM) to control a 'smart' burglar alarm. It shall have three states: 'asleep', 'attentive', and 'alarm'. It receives two binary sensor inputs: 'Movement' and 'human intruder'. It's default state is 'asleep' where it consumes very little energy and only motion sensors are active. They activate signal 'M' which is 0/false when there is no movement and 1/true if there is movement. If movement is detected the system enters its 'attentive' state, trurning on a power consuming intelligent sensor system that processes camera images to detect the shape of a human being and distinguishes it from motion triggered by animals or by plants moved by the wind. Humans are signaled by the signal 'H' being 1/true and the system goes to state 'alarm'. On the other hand, if no human shape is detected, 'H' is 0/false and the system goes back to state 'asleep' until the next time it detects motion. An alarm remains active as long

as there continues to be motion. If the movement stops, the system goes back to 'asleep'.

1) Draw a state transition graph for this FSM. In the state 'bubbles', do indicate the name and the binary encoding (!) of that state. Attention: if there are fewer states than your binary encoding would allow, make sure to incude those 'undefined' states as well with an unconditional transition to the 'asleep' state: that's always good policy in case your circuit ends up in this undefined states by mistake, e.g. during power up of your circuit!

2) Make a state transition table with columns for the 'state now' with as many bits as necessary, with the two one bit input variables H and M, and with the 'next state'. Use binary variable values, 0, 1, and you may use an X for "don't care" states/inputs to simplyfy. Make sure to include all possible states and inputs in the table.

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Maximum marks: 1