UiO : Department of Informatics
University of Oslo

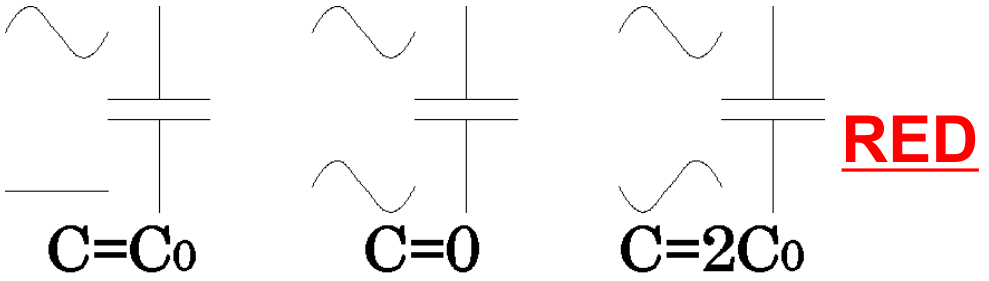
**IN5230**
**Electronic noise –**
**Estimates and countermeasures**

# Lecture 13 (Mot 10)
# Amplifier Architectures

# Miller capacitance

Before we look at the transistor configurations we need a fast repetition of the Miller effect.

- When a capacitor is connected between a signal line and a stable potential the signal line will experience a capacitance according to the standard formula ($C=\varepsilon A/t$).
- If the potential on the other side are in phase a smaller capacitance will be experienced. If the signal is exactly equal the capacitance will "disappear".
- If the signal is in opposite phase the experienced capacitance will be larger. If it is in opposite phase and exactly equal the capacitance will be double.



# Transistor configurations:

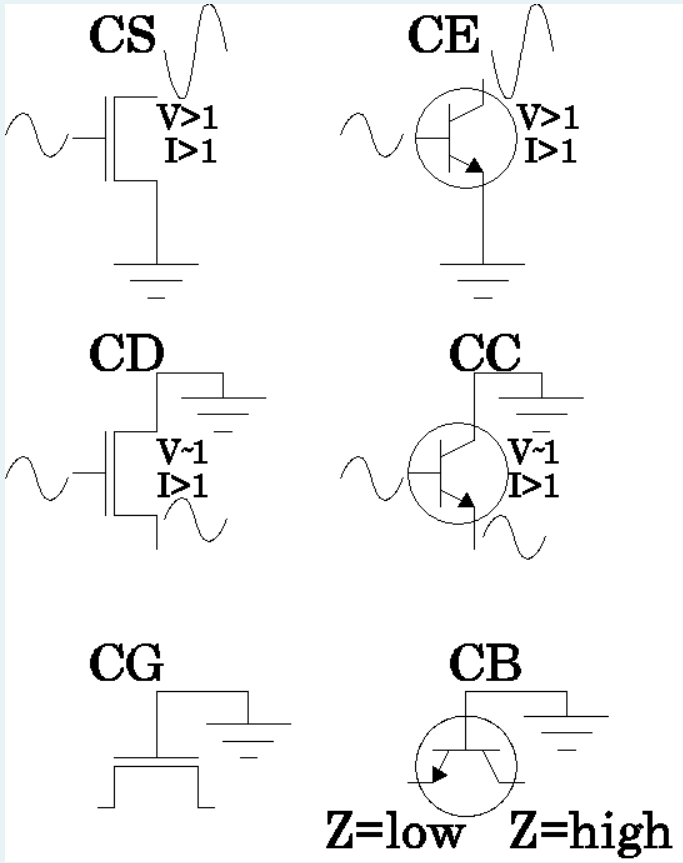
- There are mainly three alternatives for placing a FET/BJT in an architecture:

**CS/CE** has both voltage and current amplification resulting in the highest gain. But it has also the highest input capacitance (due to the Miller effect)

**CD/CC** has a high current gain but a voltage gain close to one. It has a low input capacitance (from the Miller effect) resulting in a high input impedance. It also has low output impedance.

**CG/CB** is used to achieve low input impedance and high output impedance.

| FET | BJT | |
|---|---|---|
| CS: Common Source | CE: Common Emitter | |
| CD: Common Drain | CC: Common Collector | |
| CG: Common Gate | CB: Common Base | |

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# 10-2 Common Emitter

The schematic shows a transistor that is biased for low noise operation between 10Hz and 10kHz.
The noise values are as follows:

| | 10Hz | 10kHz |
|---|---|---|
| En | 2nV | 2nV |
| In | 2pA | 0.3pA |
| R0 | 1000Ω | 6700Ω |
| NF@R0 | 1.8dB | 0.3dB |

The noise schematic shows a hybrid-π model together with passive bias elements.

Note that when VEE and VCC are stable DC-sources, they are merged together with ground during noise analysis.

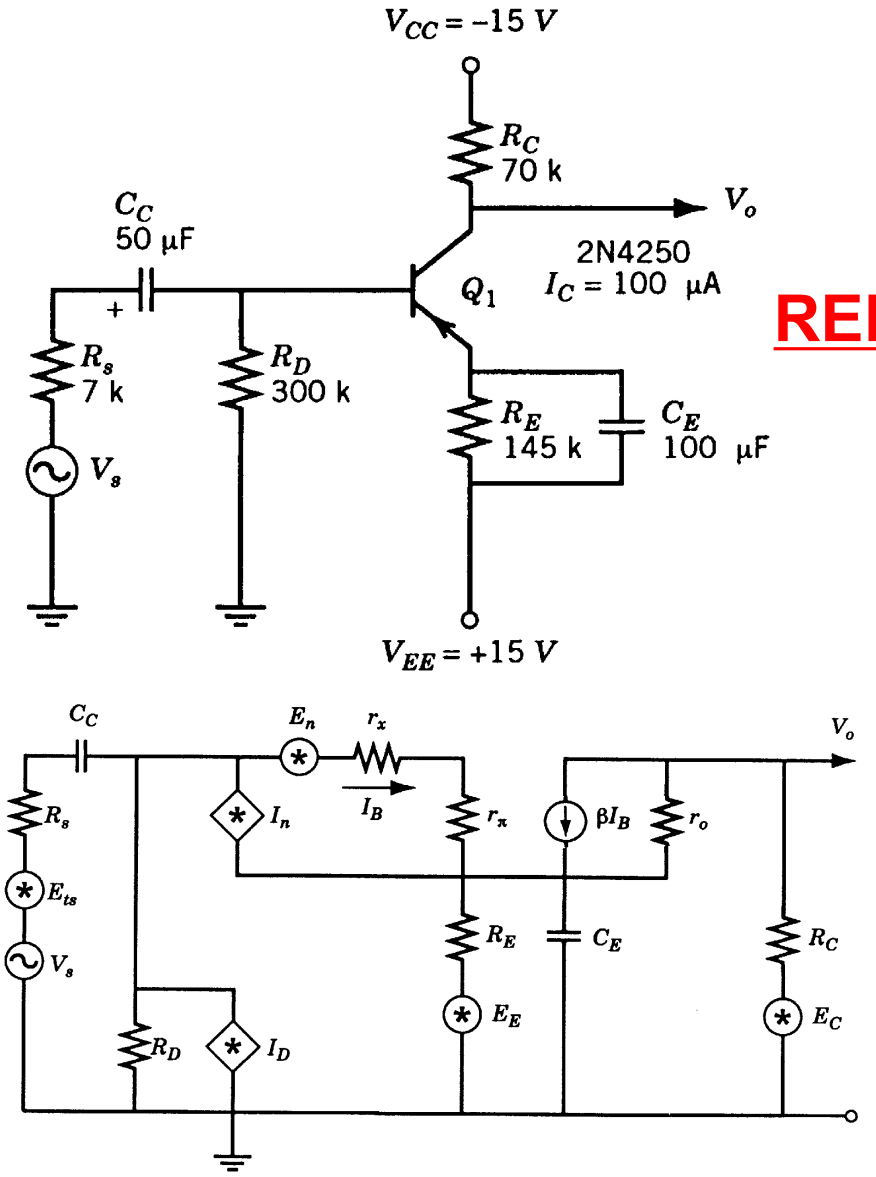


**Figure 10-2** Noise and small-signal equivalent circuit for CE stage.

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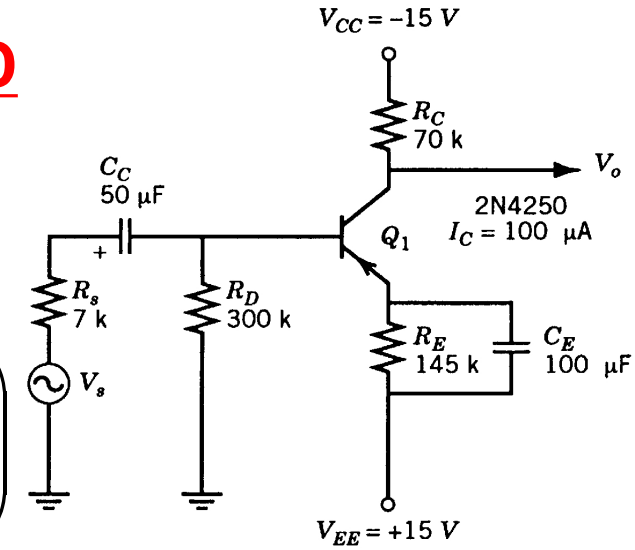
# The voltage gain Kt:




$$K_t \cong \left(\frac{-\beta R_L}{Z_i}\right)\left(\frac{Z_i \,||\, R_D}{Z_S + Z_i \,||\, R_D}\right)$$

*Kt* is the voltage gain from *Vs* to *Vo*. The first parenthesis is the voltage gain within the transistor ($\beta$ is $I_{CE}/I_{BE}$) while the second parenthesis is the network in front of the base.

$$Z_i = r_x + r_\pi + (\beta + 1)Z_E$$

The input resistance $Z_i$ includes the resistance you can see through the base towards emitter.

$$R_L \cong R_C \,||\, r_0 \,||\, R_{i2}$$

The load resistance consists of the collector bias resistance, the transistor internal resistance and the input resistance of the next stage: $R_{i2}$.

$$Z_E = R_E \,||\, -jX_E$$

The emitter impedance consists of a real part and an imaginary part (a resistance and a capacitance in parallel).

$$Z_S = R_S - jX_C$$

The source impedance is a resistance in series with a capacitor.

If we assume ignorable loss in biasing, coupling and feedback we can simplify the expression for *Kt* to:

$$K_t \cong -\frac{\beta R_L}{Z_S + r_x + r_\pi + \beta Z_E}$$

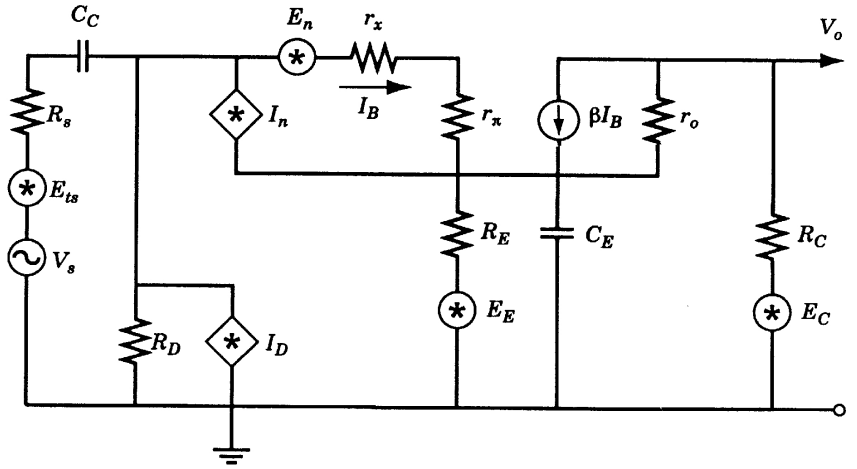



**Figure 10-2** Noise and small-signal equivalent circuit for CE stage.

If $Zs \ll r_\pi$ and $Z_E \ll r_e$ the expression is simplified to:

$$K_t \cong -\frac{R_L}{r_e} = -g_m R_L$$

If we simplify and ignore the external load we have:

$$K'_t = K_t \quad for \quad R_L = R_C$$

We will then have the following expression for the equivalent input noise:

$$E_{ni}^2 \cong E_{ns}^2 + E_n^2 \left(\frac{R_S+R_D}{R_D}\right)^2 + (I_n^2 + I_D^2)(R_S - jX_C)^2 + \frac{E_E^2}{1+(\omega R_E C_E)^2} + \left(\frac{E_C}{K'_t}\right)^2.$$

In the expression, we recognise the first part (say from section. 7.3). Last term is also known. The second last term, however, needs some comments. The noise voltage over $R_E$ will not be $E_E$ for higher frequencies, because $C_E$ will "attempt to short-circuit" this. To find the expression we first model the thermal noise in $R_E$ as a current noise of size $I_E=E_E/R_E$. The noise current over $R_E$ and $C_E$ will be:

$$E'^2_E = I_E^2 \cdot \left(C_E \parallel R_E\right) = \frac{E_E^2}{R_E^2}\left|\frac{R_E}{j\omega R_E C_E + 1}\right|^2 = \frac{E_E^2}{1+\left(\omega R_E C_E\right)^2}$$

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# Common-emitter with one voltage supply

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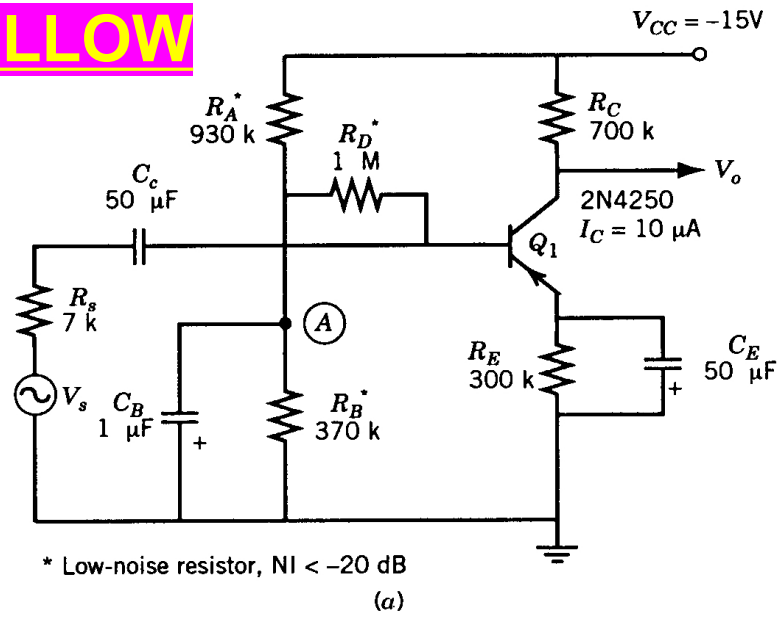
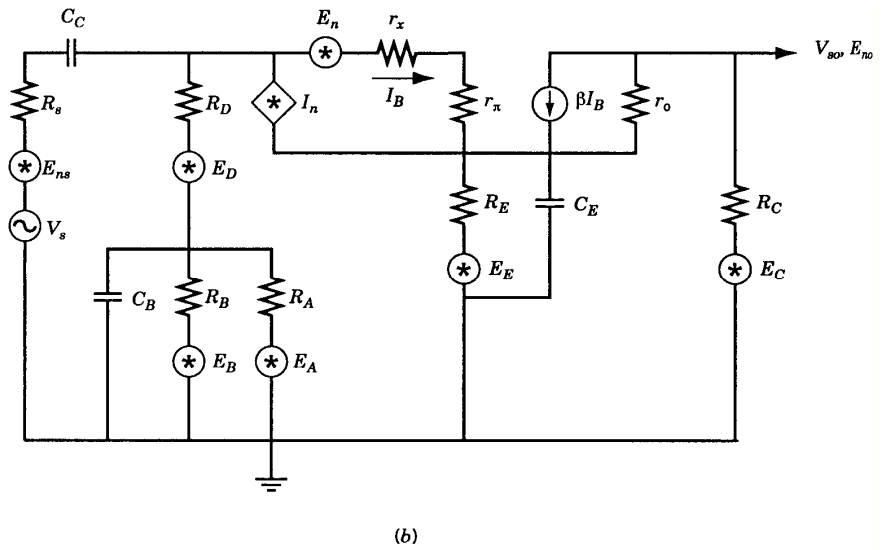
Here a point A is established supplying a stable DC potential for the base. The point A is AC-wise short circuited to ground through $C_B$.

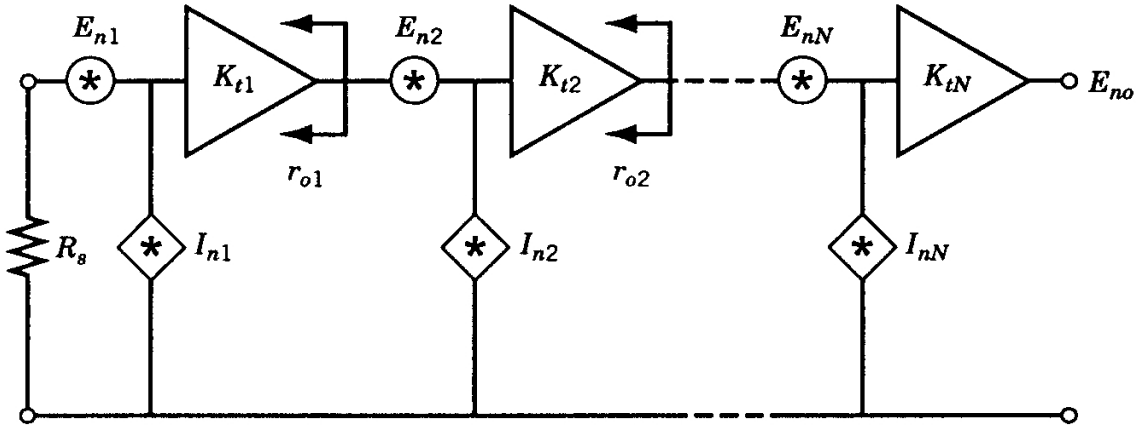



| | 10Hz | 10kHz |
|---|---|---|
| En | 4.5nV | 4.5nV |
| In | 0.3pA | 0.1pA |
| R0 | 10kΩ | 45kΩ |
| NF@R0 | 0.68dB | 0.35dB |
| Kt | 280 | |
| Ri | 780 | |

# Noise in cascaded stages

We have previously studied the noise figure for cascaded amplifiers. We will now look at the equivalent input noise:




The expression for equivalent input noise can be expressed as follows

$$E_{ni}^2 = E_{ns}^2 + E_{n1}^2 + I_{n1}^2 R_S^2 + \frac{E_{n2}^2 + I_{n2}^2 r_{o1}^2}{K_{t1}^2} + \frac{E_{n3}^2 + I_{n3}^2 r_{o2}^2}{K_{t1}^2 K_{t2}^2} + \cdots\cdots$$

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Here $r_{o1}$ is the output resistance of stage 1. Similarly for $r_{o2}$, $r_{o3}$ etc.

$K_{ti}$ is as earlier the voltage gain.

As previously if the gain is large enough in the first stage, noise from subsequent stages can be ignored.