UiO : Department of Informatics
University of Oslo

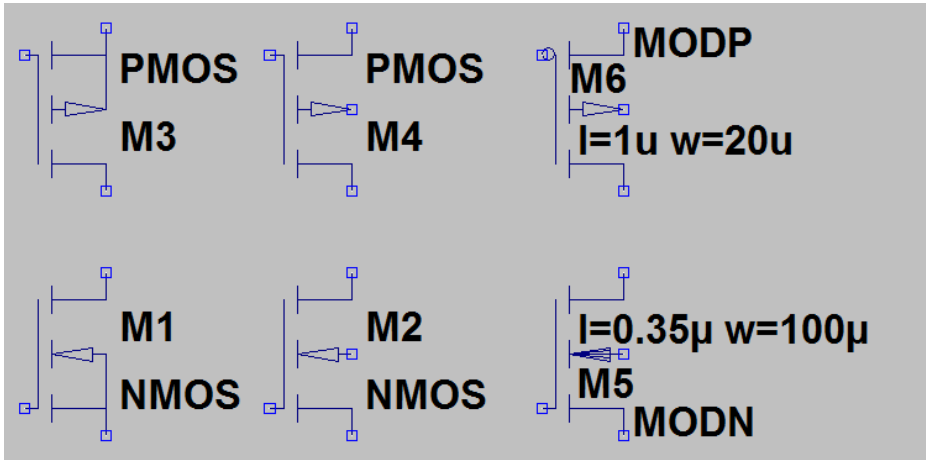
IN5230
Electronic noise – estimates and countermeasures

Lecture no 9 (Mot 6)

Noise in field effect transistors

Two types of field effect transistors:

- MOSFET: Capacitive control of the channel
- JFET: Variation of the width of a reversed biased depletion zone that determines the width of the channel. GaAs FETs have a similar behaviour.

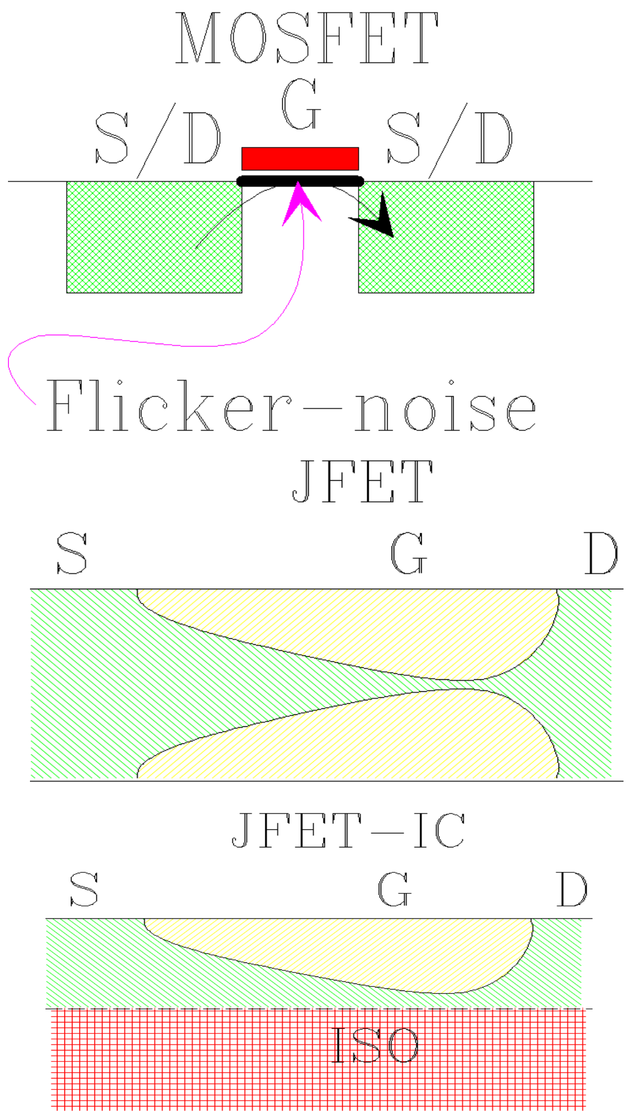


MOS and JFET

RED: All figures and text

FET (Field Effect Transistor) implies that a channel is created/throttled as a result of the voltage on a control terminal. There are essentially two ways to do this:

- MOS: The gate sets up a field that creates a channel on the other side of an insulator
- JFET (Junction FET): The voltage on the gate controls the width of the depletion zone which opens/closes the channel. JFETs are available in two variants
  - Discrete components: the gate is present on both sides of the channel.
  - ASIC: the gate is on one side while it is an insulator on the other side of the channel.



Noise Mechanisms

RED: Figure

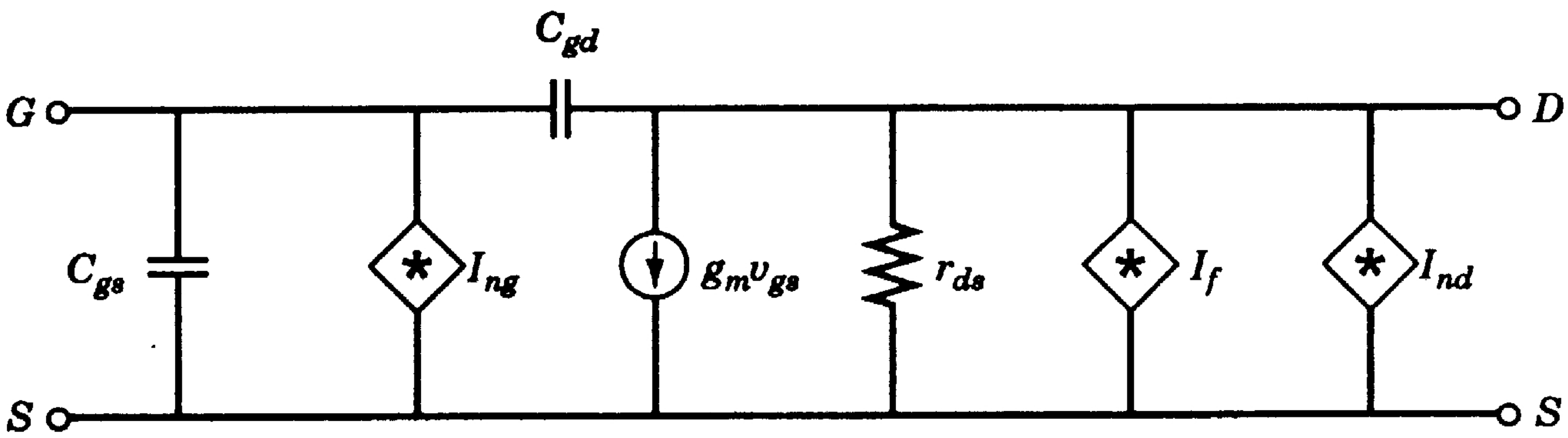


Figure 6-1 Small-signal noise equivalent circuit for a FET.

The figure shows a simple FET-model extended with noise models.

Elements of a typical model:

C_{gs}, C_{gd}: Capacitance between gate and source and between gate and drain.

$g_m V_{gs}$: Current between source and drain.

r_{ds}: Resistance in the channel between drain and source.

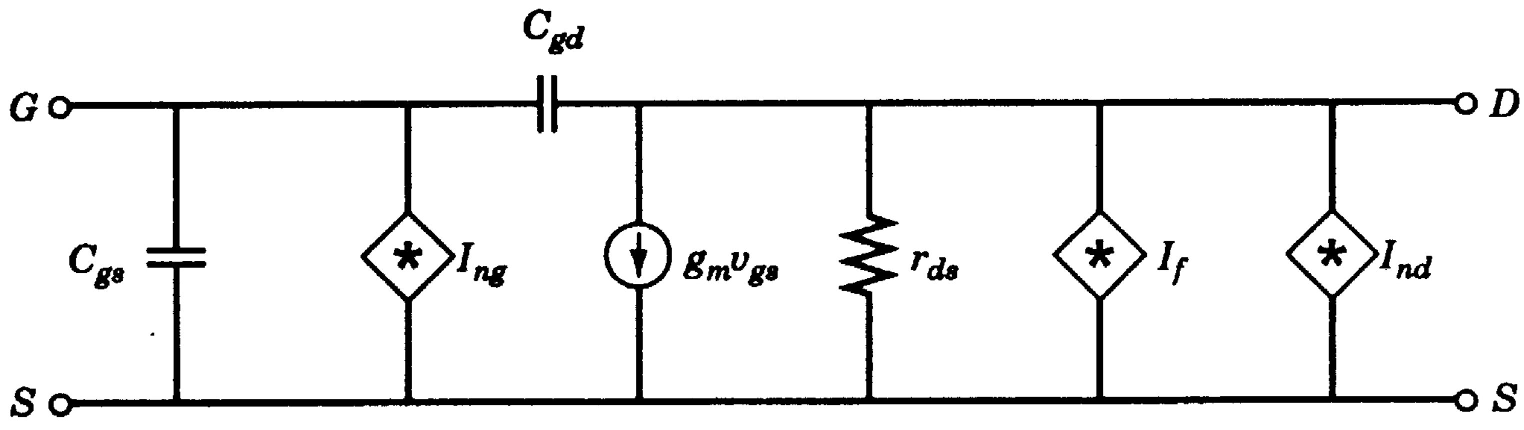


Figure 6-1 Small-signal noise equivalent circuit for a FET.

Noise models:

Gate:

- Shot-Noise in leakage current through the gate (especially JFET and newer small linewidth CMOS) and
- thermal fluctuations from the drain node, which affects the gate node

Drain:

- I_{nd}: Thermal noise in the channel.
- I_f: Flicker noise in the channel

The gate and I_{nd} thermal noises are both due to thermal noise in the channel and they are partially correlated at higher frequencies.

En-In representation of noise

RED: Figure

The figure show the typical trends for *En* and *In* in a FET. *En* is flat at high frequencies but grows at lower frequencies due to flicker noise. *In* is flat at low frequencies but grows linearly with frequency above a corner frequency.

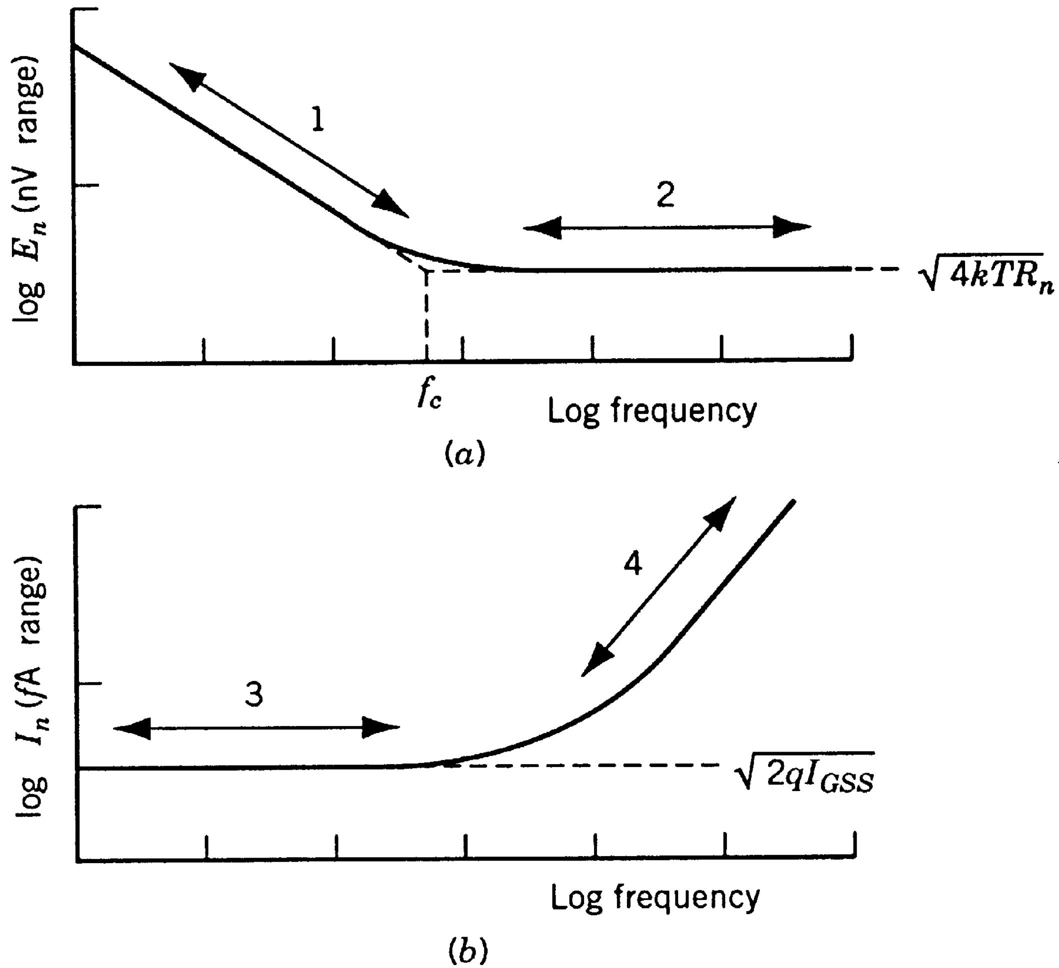


Figure 6-2 Typical noise behavior of a FET.

Simple FET model

RED: Figure

First, we ignore the noise and consider a standard MOSFET.

The transistor can be in cut-off, linear region or in saturation. In the linear region the current *Ids* has a strong dependence on *Vds*, while in saturation the dependence is weaker. The linear range is often named the resistive or ohmic region.

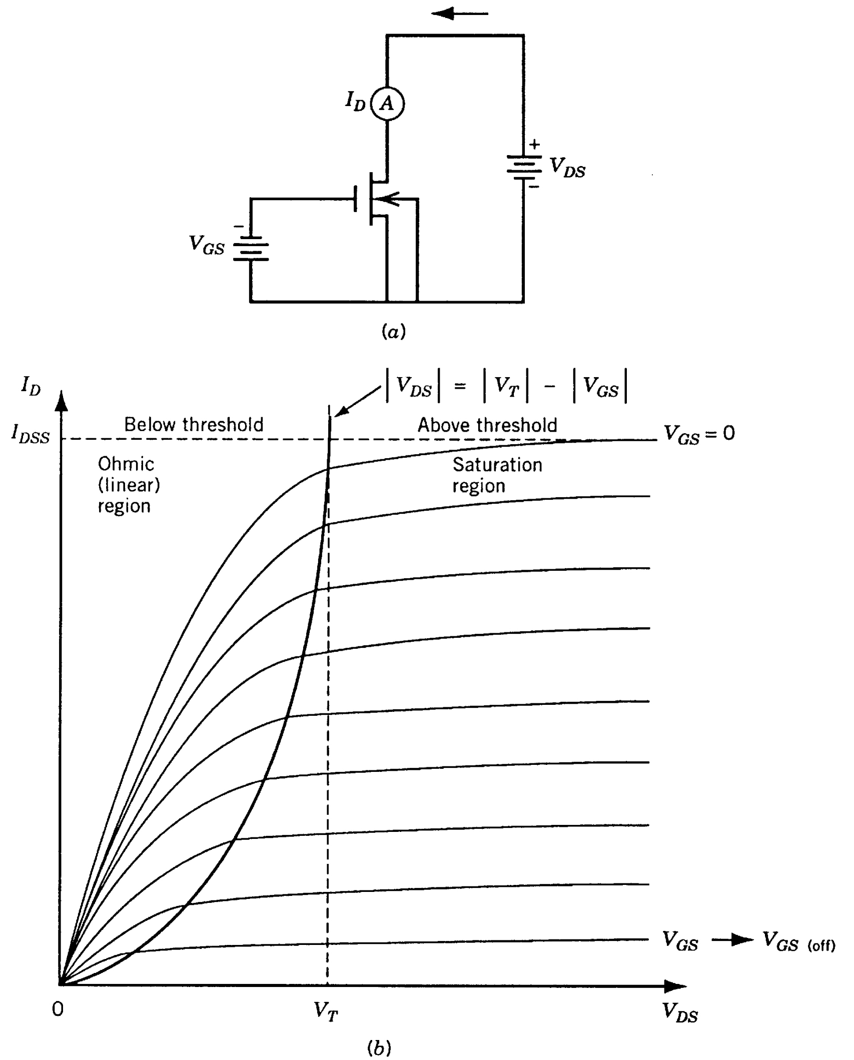


Figure 6-7 Determination of *n*-channel MOSFET *V–I* characteristics: (*a*) test circuit and (*b*) output characteristics.

In saturation *Ids* can be expressed as follows:

$$I_D = K_p\left(\frac{W}{L}\right)(V_{GS} - V_T)^2(1 + \lambda V_{DS})$$

Here λ modulates the dependence on the channel length, V_T is the threshold voltage, W is the channel width, while L is the channel length. The transconductance value K_P can be expressed as:

$$K_p = \frac{\mu_0 C_{ox}}{2}$$

Here is μ_0 the mobility of the channel and Cox the capacitance over the gate oxide.

Some examples of sizes from the book:

	N-channel	p-channel	Denomination
K_P	41.8	15.5	$\mu A/V^2$
V_T	0.79	-0.93	V
λ	0.01	0.01	1/V

Key parameters are transconductance ...

$$g_m = \left.\frac{\partial I_D}{\partial V_{GS}}\right|_{Q-point} = 2K_p\left(\frac{W}{L}\right)(V_{GS}-V_T)(1+\lambda V_{DS}) = \frac{2I_D}{V_{GS}-V_T}$$

.. and output conductance ...

$$g_{ds} = \frac{\partial I_D}{\partial V_{DS}} = \left.\frac{1}{r_{ds}}\right|_{Q-point} = \lambda K_p\left(\frac{W}{L}\right)(V_{GS}-V_T)^2(1+\lambda V_{DS}) = \lambda I_D$$

The capacitances Cgd and Cgs.

These capacitances will vary depending on the region:

	Region		
	Cut-off	Linear	Saturation
Cgd	$C_{OX}WL_D$	$C_{OX}WL_D$ + (1/2) WLC_{OX}	$C_{OX}WL_D$
Cgs	$C_{OX}WL_D$	$C_{OX}WL_D$ + (1/2) WLC_{OX}	$C_{OX}WL_D$ + (2/3) WLC_{OX}

Cox may be defined as:

$$C_{ox} = \frac{\varepsilon_0 \varepsilon_{SiO_2}}{t_{ox}}$$

... and stated i fF/um ²

Ind in short length devices

The thermal noise in the channel can be expressed as:

$$I_{nd}^2 = \frac{8kTg_m}{3}$$

However in newer technologies with smaller transistor lengths it is a little more complicated and more correct will be:

$$I_{nd}^2 = 4kT\gamma g_m$$

where γ is 2/3 for long L and increasing for short L. An example measurement shows γ=2.5 for L=0.25µm.

When Vds=0 the expression is $I_{nd}^2 = 4kT\gamma g_{ds}$ NB! *g_{ds}!*
where $g_{ds} = 1/R_{on}$ for short L and $g_{ds} = g_m$ for long L in saturation.

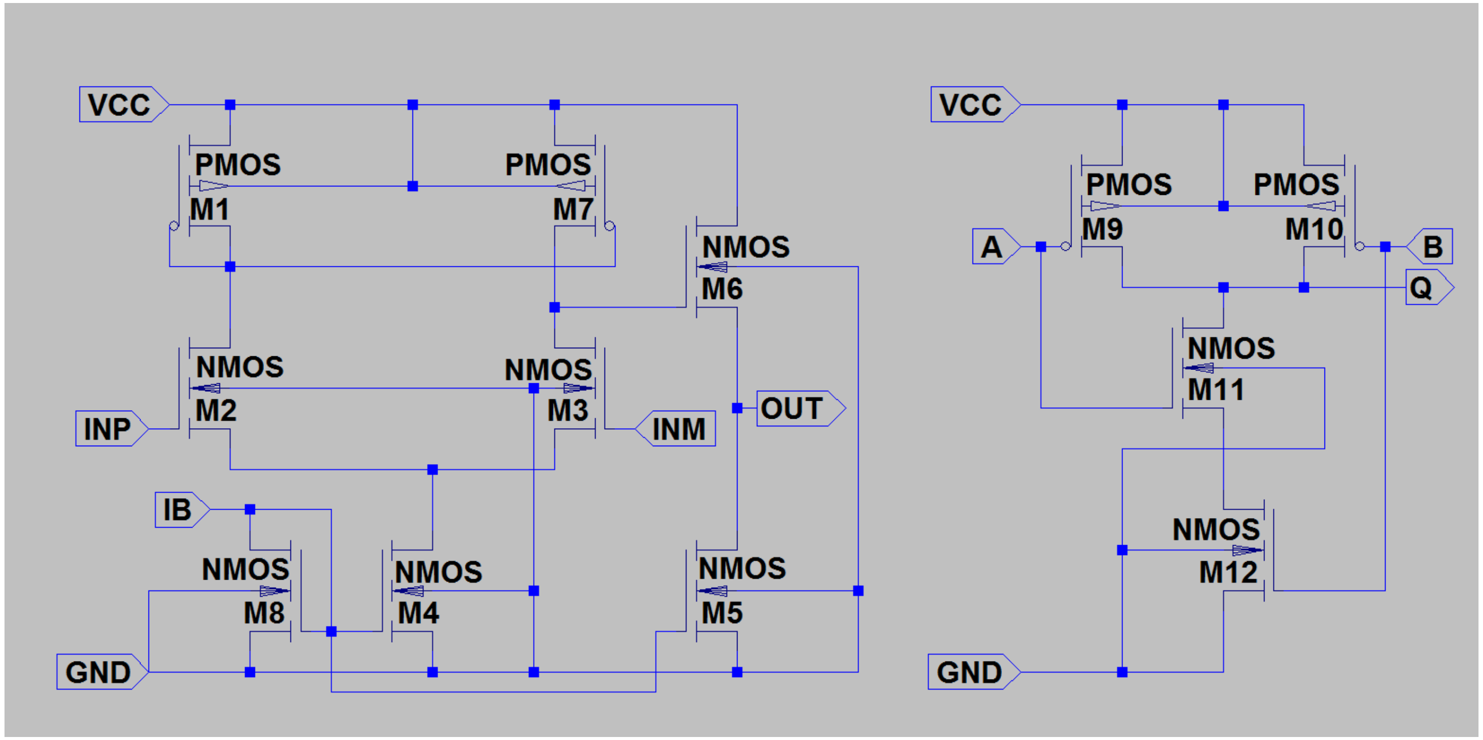
Ref: Razavi *Design of Analog CMOS Integrated Circuits*

MOS noise sources

- Thermal noise in channel
- Flicker noise in channel
- Shot-noise in leakage channel-gate
- Coupled thermal noise at gate
- Thermal noise in gate
- Thermal noise in bulk
- Thermal noise in source
- Thermal noise in drain
- Shot-noise drain-bulk
- Shot-noise source-bulk
- (Coupling noise to bulk)

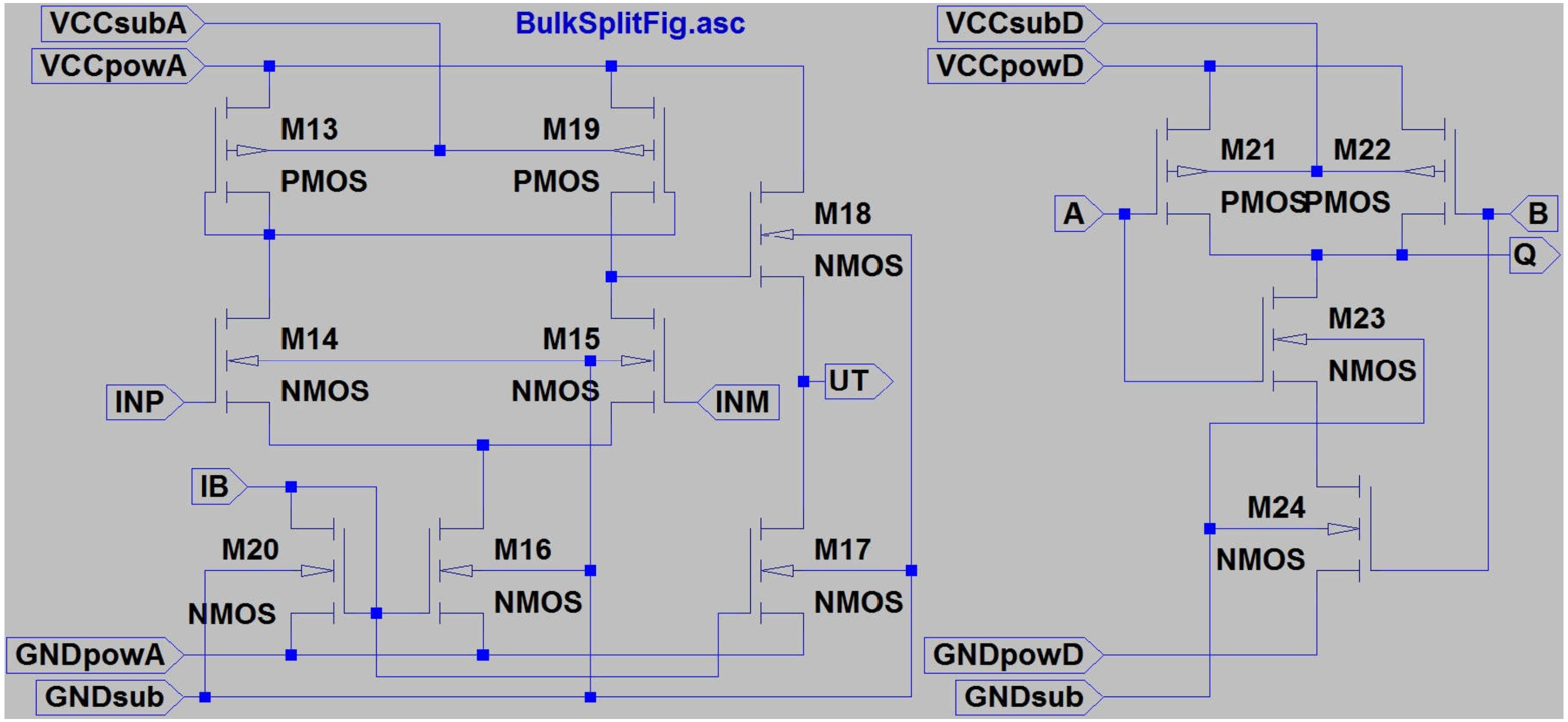
CMOS Standard bulk connection

- The schematics shows an amplifier and a digital NAND gate with standard sub connections.
- NMOS bulk terminals are connected to the lowest potential, while PMOS bulk are connected to the highest.



CMOS low noise bulk connection

- For low noise the NMOS bulk and PMOS bulk are split from the power lines.



- Little current will pass through the bulk terminal. However the transistor is sensitive to noise on this terminal.
- By splitting the power wires we reduce the noise on the sensitive bulk terminal. This will prevent digital source/drain noise to reach the analog bulk terminal.