UiO : Department of Informatics
University of Oslo

IN5230
Electronic noise –
Estimates and countermeasures

Lecture X (Razavi 7)

Noise – Razavi – Chapter 7

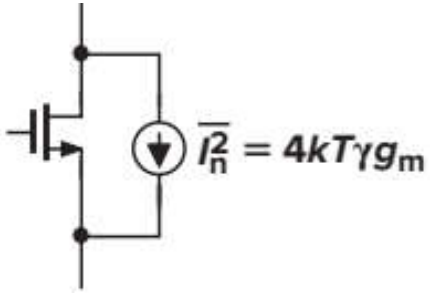
MOSFET Thermal Noise(29)

- MOS transistors exhibit thermal noise with the most significant source being the noise generated in the channel
- For long-channel MOS devices operating in saturation, the channel noise can be modelled by a current source connected between the drain and source terminals with a spectral density

$$\overline{I_n^2} = 4kT\gamma g_m$$

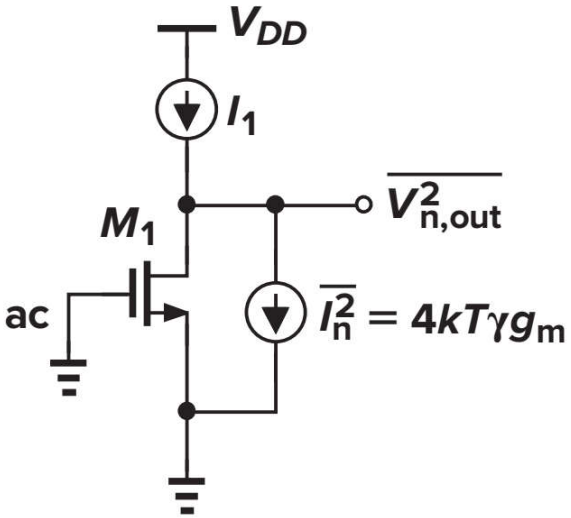
Red: Equation

- The coefficient 'γ' (Not body effect coefficient!) is derived to be 2/3 for long-channel transistors and is higher for submicron MOSFETs
- As a rule of thumb, Razavi assume γ=1



Red: Figure

MOSFET Thermal: Example

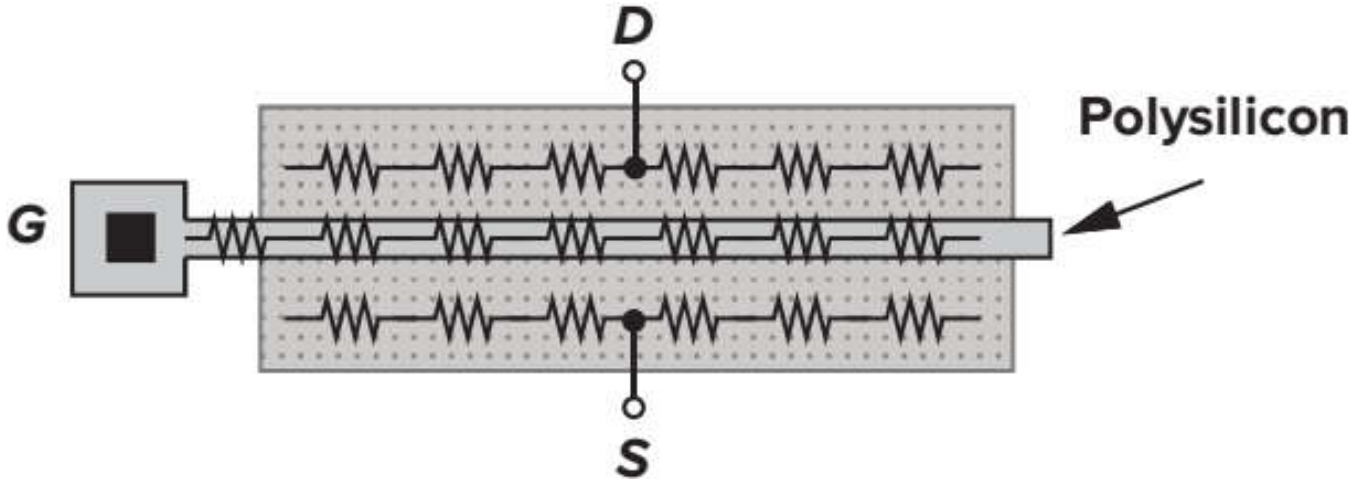


- The maximum output noise occurs if the transistor sees only its own output impedance as the load, i.e., if the external load is an ideal current source
- Output noise voltage spectrum is given by (7.29,7.30)

$$S_{out}(f) = S_{in}(f)|H(f)|^2$$

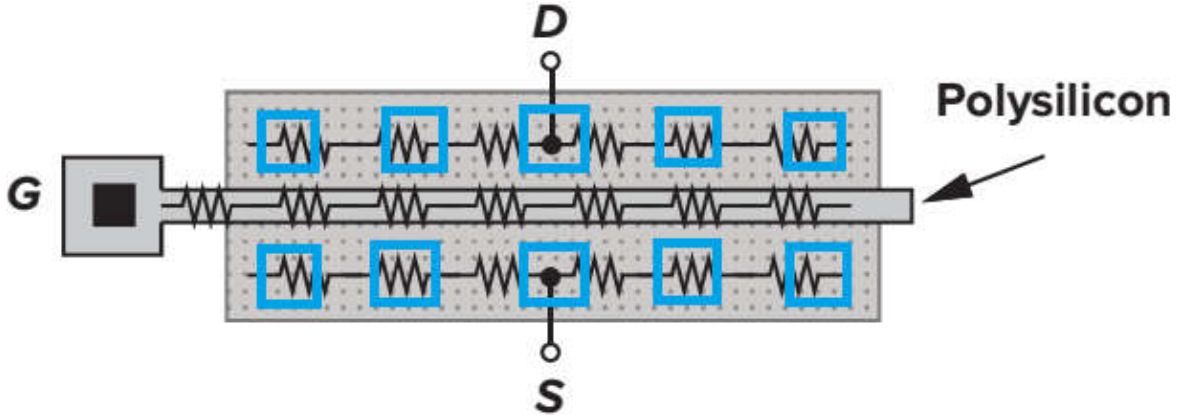
$$\overline{V_n^2} = \overline{I_n^2} r_O^2 = (4kT\gamma g_m) r_O^2$$

MOSFET Thermal Noise

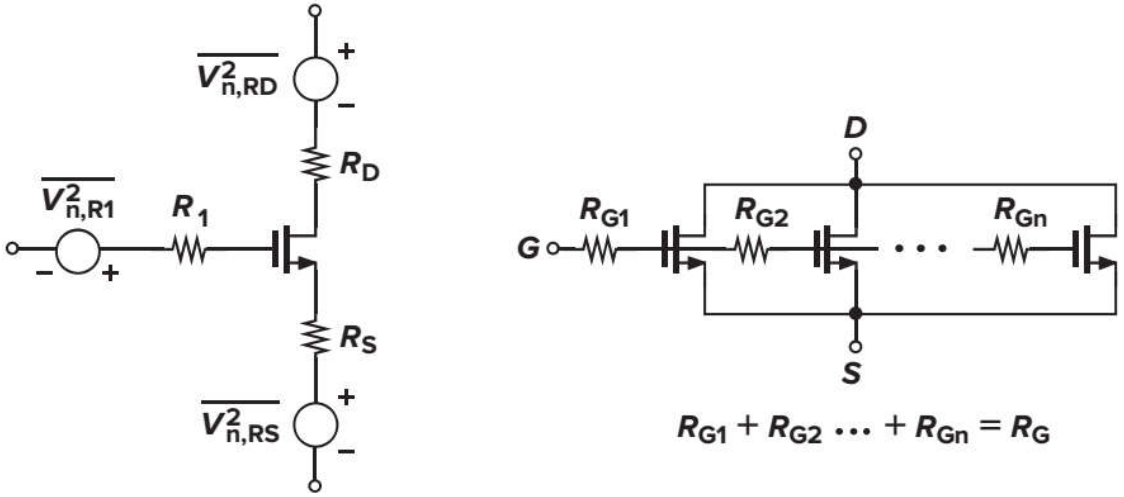


- Ohmic sections of a MOSFET have a finite resistivity and exhibit thermal noise
- For a wide transistor, source and drain resistance is negligible whereas the gate distributed resistance may become noticeable.

□ = contact



MOSFET Thermal Noise

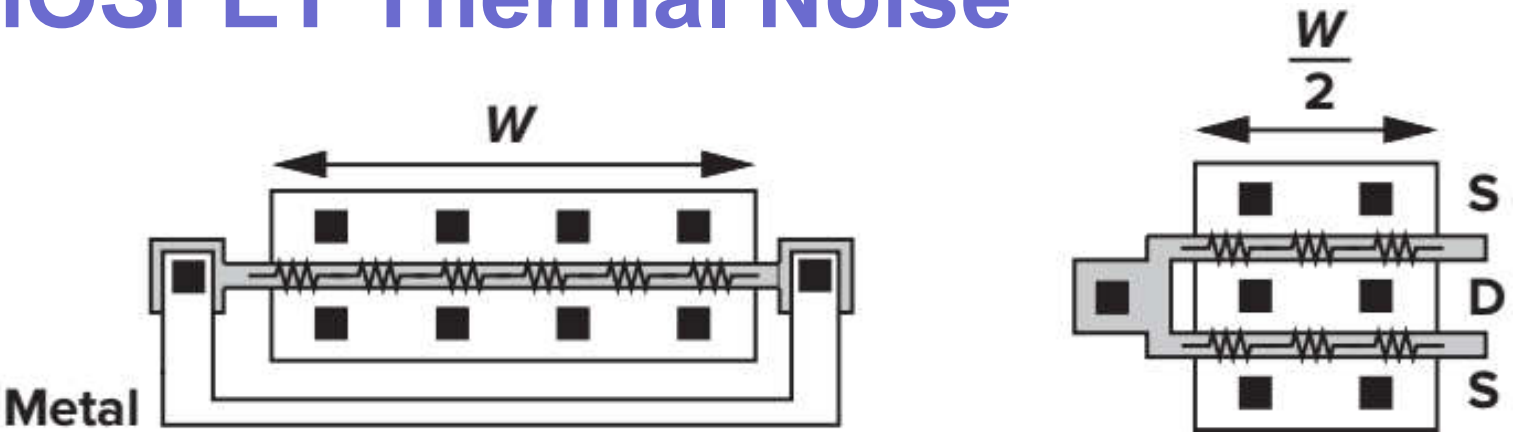


- In the noise model (left fig), the lumped resistance R_1 represents the distributed gate resistance
- In the distributed structure of the right figure, unit transistors near the left end see the noise of only a fraction of R_G whereas those near the right end see the noise of most of R_G

Red: Equation

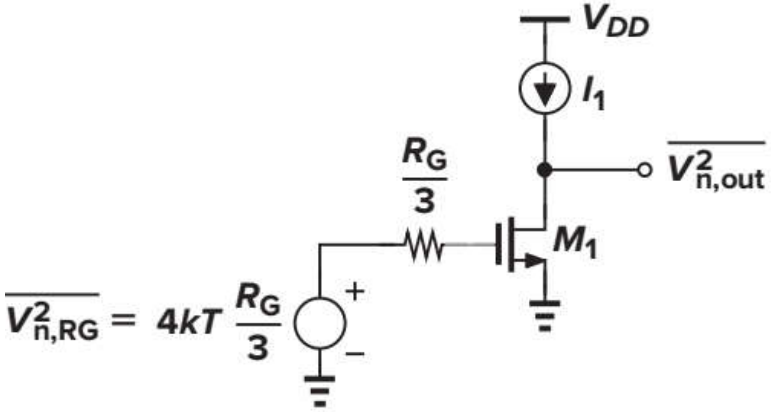
- It can be proven that $R_1 = R_G/3$ and hence the noise generated by gate resistance is $\overline{V^2_{nRG}} = 4kT\,R_G/3$

MOSFET Thermal Noise



- Effect of R_G can be reduced by proper layout
- In left fig, the two ends of the gate are shorted by a metal line, reducing the distributed resistance from R_G to $R_G/4$
- Alternatively, the transistor can be folded as in the right figure so that each gate “finger” exhibits a resistance of $R_G/4$ for composite transistor

MOSFET Thermal Noise: Example



- If the total distributed gate resistance is R_G, the output noise voltage due to R_G is given by (7.32)

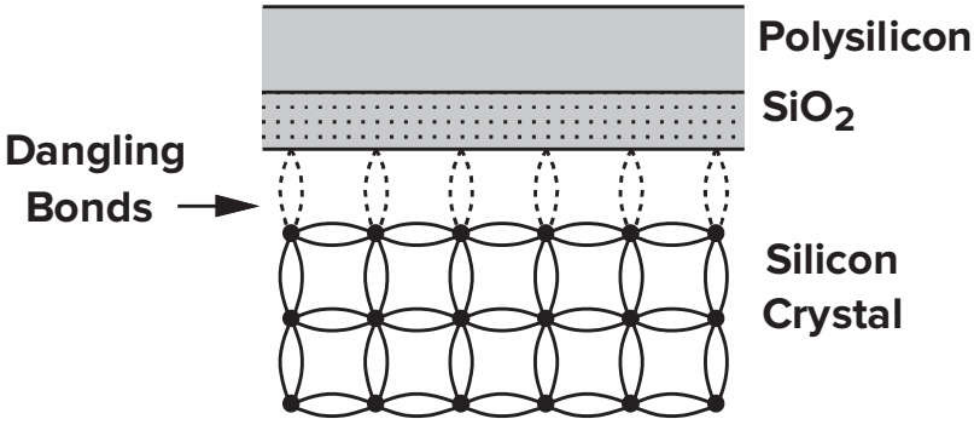
$$\overline{V_{n,out}^2} = 4kT \frac{R_G}{3} (g_m r_O)^2$$

- For the gate resistance noise to be negligible, we must ensure (7.33)

$$\frac{R_G}{3} \ll \frac{\gamma}{g_m}$$

Yellow: Equation

Flicker Noise(36)



Yellow: Figure

- At the interface between the gate oxide and silicon substrate, many “dangling” bonds appear, giving rise to extra energy states
- Charge carriers moving at the interface are randomly trapped and later released by such energy states, introducing “flicker” noise in the drain current
- Other mechanisms in addition are believed to generate flicker noise

Flicker Noise

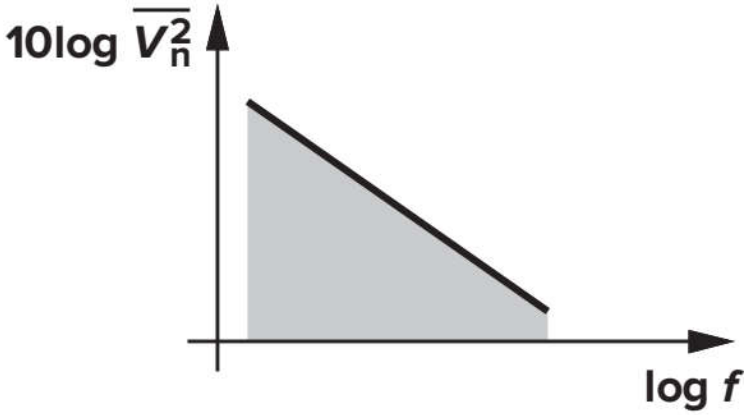
- Average power of flicker noise cannot be predicted easily
- It varies depending on cleanness of oxide-silicon interface and from one CMOS technology to another
- Flicker noise is more easily modelled as a voltage source in series with the gate and in saturation region, is roughly given by

$$\overline{V_n^2} = \frac{K}{C_{ox} W L} \cdot \frac{1}{f}$$

Red: Equation

- K is a process-dependent constant on the order of 10E-25V²F

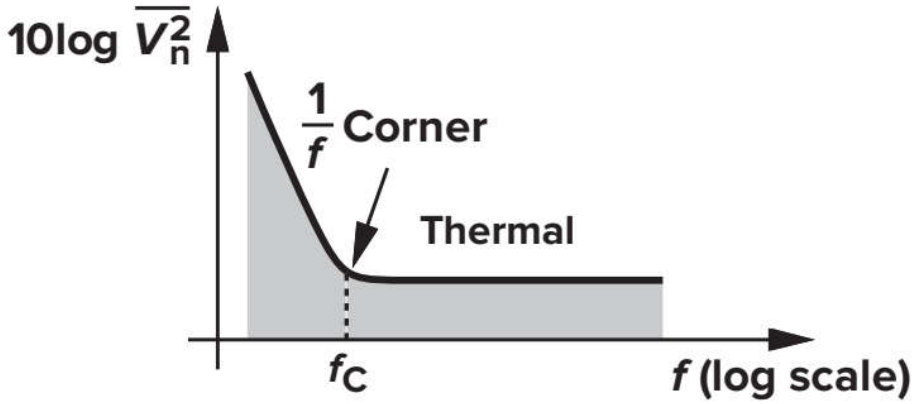
Flicker Noise



- The noise spectral density is inversely proportional to frequency
  - Trap and release phenomenon occurs at low frequencies more often
- Flicker noise is also called “1/f” noise
- To reduce 1/f noise, device area must be increased
- Generally, PMOS devices exhibit less 1/f noise than NMOS transistors
  - Holes are carried in a “buried” channel, at some distance from the oxide-silicon interface

Flicker Noise Corner Frequency

- At low frequencies, the flicker noise power approaches infinity
- At very slow rates, flicker noise becomes indistinguishable from thermal drift or aging of devices
  - Noise component below the lowest frequency in the signal of interest does not corrupt it significantly
- Intersection point of thermal noise and flicker noise spectral densities is called “corner frequency” fc



Yellow: Figure

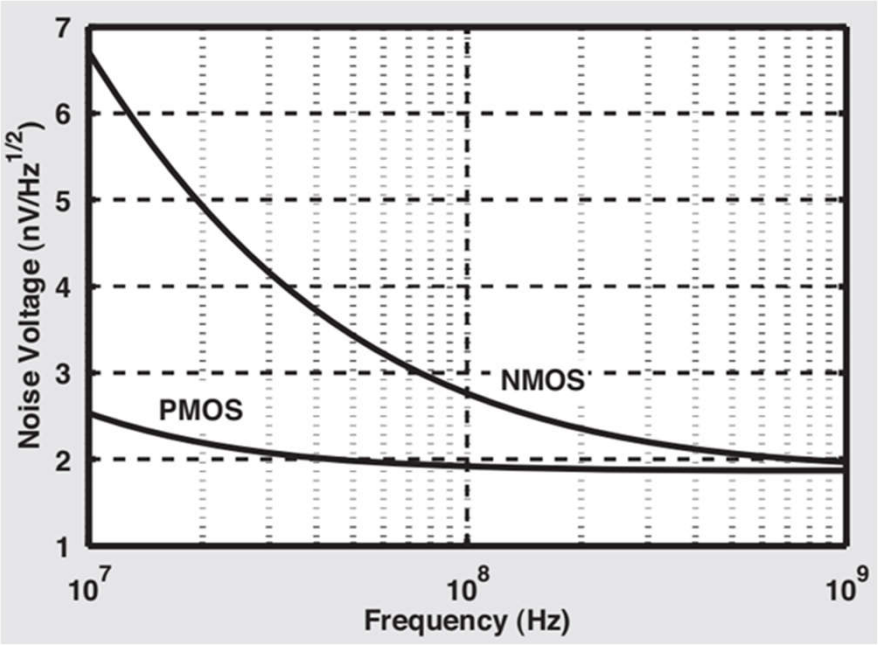
Nanometer Design Notes

- W/L = 5μm/40nm,
- ID = 250μA

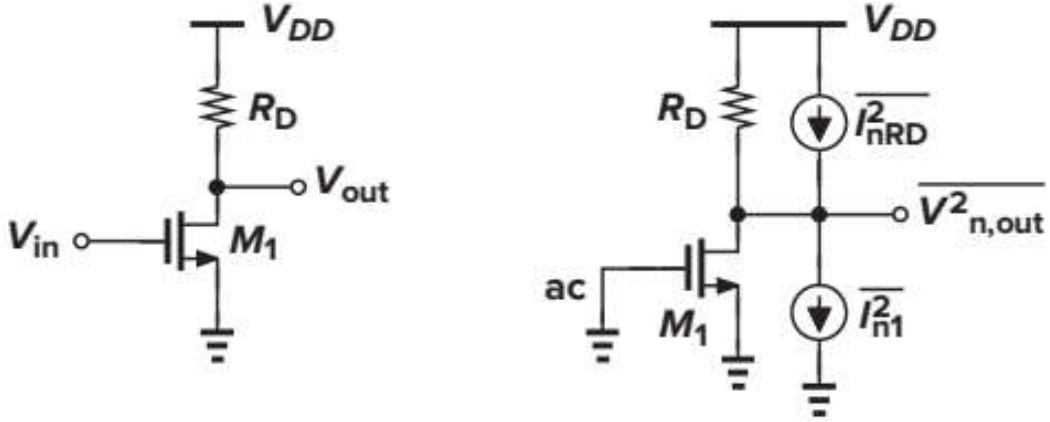
- Low frequencies: Flicker noise
- High frequencies: Thermal noise

- ⇒ PMOS exhibit less noise than NMOS (and PNP less than NPN)
- ⇒NMOS noise corner at several hundred MHz

Yellow: Figure



Input-Referred Noise: Example 3/9



- For the simple CS stage, the input-referred noise voltage is given by (7.45,7.46,7.47)

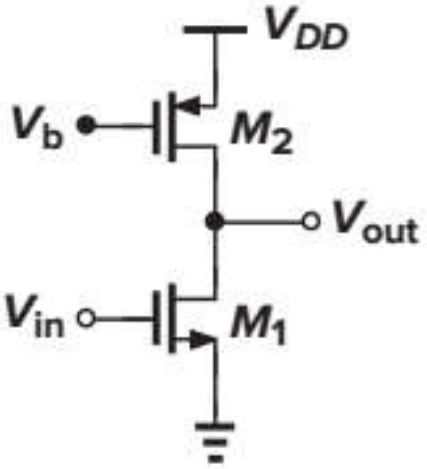
$$\overline{V_{n,in}^2} = \frac{\overline{V_{n,out}^2}}{A_v^2}$$

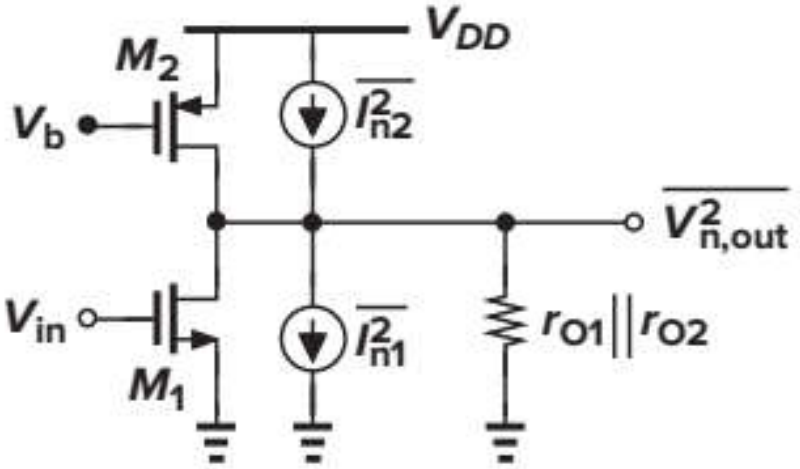
$$= \left(4kT\gamma g_m + \frac{K}{C_{ox}WL}\cdot\frac{1}{f}\cdot g_m^2 + \frac{4kT}{R_D}\right) R_D^2 \frac{1}{g_m^2 R_D^2}$$

$$= 4kT\frac{\gamma}{g_m} + \frac{K}{C_{ox}WL}\cdot\frac{1}{f} + \frac{4kT}{g_m^2 R_D}$$

- First and third terms combined can be viewed as thermal noise of an equivalent resistance R_T, so that the equivalent input-referred thermal noise is $4kTR_T$

Common-Source Stage: Example 3/4



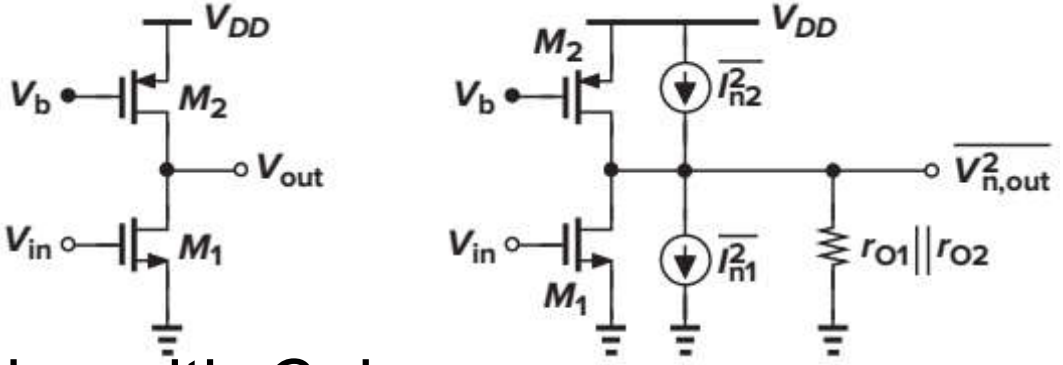


- Since the voltage gain is equal to $g_{m1}(r_{O1} \| r_{O2})$, total noise voltage referred to the gate of *M1* is (7.77,7.78)

$$\overline{V_{n,in}^2} = 4kT(\gamma g_{m1} + \gamma g_{m2})\frac{1}{g_{m1}^2} = 4kT\gamma\left(\frac{1}{g_{m1}} + \frac{g_{m2}}{g_{m1}^2}\right)$$

- Thus, g_{m2} must be minimized because *M2* serves as a current source rather than a transconductor

Common-Source Stage: Example 4/4



- Total output noise with C_L is (7.79,7.80)

$$\overline{V_{n,out,tot}^2} = \int_0^\infty 4kT\gamma(g_{m1}+g_{m2})(r_{O1}\|r_{O2})^2 \frac{df}{1+(r_{O1}\|r_{O2})^2 C_L^2 (2\pi f)^2}$$

$$\overline{V_{n,out,tot}^2} = \gamma(g_{m1}+g_{m2})(r_{O1}\|r_{O2})\frac{kT}{C_L}$$

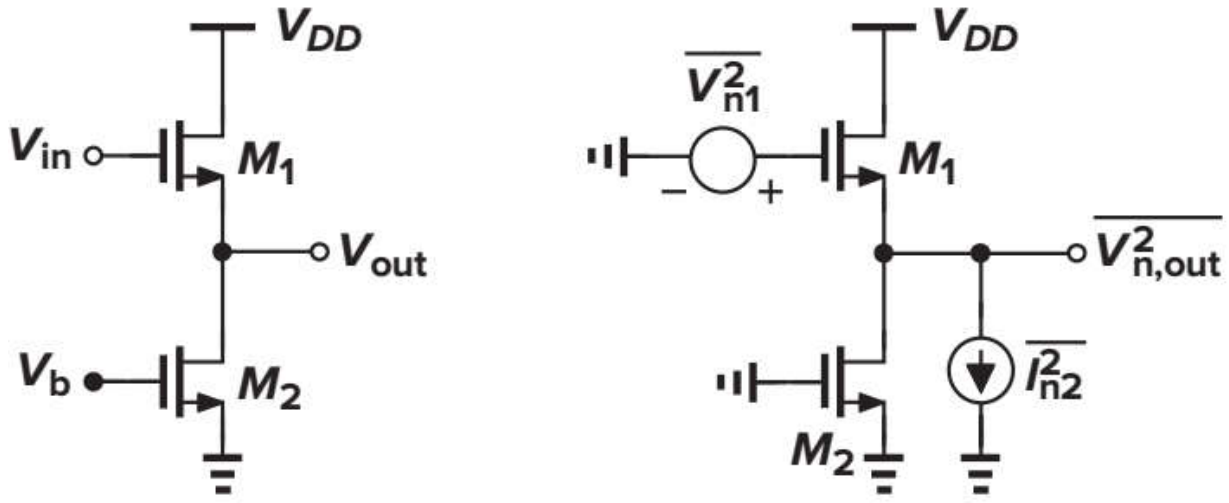
- A low-frequency input sinusoid of amplitude Vm yields an output amplitude equal to $g_{m1}(r_{O1}\|r_{O2})V_m$ with an output SNR of (7.81,7.82)

$$\text{SNR}_{out} = \left[\frac{g_{m1}(r_{O1}\|r_{O2})V_m}{\sqrt{2}}\right]^2 \cdot \frac{1}{\gamma(g_{m1}+g_{m2})(r_{O1}\|r_{O2})(kT/C_L)}$$

$$= \frac{C_L}{2\gamma kT} \cdot \frac{g_{m1}^2(r_{O1}\|r_{O2})}{g_{m1}+g_{m2}} V_m^2$$

Yellow: Equation

Source Followers: Thermal Noise 2/2



- The voltage gain is

$$A_v = \frac{\dfrac{1}{g_{mb1}} \Big\| r_{O1} \| r_{O2}}{\dfrac{1}{g_{mb1}} \Big\| r_{O1} \| r_{O2} + \dfrac{1}{g_{m1}}}$$

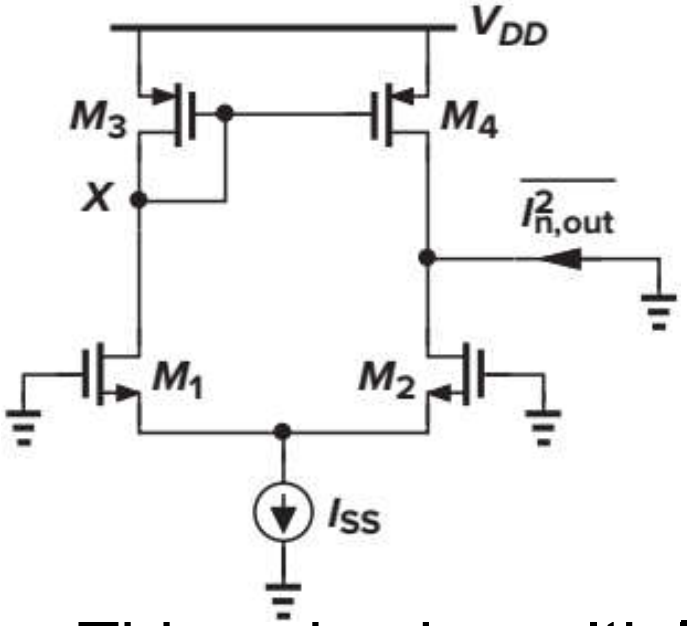
- Total input-referred noise voltage is (7.110,7.111)

$$\overline{V_{n,in}^2} = \overline{V_{n1}^2} + \frac{\overline{V_{n,out}^2}\Big|_{M2}}{A_v^2} = 4kT\gamma\left(\frac{1}{g_{m1}} + \frac{g_{m2}}{g_{m1}^2}\right)$$

Yellow: Equation

- Source followers add noise to the input signal and provide a voltage gain less than unity

Noise in five-transistor OTA



- The noise current of M_3 primarily circulates through the diode-connected impedance $1/g_{m3}$, producing a voltage at the gate of M_4 with spectral density $4kT\gamma/g_{m3}$

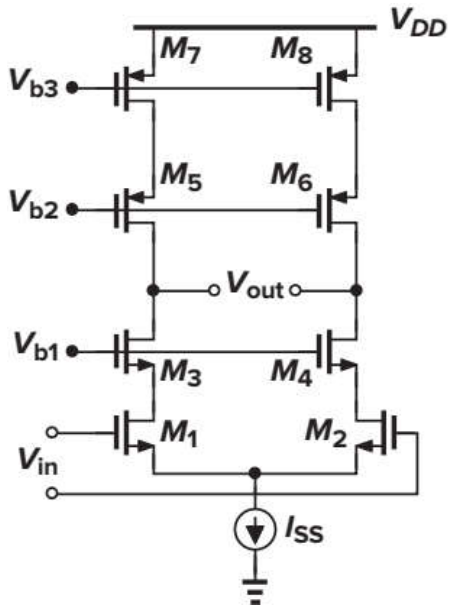
- This noise is multiplied by g_{m4}^2 as it emerges from the drain of M_4; the noise current of M_4 also flows directly through the output short-circuit thus (7.141) $\overline{I_{n,out}^2} = 4kT\gamma(2g_{m1,2} + 2g_{m3,4})$
- Multiplying this noise by $R_{out}^2 \approx (r_{O1,2} || r_{O3,4})^2$ and dividing the result by $A_v^2 = G_m^2 R_{out}^2$ the total input-referred noise is

$$\overline{V_{n,in}^2} = 8kT\gamma\left(\frac{1}{g_{m1,2}} + \frac{g_{m3,4}}{g_{m1,2}^2}\right)$$

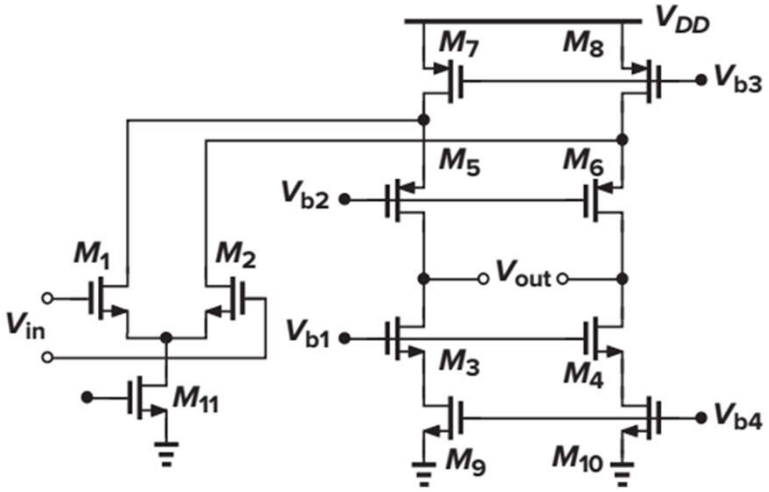
Yellow: Equation

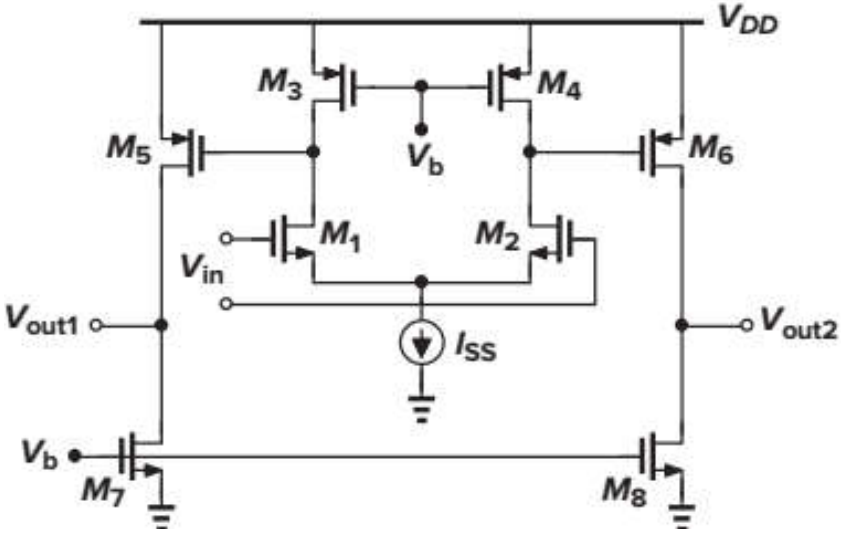
Noise in Op Amps 9.12

- How to analyse for noise in more complex amplifier structures?
- ⇒ Find which gate voltages that influence most on the output!
- ⇒ Analyse manually or by simulation!



- Upper right: Telescopic
- Lower left: Folded cascode
- Lower right: Two-stage opamp



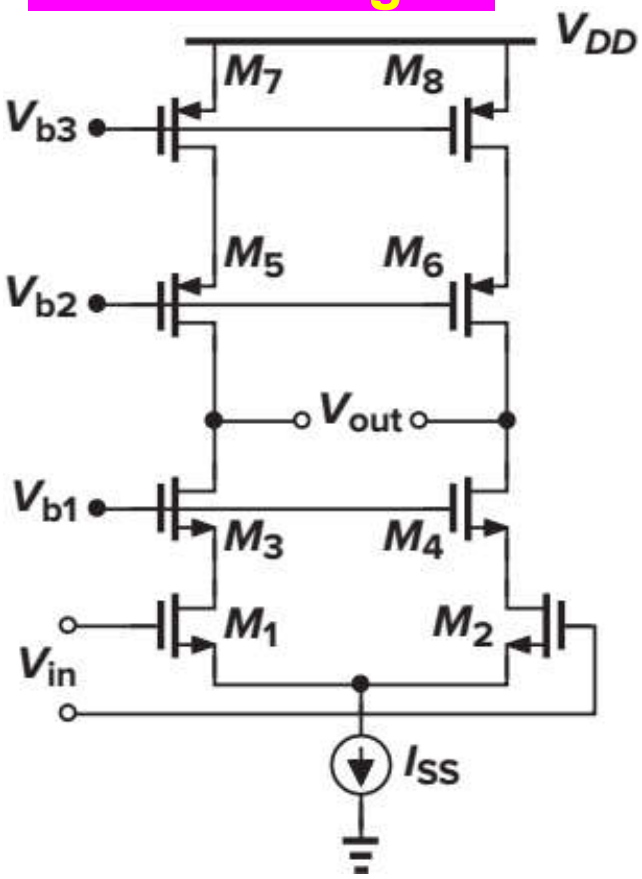


YELLOW: Figure

Noise in Op Amps 9.12

Telescopic

- M7-M8 give a coarse regulation of current while M5-M6 gives fine tuning i.e. M7-M8 has larger influence
- M1-M2 is the signal inputs, obviously more sensitive than M3-M4.
- $\Rightarrow$ M1-M2 and M7-M8 are the most noise sensitive.



- Resulting expression below:

$$\overline{V_n^2} = 4kT\left(2\frac{\gamma}{g_{m1,2}} + 2\frac{\gamma g_{m7,8}}{g_{m1,2}^2}\right) + 2\frac{K_N}{(WL)_{1,2}C_{ox}f} + 2\frac{K_P}{(WL)_{7,8}C_{ox}f}\frac{g_{m7,8}^2}{g_{m1,2}^2}$$

Noise in Op Amps 9.12

Folded-cascode

- The gate voltage of M1-M2, M7-M8, M9-M10 will give the largest influence on the output and are hence most noise sensitive. (We test by making a small step on M7 and keep the others fixed etc.)
- We calculate (thermal) noise from M7-M8 and M9-M10 to output.

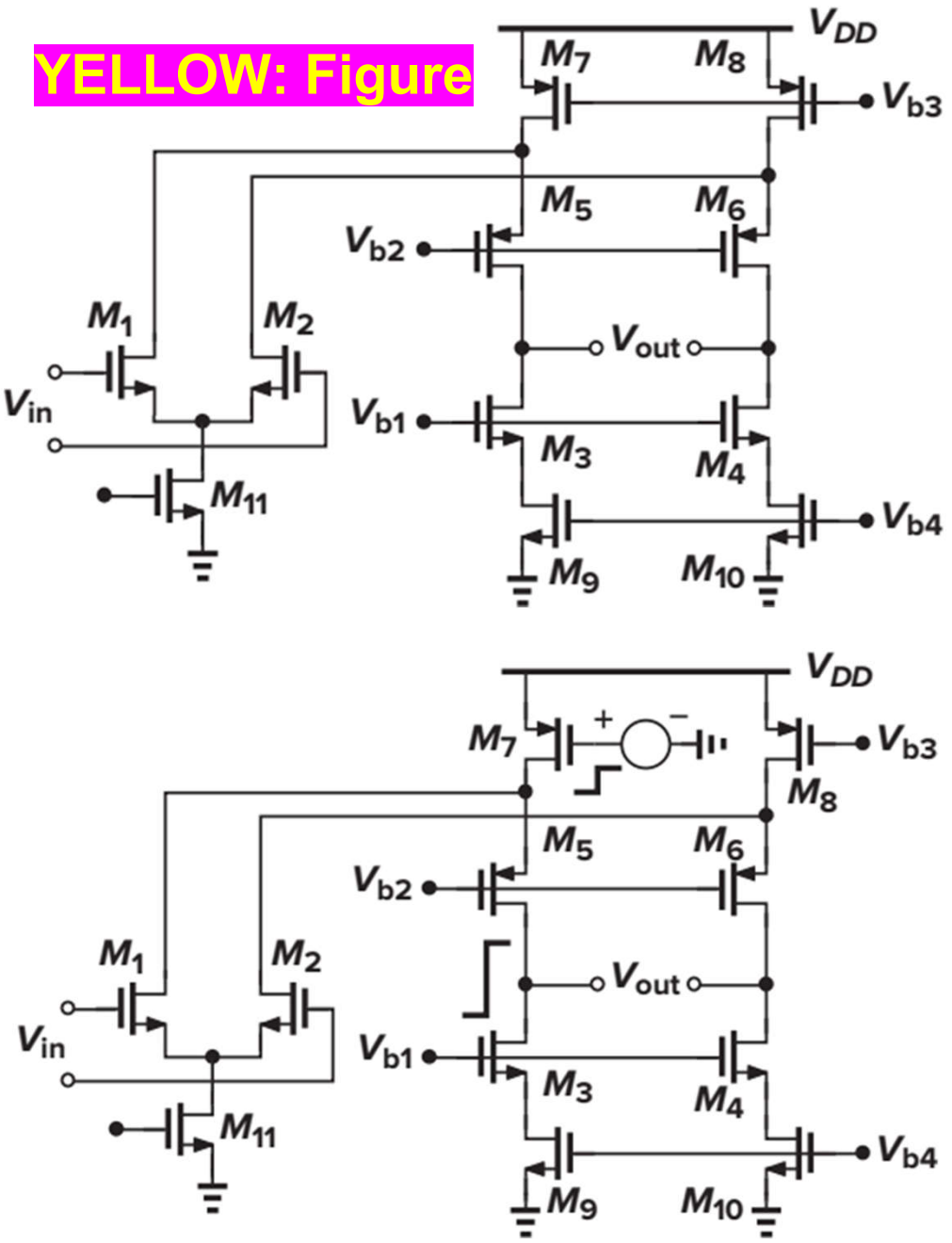
$$\overline{V_{n,out}^2}\big|_{M7,8} = 2\left(4kT\frac{\gamma}{g_{m7,8}}g_{m7,8}^2 R_{out}^2\right)$$

$$\overline{V_{n,out}^2}\big|_{M9,10} = 2\left(4kT\frac{\gamma}{g_{m9,10}}g_{m9,10}^2 R_{out}^2\right)$$

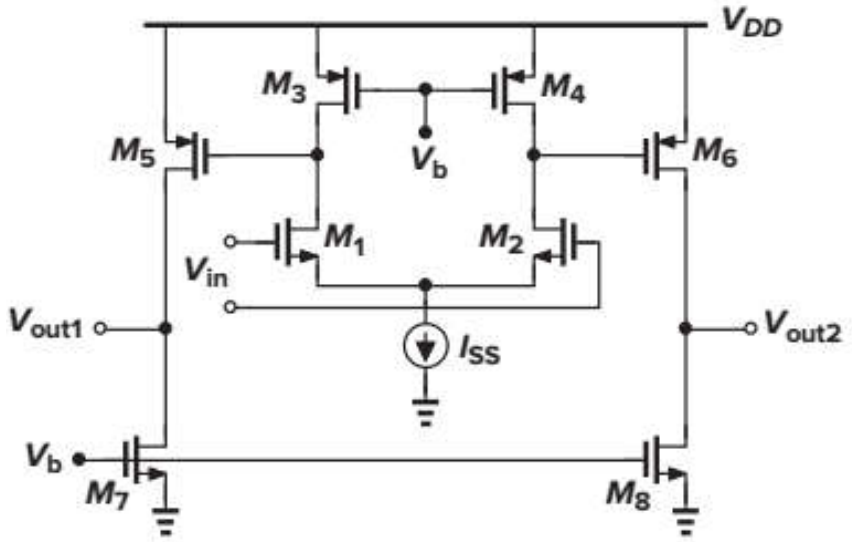
- Then we add M1-M2 contribution and calculate back to the input Vin

$$\overline{V_{n,int}^2} = 8kT\left(\frac{\gamma}{g_{m1,2}} + \gamma\frac{g_{m7,8}}{g_{m1,2}^2} + \gamma\frac{g_{m9,10}}{g_{m1,2}^2}\right)$$

YELLOW: Figure



Noise in Op Amps 9.12



Two-stage opamp

- Gain to Vout1:

$$g_{m1}(r_{O1} \| r_{O3}) \times g_{m5}(r_{O5} \| r_{O7})$$

- Noise from M5-M8 on input

YELLOW: Figure

$$\overline{V_n^2}\big|_{M5-8} = 2 \times 4kT\gamma(g_{m5}+g_{m7})(r_{O5} \| r_{O7})^2 \frac{1}{g_{m1}^2(r_{O1} \| r_{O3})^2 g_{m5}^2(r_{O5} \| r_{O7})^2} = 8kT\gamma \frac{g_{m5}+g_{m7}}{g_{m1}^2 g_{m5}^2(r_{O1} \| r_{O3})^2}$$

- Noise from M1-M4 on input

$$\overline{V_n^2}\big|_{M1-4} = 2 \times 4kT\gamma \frac{g_{m1}+g_{m3}}{g_{m1}^2}$$

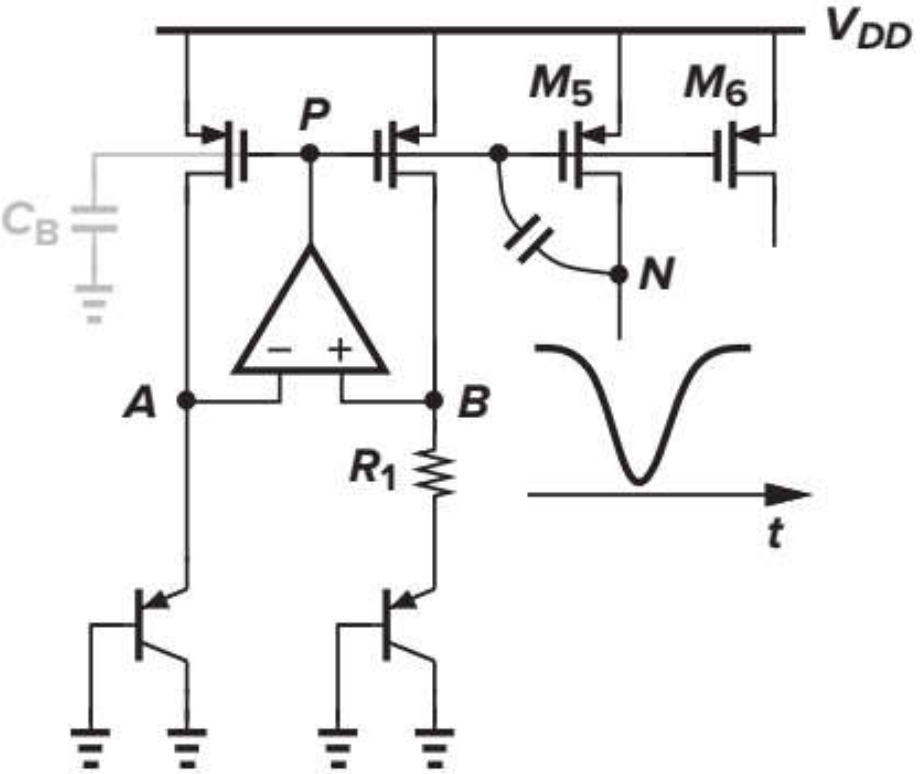
YELLOW: Equation

- Total noise on input

$$\overline{V_{n,tot}^2} = 8kT\gamma \frac{1}{g_{m1}^2}\left[g_{m1}+g_{m3}+\frac{g_{m5}+g_{m7}}{g_{m5}^2(r_{O1} \| r_{O3})^2}\right]$$

Bandgap - Speed and Noise Issues 12.6

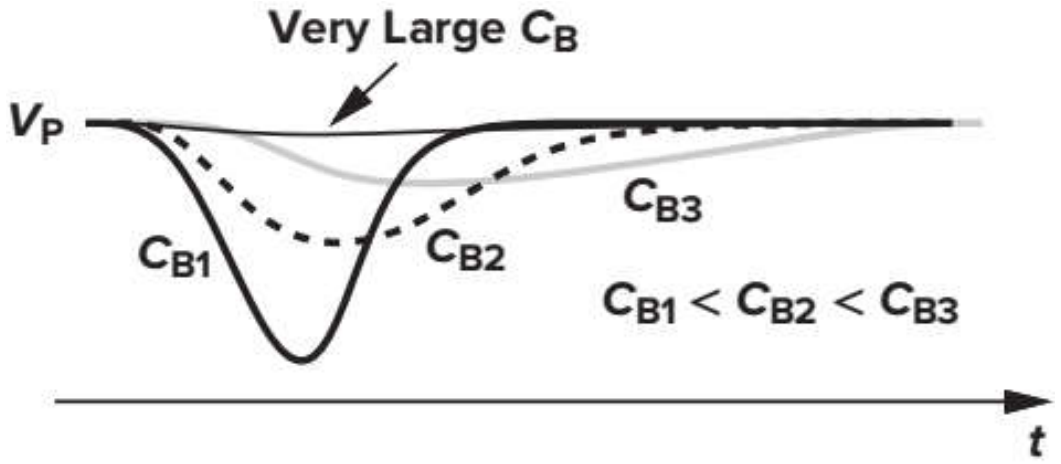
- The bandgap reference generates a stable voltage on P independent of temperature variations. This is used to generate stable currents on M5, M6 etc.
- An unwanted voltage spike on N may be transferred to P and further on to M6 and other parts using the reference.
- In a low power implementation the amplifier will be slow and this makes it less resistant towards noise



YELLOW: Figure

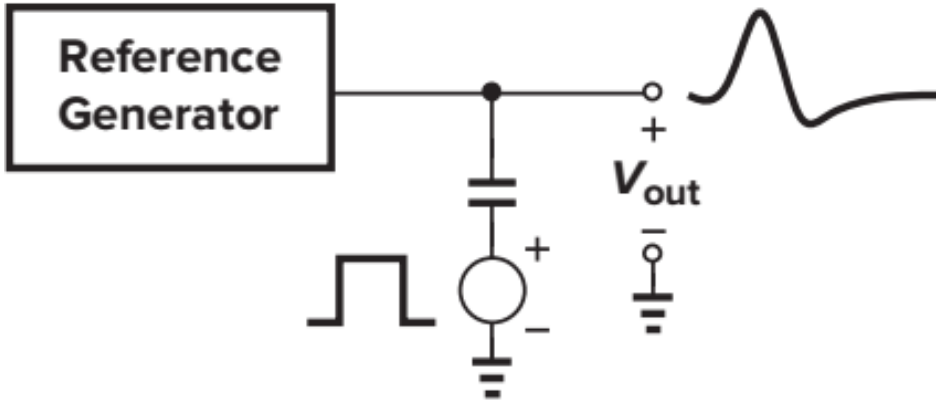
Bandgap - Speed and Noise Issues 12.6

- Using a faster amplifier will reduce the noise but increase the power consumption
- An alternative is to add a capacitor C_B in node P. A large C_B reduces the noise spike but makes it last for a longer time. It also increases the time before the circuit is settled after power on. This is a disadvantage in particular when the reference is normally off and only turned on when it should be used.



Bandgap - Speed and Noise Issues 12.6

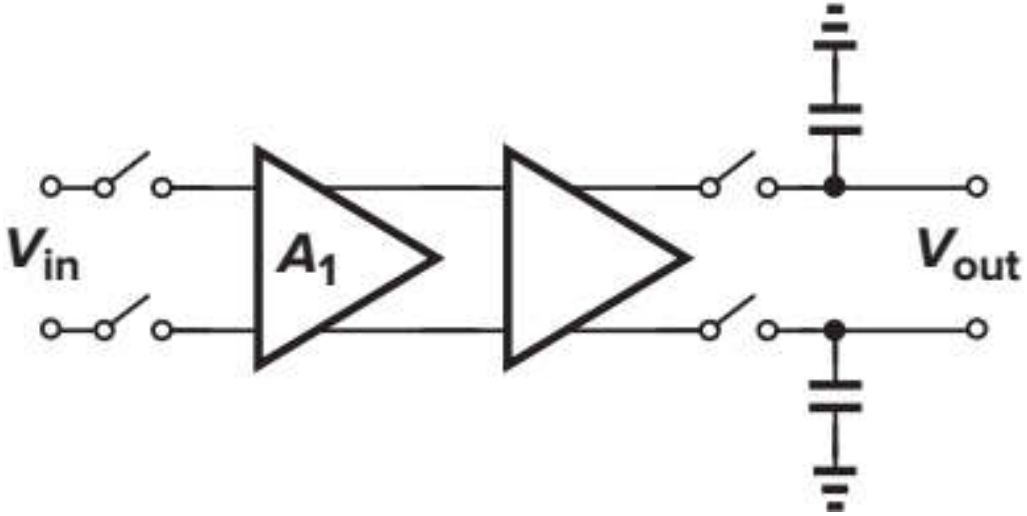
- Whether a fast amplifier or large capacitance (or a combination) should be used will depend on the application.
- The noise resistivity towards this type of noise can be modelled by adding a voltage pulse on a capacitor connected to the generated reference voltage.



RED: Figure

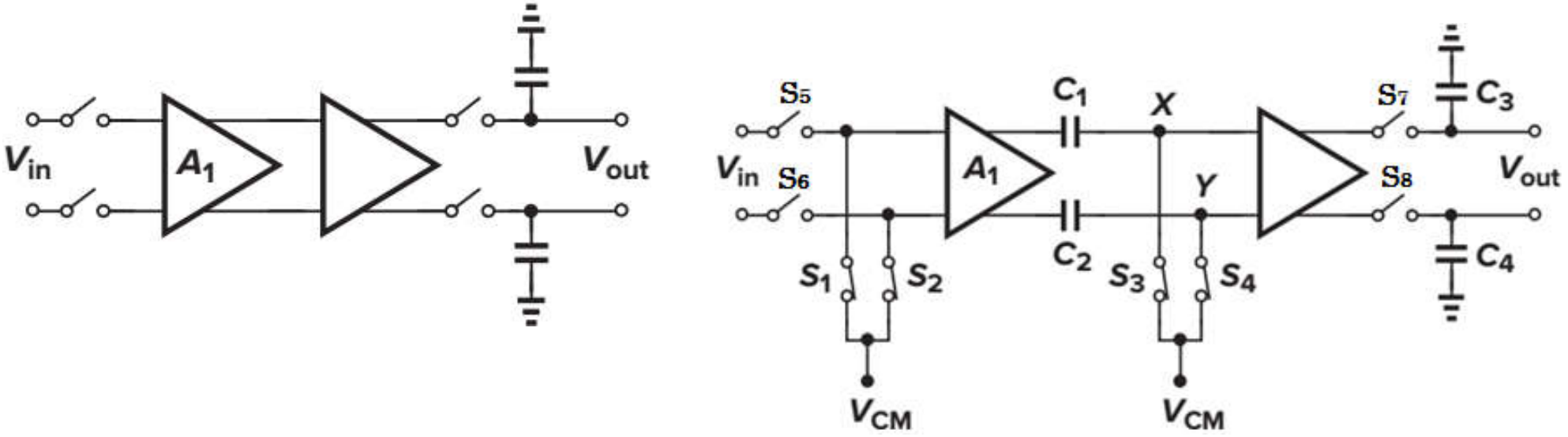
Reduction of Noise by Offset Cancellation 14.2.3

- DC-offset ≈ low frequency
- Periodic cancellation?



- Problem: Noise of A1 corrupts V_{in}

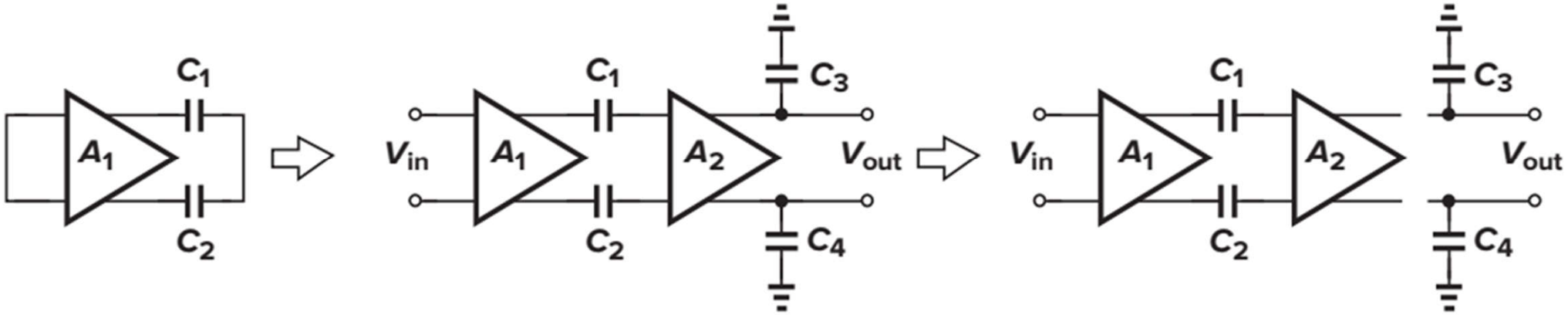
Reduction of Noise by Offset Cancellation 14.2.3



- Offset cancellation before every sampling
- CDS: Correlated Double Sampling
  - (Leads to aliasing of wideband noise)

Reduction of Noise by Offset Cancellation 14.2.3

YELLOW: Figure



1. S1-S4 closed, S5-S8 open: Offset of A_1 stored on C_1 and C_2
2. S1-S4 open, S5-S8 closed: Input sets C_3 and C_4
3. (S1-S6 closed, S5-S6 open), S7-S8 open: C_3 and C_4 keeps sampled value

Reduction of Noise by Offset Cancellation 14.2.3

- $\Delta t = t_2 - t_1 = 10$ ns
- Offset/noise under $1/\Delta t$ is supressed
- Sinus maximum slew rate: $2\pi fA$, maximum voltage change: $\Delta V = 2\pi fA\Delta t$.
- 1MHz: $\Delta V_1/A = 6.3\%$
- 10MHz: $\Delta V_1/A = 63\%$
- Low frequency has not time to change