UiO : Department of Informatics
University of Oslo

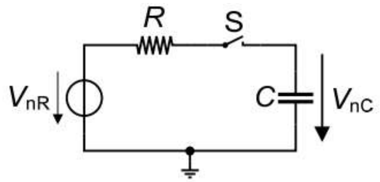
IN5230
Electronic noise –
Estimates and countermeasures

Lecture Z

Sampling, Switches, Auto Zero (AZ) and Chopper Stabilization (CS)

Equivalent bandwidth of sampled white noise

Equivalent Bandwidth of Sampled White Noise



Noise on C with switch S closed (continuous-time)

- Noise voltage PSD across C

$$S_{V_{nC}} = \frac{2kTR}{1+(f/f_c)^2} \text{ with } f_c = \frac{1}{2\pi RC}$$

- Equivalent noise bandwidth

$$B_n = \frac{\pi}{2} f_c$$

- Noise power

$$V_{nC}^2 = S_{V_{nC}}(0) \cdot 2B_n = 2kTR \cdot \pi f_c = \frac{kT}{C}$$

Noise sampled on C

- Noise voltage PSD on C

$$S_{V_{nC}}(f) = sinc^2(\pi f T_s) \cdot \pi f_c T_s \cdot 2kTR$$

- Equivalent noise bandwidth

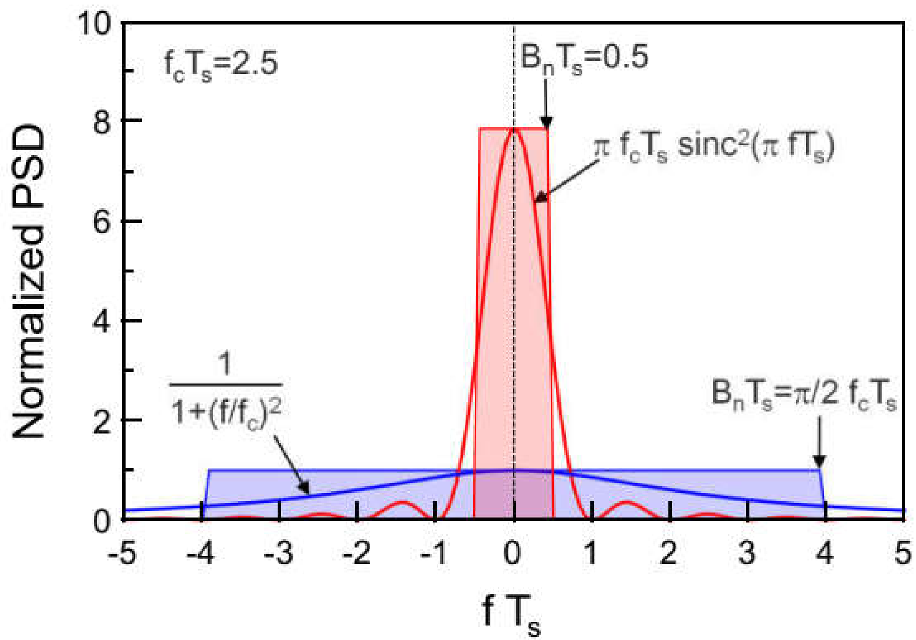
$$B_n = \frac{1}{2S_{V_{nC}}(0)} \cdot \int_{-\infty}^{+\infty} S_{V_{nC}}(f) \cdot df$$

$$= \int_{0}^{+\infty} sinc^2(\pi f T_s) \cdot df = \frac{f_s}{2}$$

- Noise power

$$V_{nC}^2 = S_{V_{nC}}(0) \cdot 2B_n = \pi f_c T_s \cdot 2kTR \cdot \frac{f_s}{2} = \frac{kT}{C}$$

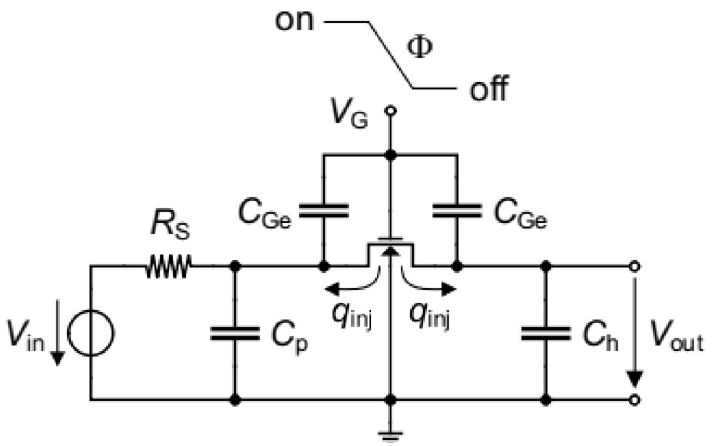
The total noise power (corresponding to the shaded area) remains constant but is transposed from high-frequency down to the baseband (Nyquist band)



Introduction

- **Low-frequency noise** is the **main noise contributor** to analog circuits operating at low frequency (typically below 1 MHz) such as sensor interfaces
- The **flicker noise** being inversely proportional to the gate area, it **can be reduced** at the cost of area and power increase, but it **cannot be eliminated** by this mean
- On the other hand, flicker noise can be almost eliminated and offset strongly reduced using proper **circuit techniques**
- There are mainly two approaches:
  - **Autozero (AZ)** or **correlated double sampling (CDS)**, which are **sampling** techniques
  - **Chopper stabilization (CS)**, which is a **modulation** technique
- Although these techniques look similar they have **very different properties** in terms of residual noise
- Both techniques are extensively using switches which have some nonidealities that will be examined first

Nonideal Effects in Switches



- clock feedthrough,
- channel charge injection
- sampled noise and
- leakage current.

$$\Delta V = \alpha \cdot \frac{C_{Ge}}{C_{Ge} + C_h} \cdot V_{swing} + \frac{q_{inj}}{C_h} + \sqrt{\frac{kT}{C_h}} + \frac{I_{leak} \cdot T_h}{C_h}$$

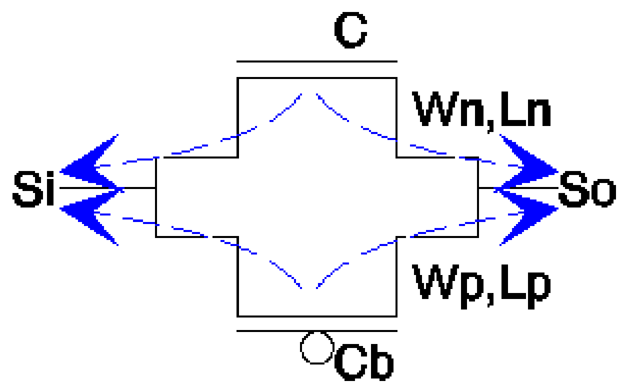
- BSIM3 and BSIM4 does not model correct
- All contributions decrease if a larger hold capacitor is used, but cost power.

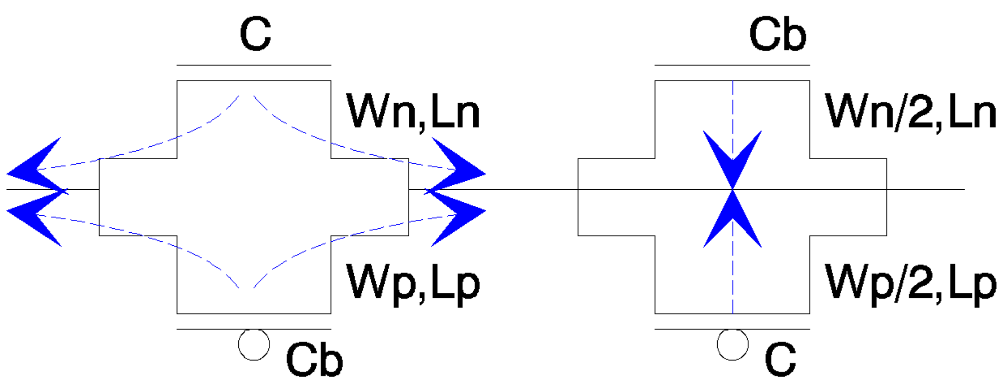
Techniques to Reduce Charge Injection

- The simplest technique uses **complementary switches** in such a way that the charges released by one switch are absorbed by the complementary device building its channel. This technique is rather inefficient, since the matching between the channel charges of the n-MOS and the p-MOS devices is poor and signal dependent. This charge mismatch is further degraded by phase jitter between the two complementary clocks
- Other more efficient strategies are described below
- It should be noted that **none of the techniques** described below offers a **perfect charge-injection cancellation**
- The efficiency of the **half-sized dummy transistor** technique depends on a proper layout in order to insure a good matching and a first-order insensitivity to doping gradient
- The technique which usually offers the best results is a **combination** of a fully **differential structure** and the **half-sized dummy transistor** technique

CMOS switch charge injection

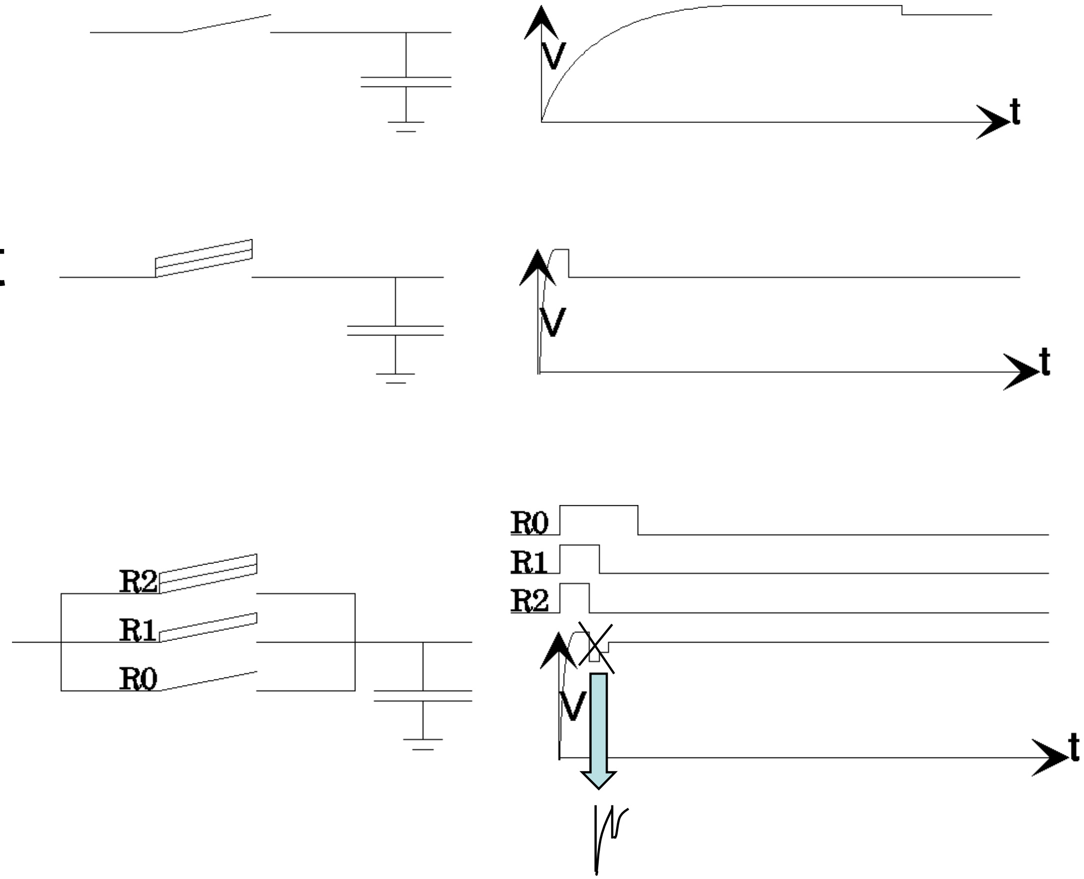
- A conducting CMOS transistor keeps some charge in the channel
- When turned off this charge is released through the source/drain and generates an (unpredictable) voltage change
- A proposal is to add a pair of half-sized "opposite" dummy transistors. However this solution requires impedance symmetry.





CMOS switch charge injection

- The injected charge is a function of transistor size and voltage level
- Small transistor gives slow response but small step.
- Large transistors gives fast response but large step.
- Parallel, different sized transistors with different pulse termination times may give both fast response and minimum step.



CMOS switch charge injection

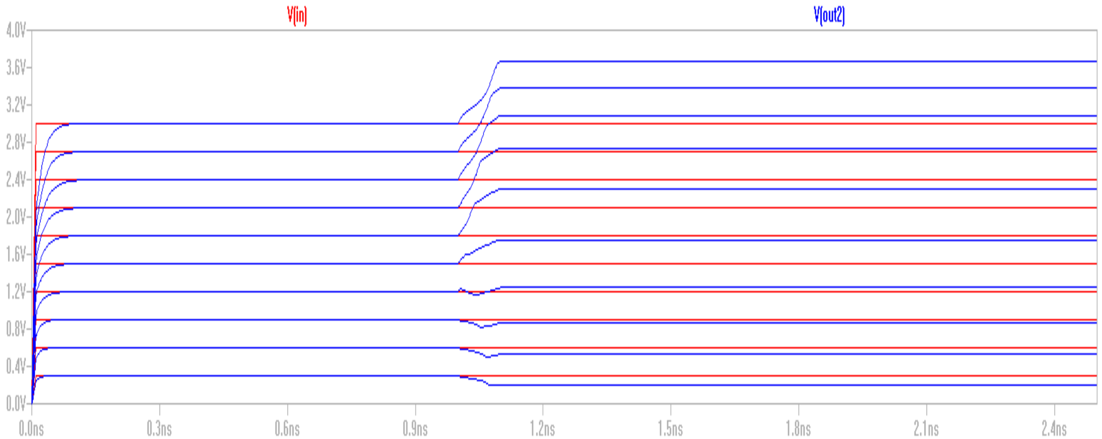
Top figure:

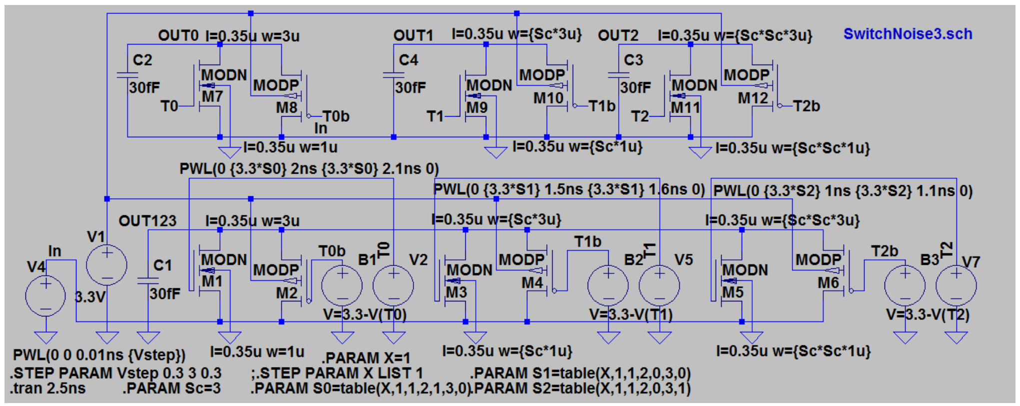
Observations:

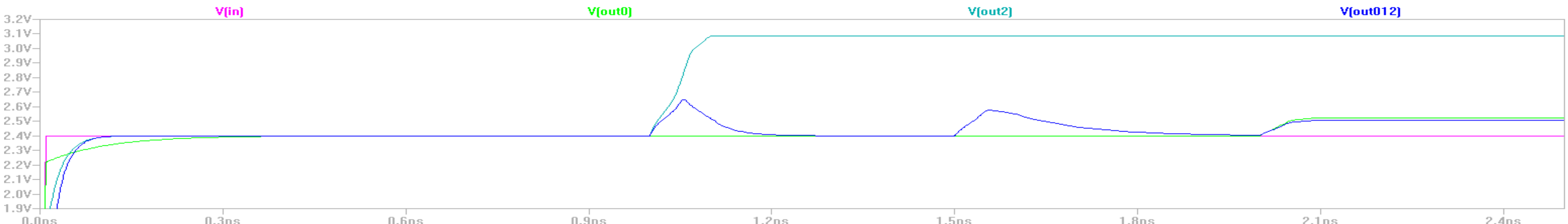
- Generated voltage step depends on signal level

Bottom figure:

- Sharp input pulse at 0ns, all switches closed (conducting)
- R2 (large) opens at 1ns
- R1 (medium) opens at 1.5ns
- R0 (small) opens at 2ns
- OUT0 : R0 : Slow but minimum step
- OUT2 : R2 : Fast but large step
- OUT012: R0+R1+R2 : Fast and minimum step



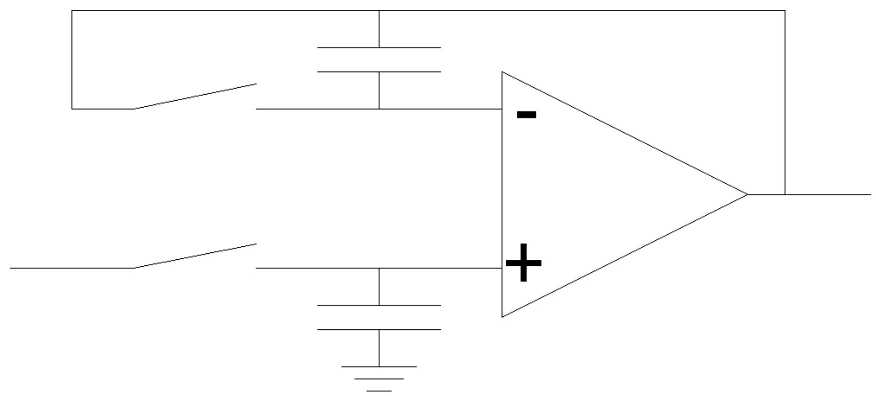




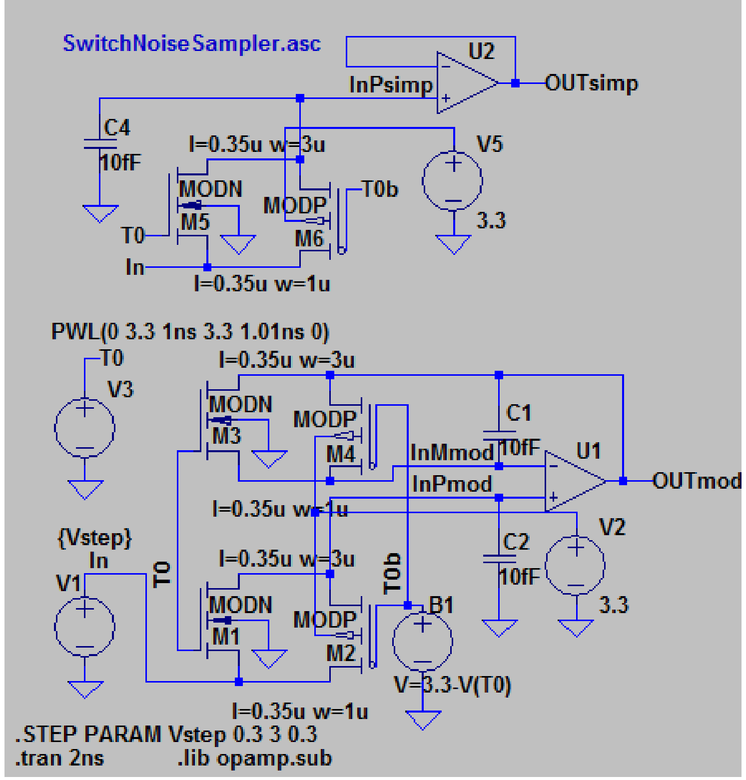
Sampler with switch charge cancelation

- A differential sampler with same sized switches on both inputs may almost eliminate the influence by the charge injection.
- At sampling both switches have the same potential and generates similar charge on both inputs.

RED: Figure

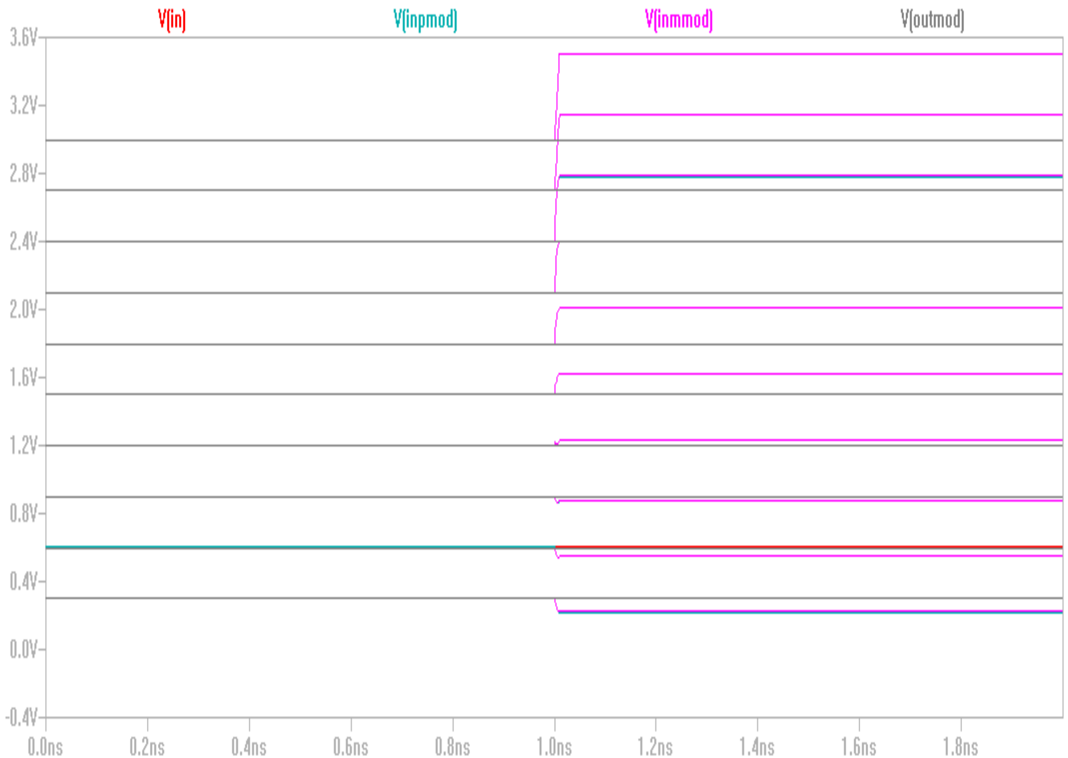


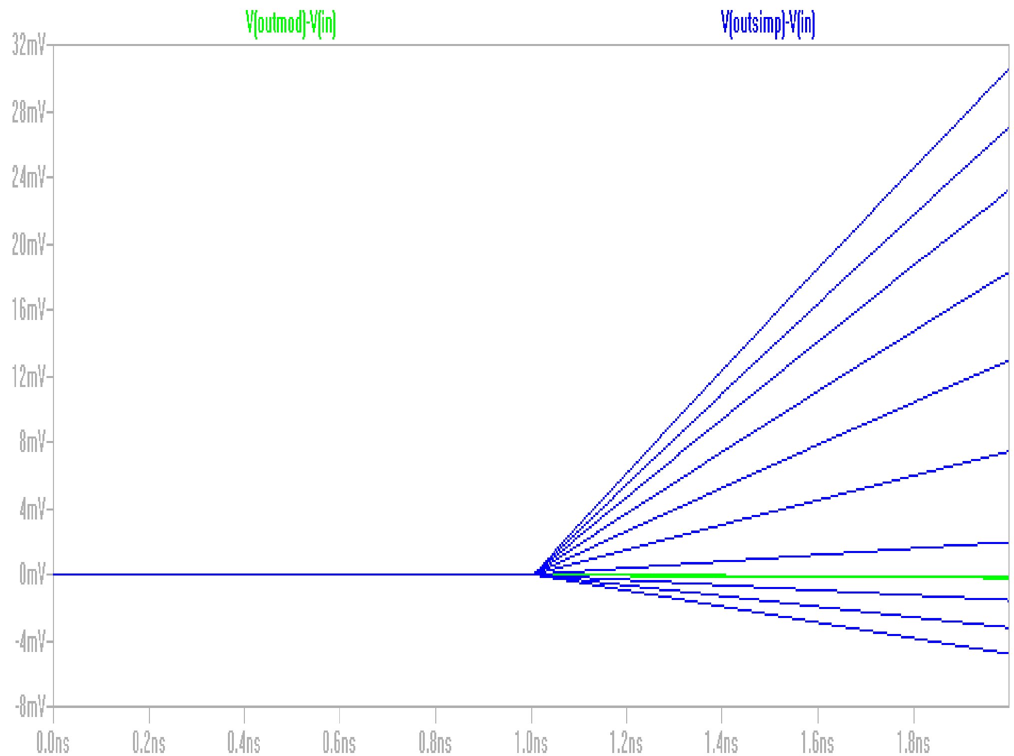
Sampler with injection compensation



- OUTsimp: standard
- OUTmod: with charge injection compensation

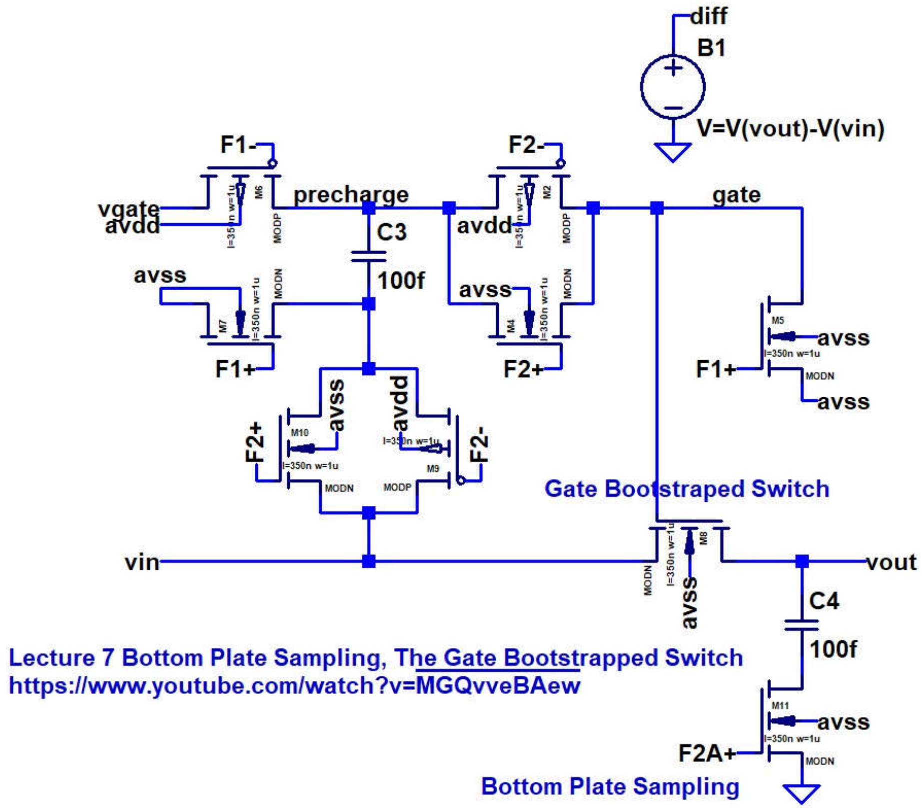
The two inputs experience an almost equal step resulting in a stable output





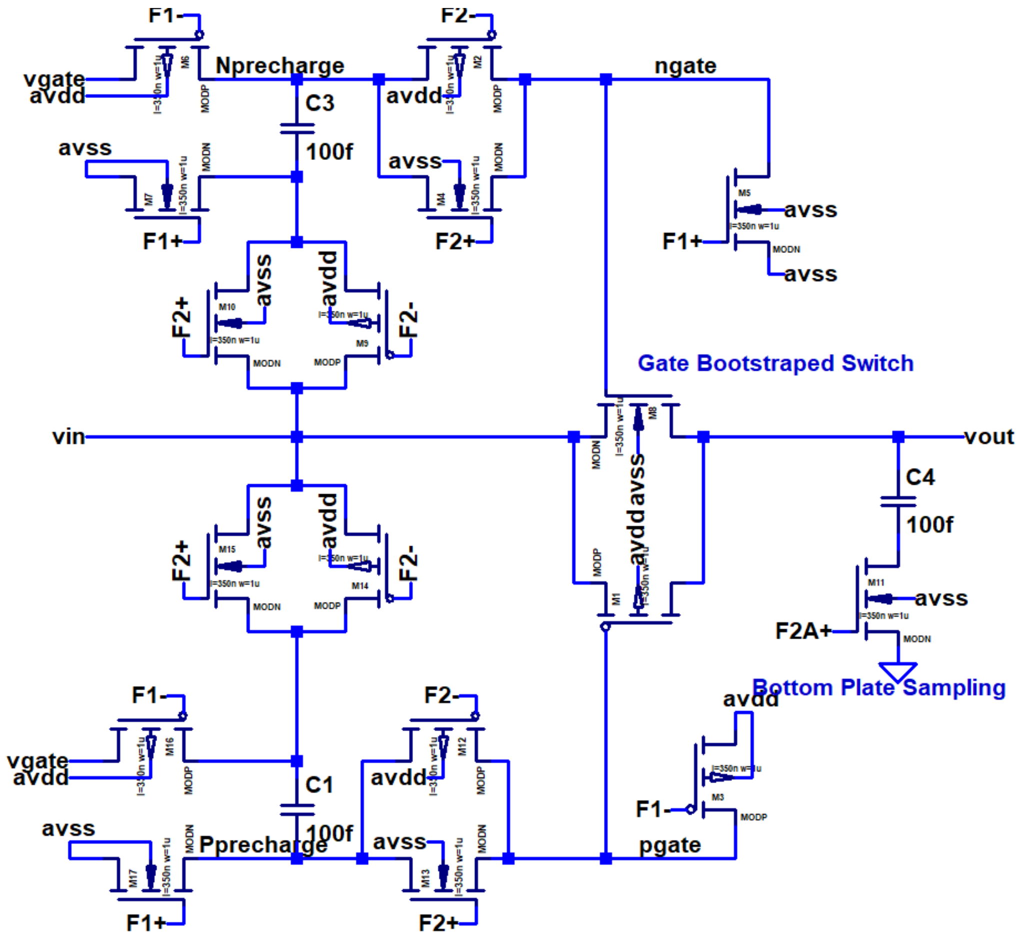
Gate bootstrapped switch with bottom plate sampling

- Bottom plate switch
  - Makes capacitor high impedance when sampling switch opens
- Gate bootstrap
  - Fixed *gate-vin* voltage reduces the errors steps *vin* dependence



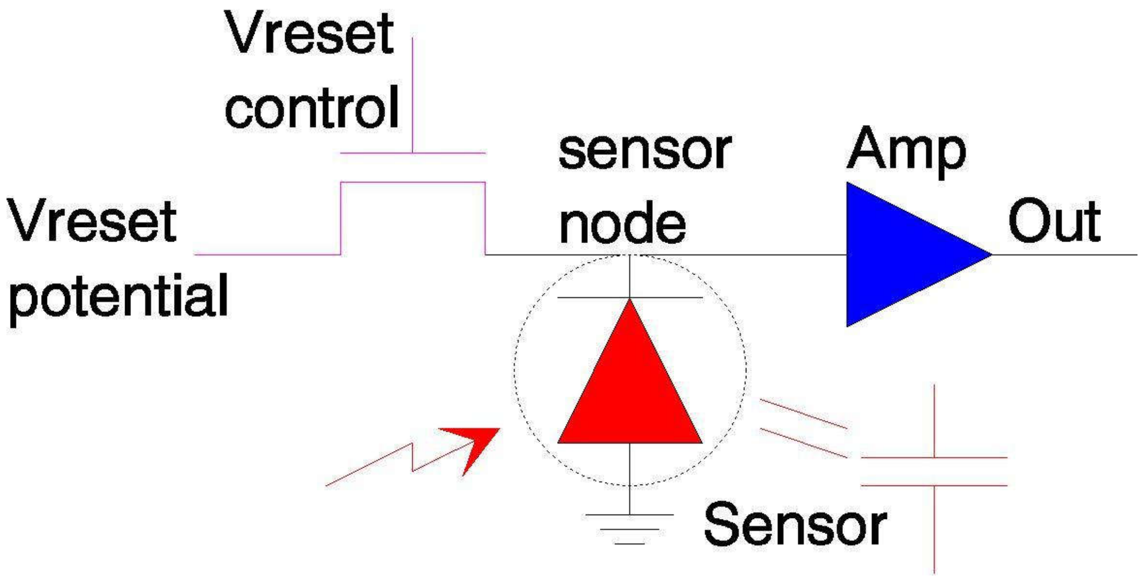
Double gate bootstrapped switch with bottom plate sampling

- Bootstrap on both NMOS and PMOS



Correlated double sampling: Background

- Photo diodes (CMOS pixel cells) consist of a reversed biased diode operating as a capacitor.



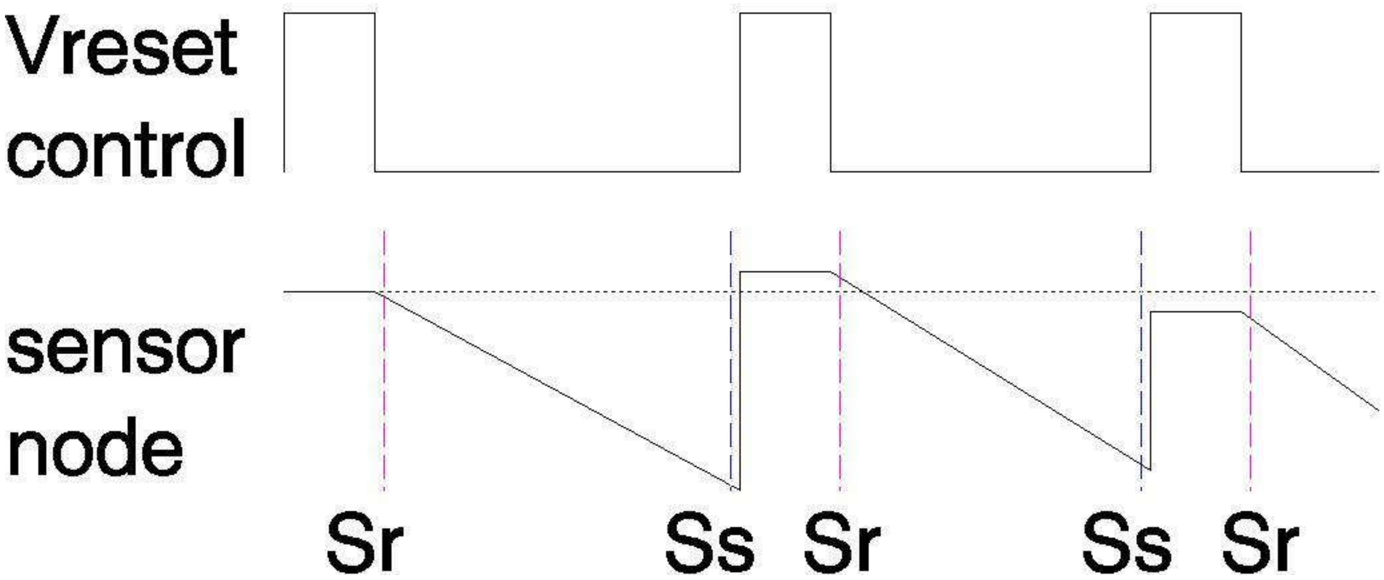
YELLOW: Figure

- A switched reset potential is placed on the sensor node. Accumulated electrons generated from light photons reduces the sensor node potential.

Correlated double sampling

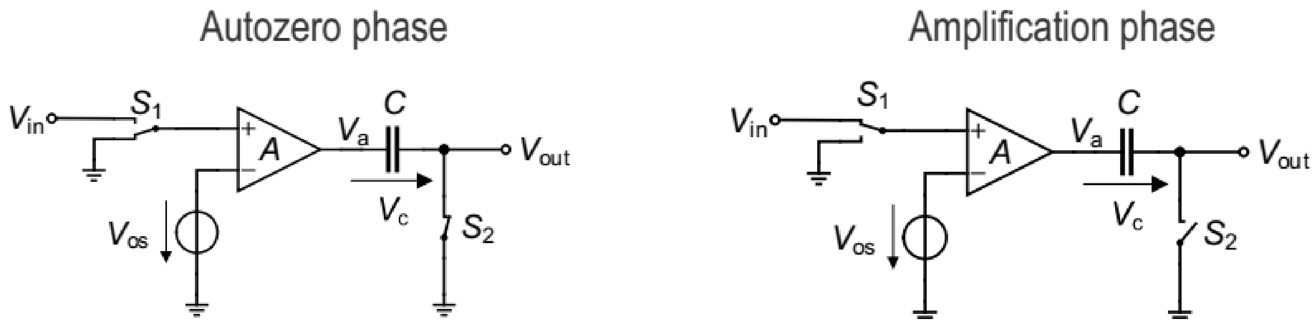
YELLOW: Figure

Due to charge injection and thermal noise the sensor node will be resat to unpredictable levels.

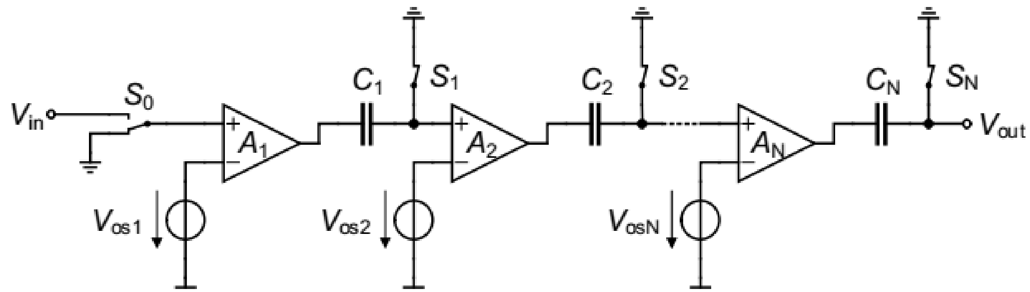


With correlated double sampling the value is measured both immediately after reset and before next reset. The difference is used.

The Autozero (AZ) technique

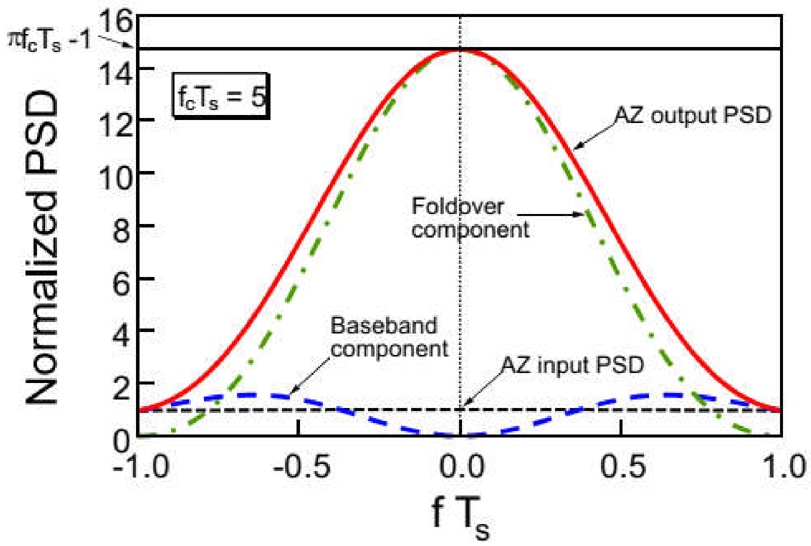


- On top: simple AZ
- Bottom: Multistage AZ

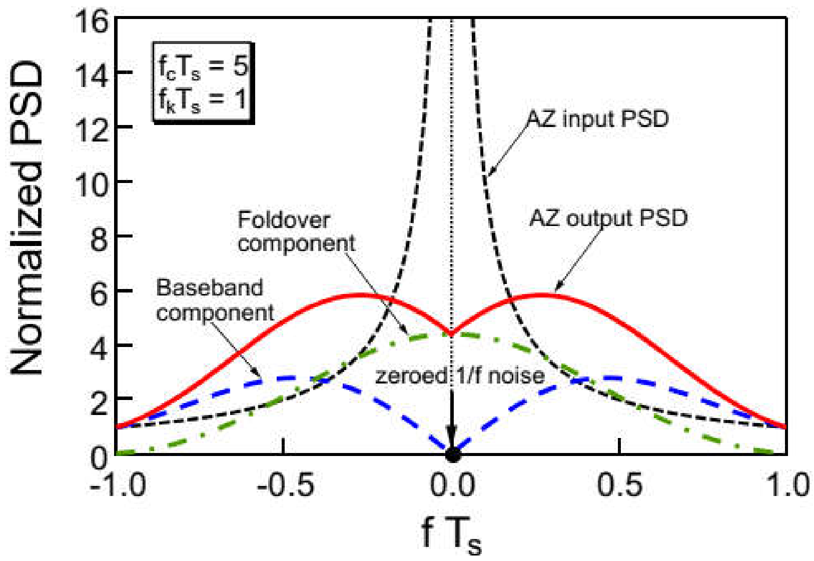


The Autozero (AZ) technique

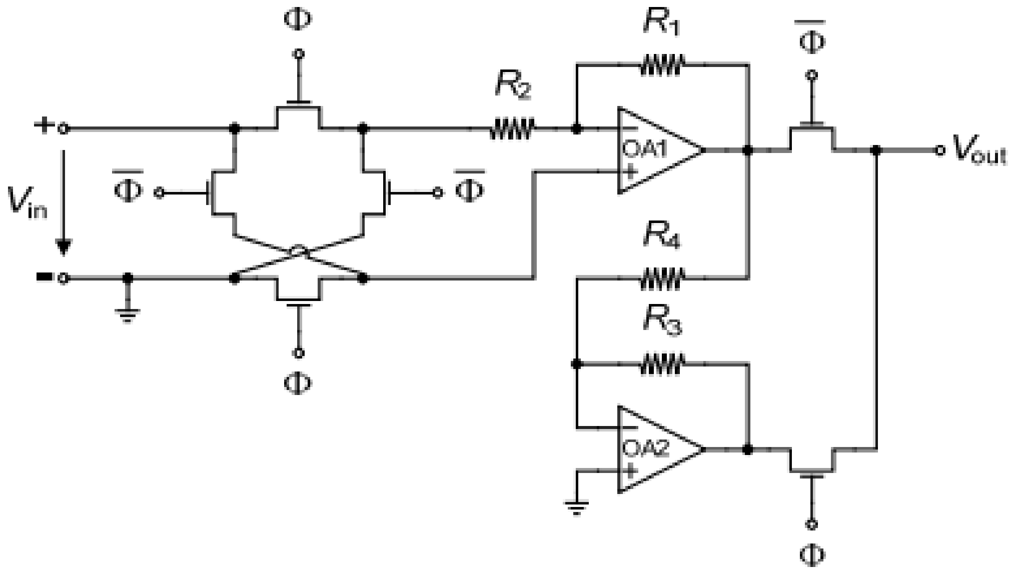
Effect of AZ on amplifier white noise

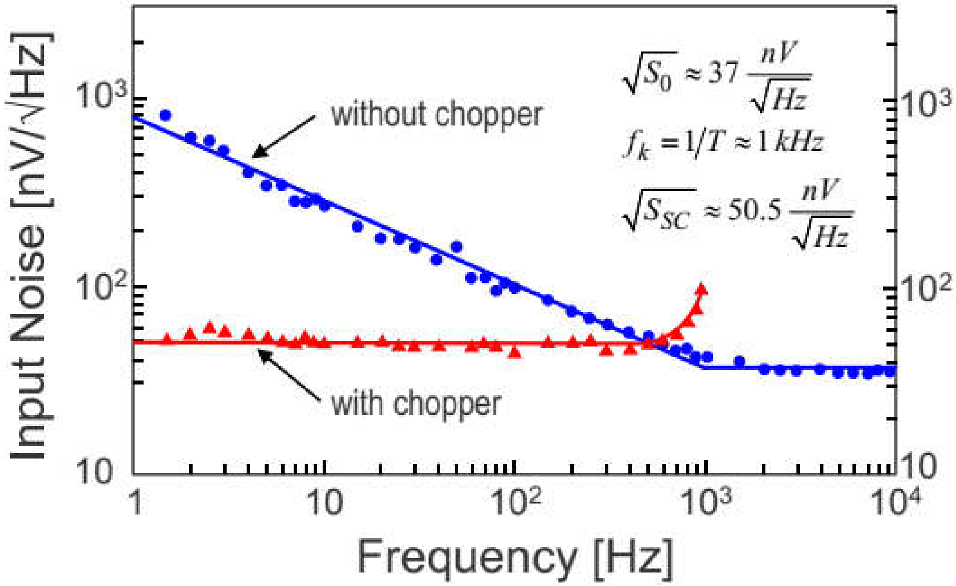


Effect of AZ on amplifier 1/f Noise



The Chopper Stabilization (CS) technique



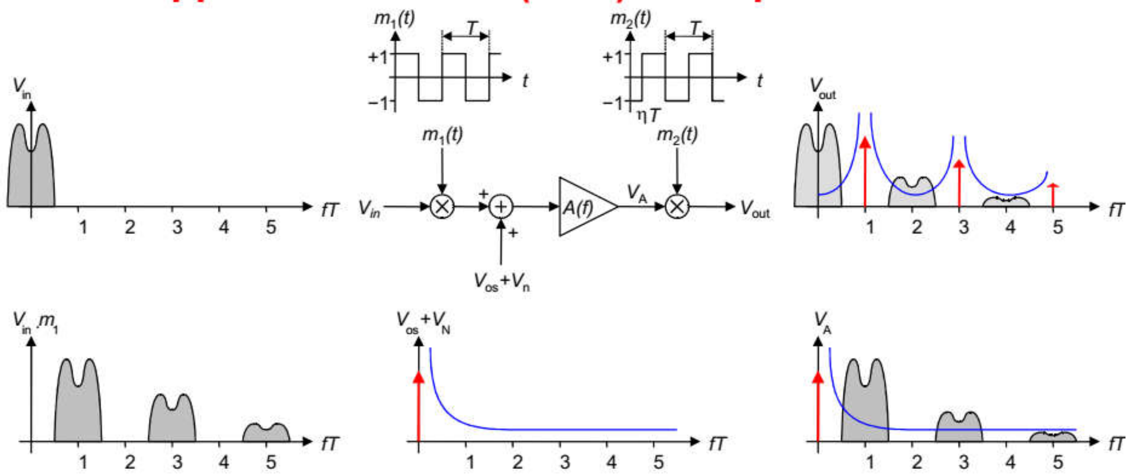


Chopper frequency set to amplifier corner frequency $f_{chop} = f_k = 1kHz$

The Chopper Stabilization (CS) technique

- CS requires two mixers
- It is only noise generated between the mixers that are reduced.

The Chopper Stabilization (CHS) Principle

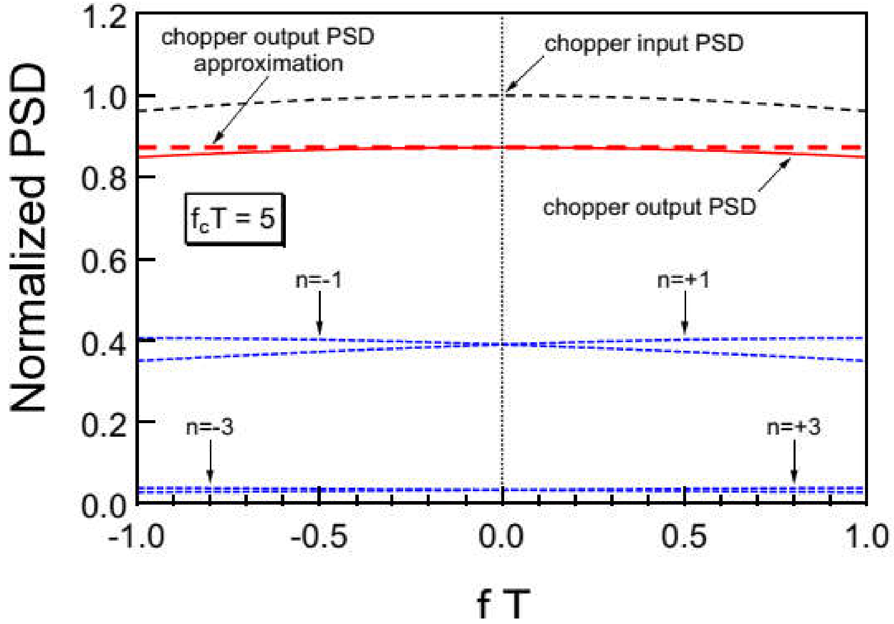


Unlike the AZ process, the CHS technique **does not use sampling**, but rather applies **modulation** to transpose the signal to a higher frequency where there is no 1/f noise, and then demodulates it back to the baseband after amplification

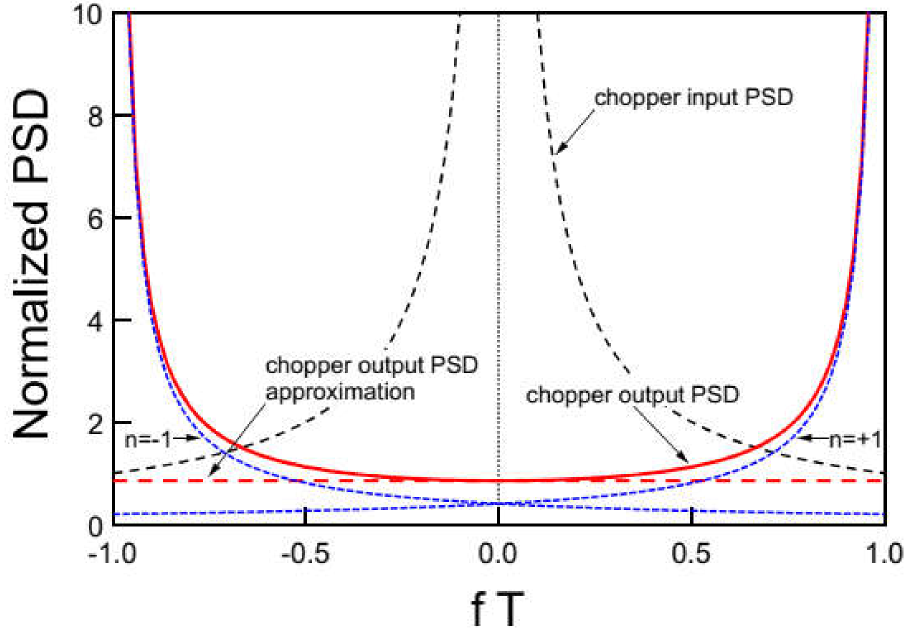
Since noise and offset are modulated only once, they are transposed to the odd harmonics of the output chopping square wave, leaving the amplifier ideally without any offset and low-frequency noise

The Chopper Stabilization (CS) technique

Effect of Chopping on the Amplifier White Noise



Effect of Chopping on the Amplifier 1/f Noise



The Chopper Stabilization (CS) technique

Conclusions

- Autozero and chopper stabilization are very effective techniques to reduce 1/f noise in low-frequency analog circuits
- They have been used extensively in the recent years to fight against the increased 1/f noise of nano-scale CMOS
- AZ is a **sampling technique** resulting in **noise aliasing**
- Thanks to the high-pass characteristic, the 1/f is canceled at the cost of an **increase of the white noise** coming from the foldover component
- Unlike AZ, CS **does not alias noise**
- 1/f noise is shifted to higher frequency **with almost no penalty on the residual white noise**