INF2270, counter with synchronous load

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Abstract

In this exercise you will extend the functionality of a simple sequential circuit that has been presented in the lecture.

Synchronous Counter with Load

Consider the state transition table 1 which is an extension from the one presented in the lecture of a 3bit counter. Here, the states are given as unsigned integer variables instead of spelling out the binary numbers, but they are still binary numbers. Two control signals and a 3-bit input I have been added: count enable (CE) and synchronous load (LD). Remember that 'X' means 'don't care', i.e. the value of that variable does not matter for the outcome of the next state. In contrast to the state transition table in the lecture, the schematics of the synchronous in the lecture (figure 1) did already accommodate a control signal CE. Can you extend the circuit further to also implement the function of the control signal LD? Hint: use JK-flipflops instead of T-flipflops and use two 1-bit multiplexers and one inverter per JK-flipflop (in addition to the gates already used in the lecture script) to achieve one possible solution.

present	in			next
S(2:0)	I(2:0)	CE	LD	S(2:0)
X	I	X	1	I
S	X	1	0	S+1
S	X	0	0	S

Table 1: State transition table for a counter with synchronous load and count enable

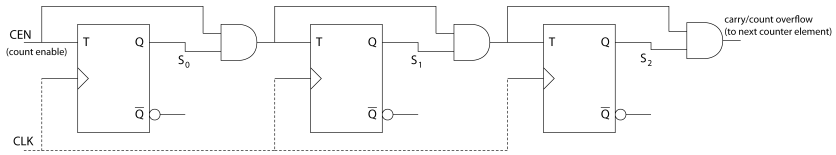

Figure 1: Synchronous counter from lecture with CE (but no LD)