# INF2270, building a simple memory control unit: example solution

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Figure 1 shows the solution. The combinational logic circuits resulting from the state transition conditions have been added to the D-flipflop input:

$$\begin{aligned} \text{MARCLK} &<= \text{CUopcode}(0) \wedge \overline{\text{MARCLK}} \\ \text{MBRCLK} &<= \text{MARCLK} \\ \text{WE} &<= \text{CUopcode}(1) \wedge \text{MARCLK} \end{aligned}$$

This implements the state machine as defined in the exercise's figure 1.

The following control signals were not yet connected in top.sch: The control signal for the bus multiplexer is directly 'CUopcode(1)' setting the source of the MBR to the CUregbus, if CUopcode(1) is low and to the memory output 'M' if opcode(1) is high. The clock signals for the MAR and MBR are (obviously) MARCLK and MBRCLK respectively, latching MAR at the start of the first clock cycle and MBR at the start of the second.

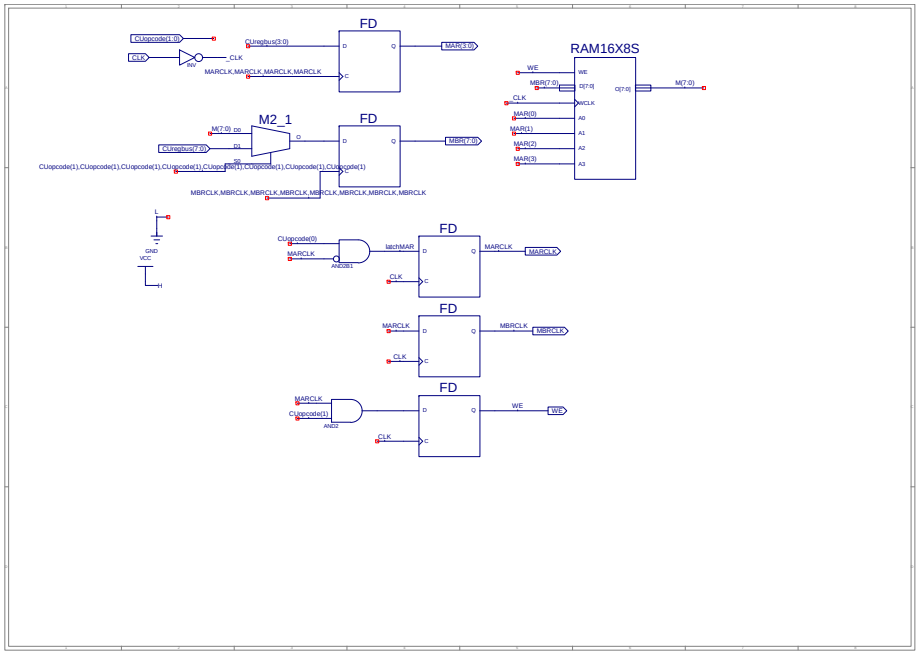


Figure 1: Schematics of the solution