INF2270, counter with synchronous load

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Synchronous Counter with load

Figure 1 shows one possible solution. Remember that a JK flipflop works like a T-flipflop if J and K are shortened. This is the case if LD=0 since the same signal is routed to bothe J and K through the multiplexers and the circuit becomes equivalent to the synchronous counter without a LD control signal.

When LD=1, on the other hand, K receives the inverted J signal and J is shorted to the input. Thus, on the next clock edge, the value I is loaded into the counter.

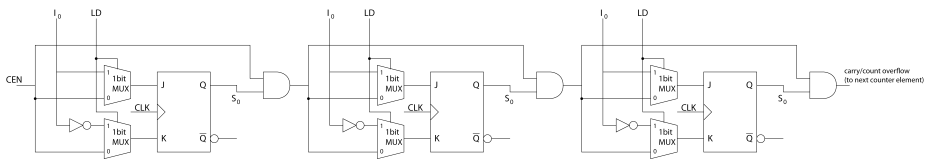

Figure 1: A counter with LD and CE control signals