INF2270, exercise in sequential logic: example solution

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Figure 1 shows a solution with a Moore machine. A useful sanity check for this particular example here: make sure that for any possible input there is a way out of a state! That is necessary for this particular FSM since the time variable t will always have to change.

For the time variable t we simply use a normal synchronous counter that we already have deduced in the lecture. Table 1 shows the state transition table for state variable h.

The Karnaugh map for the state variable h is shown in table 2. There are things that I did not tell you in the lecture about Karnaugh maps with more than 4 variables. If there are three variables along one edge of the map, the map is divided into two sections. The most significant bit is constant for the whole section. Rectangles cannot be formed in the same plain accross the division but 3D cubes can be formed by folding the two sections on top of each other. (Karnaugh maps with more than 4 binary variables will not occure in the exam!) Note that the X's (do not care, for the input c bigger than 4 that do not occure) can be combined into rectangles of 1's freely to make them as big as possible, since they may be chosen to be 1's.

The resulting Boolean function is

$$
\begin{aligned}
h_{\text{next}} &= (c_2) \vee (t_0 \wedge t_1 \wedge c_0) \vee (t_0 \wedge t_1 \wedge c_1) \vee (\bar{t1} \wedge c_0 \wedge c_1) \vee (\bar{t_0} \wedge \bar{t_1} \wedge c_1) \\
&= (c_2) \vee (t_0 \wedge t_1 \wedge (c_0 \vee c_1)) \vee (\bar{t1} \wedge c_0 \wedge c_1) \vee (\bar{t_0} \wedge \bar{t_1} \wedge c_1)
\end{aligned}
$$

and the corresponding schematic is shown in figue 2. The output is identical with the state variable h.

The Mealy machine is deduced quite similarly, but h is now only the output and no state variable. It is deduced directly from the input and the state variable t. The truth table of the output combinational logic is quite similar to the state transition table of the Moore machine, with the difference being that the output switching to 1 is shifted forward in time since it is not buffered by a D-flip-flop that only switches at the *next* positive clock edge. See table 3

The Karnaugh map is in table 4.
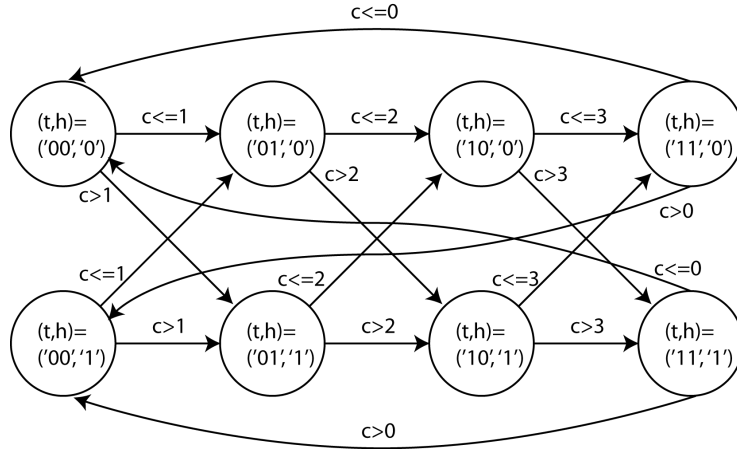
The resulting Boolean function is:

Figure 1: A Moore FSM that solves the control task. State variables are the time t (2bit) and the state of the heater h (1 bit, on/off). The control signal from the switch we choose to be binary numbers 0-4, i.e. 3 bits.

t	c	h_{next}
00	000	0
00	001	0
00	010	1
00	011	1
00	100	1
01	000	0
01	001	0
01	010	0
01	011	1
01	100	1
10	000	0
10	001	0
10	010	0
10	011	0
10	100	1
11	000	0
11	001	1
11	010	1
11	011	1
11	100	1

Table 1: State Transition Table for variable 'h'

Table 2: Karnaugh map for the state variable h.
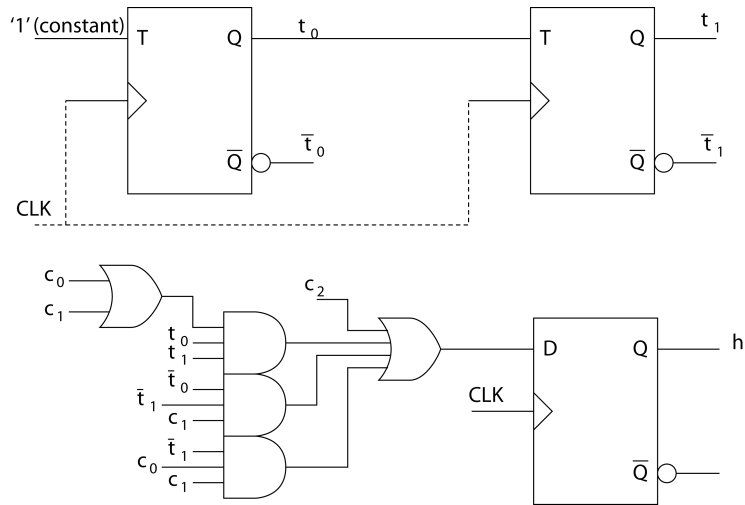
Figure 2: The resulting Sequential logic circuit

t	c	h_{next}
00	000	0
00	001	1
00	010	1
00	011	1
00	100	1
01	000	0
01	001	0
01	010	1
01	011	1
01	100	1
10	000	0
10	001	0
10	010	0
10	011	1
10	100	1
11	000	0
11	001	0
11	010	0
11	011	0
11	100	1

Table 3: Output Truth Table for output 'h' for the Mealy FSM

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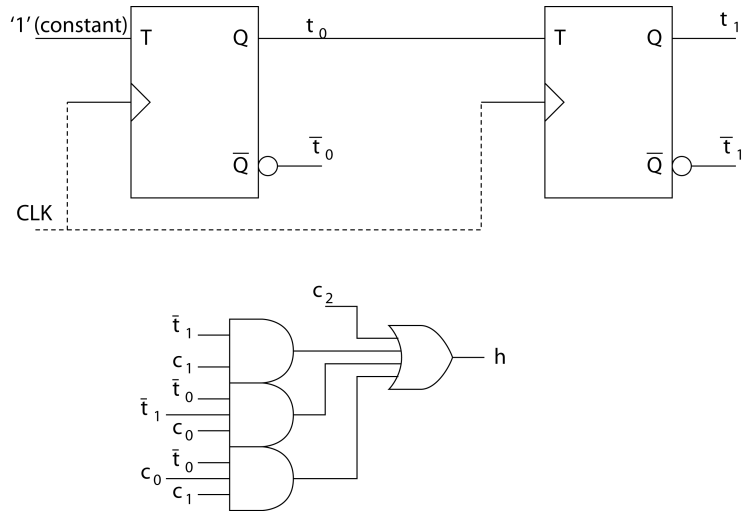| c \ t	00	01	11	10
000	0	0	0	0
001	1	0	0	0
011	1	1	0	1
010	1	1	0	0
110	X	X	X	X
111	X	X	X	X
101	X	X	X	X
100	1	1	1	1

Table 4: Karnaugh map for the output h.

Figure 3: The sequential logic circuit resulting from the Mealy FSM

$$h \;=\; (c_2) \vee (\bar{t_1} \wedge c_1) \vee (\bar{t_0} \wedge \bar{t_1} \wedge c_0) \vee (\bar{t_0} \wedge c_0 \wedge c_1)$$

and the corresponding circuit is shown in figure 3