INF2270, count once from 0 to 15

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Abstract

In this exercise we will have a closer look at a part of the mandatory exercise

The Task

Implement and simulate a circuit that is triggered by a short voltage pulse (Diglog cell PULSE) or by switching a SWITCH on and off, and then counts from 0 to 15 once, before stopping and being reset to zero. Use the cell 16COUNT of Diglog.

Note that it has an 'asynchronous reset' control signal labelled with 'C', i.e. once the control signal is asserted it is reset immediately without waiting for a clock. Thus, there are some solutions to our task where the counter output is at 15 only briefly and not for a whole clock cycle. To improve this, try to think about using an extra flipflop, e.g. a JK flipflop, between your combinational logic that determines the reset condition and the actual reset pin of the 16COUNT cell. This will delay the reset until the next clock edge. Also note that the JK flipflop cell JKPOS also has two additional inputs as compared to a basic JK flipflop as presented in the course: an asynchronous active low set (top pin) and an asynchronous active low reset (bottom pin). It is, thus, both an RS flipflop and a JK flipflop in one building block.

Another potential problem when using a PULSE to start the counting is the fact that this pulse is of no use setting a *synchronous* flipflop, since it would need to exactly coincide with the clock edge. Thus, one would need an asynchronous flipflop that extends this pulse to at least the start of the next clock cycle. Since the JKPOS cell is botha a JK and an RS flipflop one can solve this problem by applying the PULSE signal to an asynchronous input, wheras the reset codition combinational logic output can be connected to a synchronous input (J or k). With only flipflops that ar *either* synchronous *or* asynchronous one would actually need two, e.g. an RS latch and a JK flipflop.

Go ahead and experiment with different options. There are actually several possible solutions. Good luck!