INF2270, repetitions: sequential logic

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Abstract

Sequential Logic from a State Transition Graph (Exam 2010)

Figure 1 shows a state transition graph defineing a synchronous finite state machine (FSM). Draw a circuit schematics that implements this FSM with state variables s_0 and s_1 and inputs x_0 and x_1. Remember to make sure that the FSM remains in the same state if the state transition condition is not met! Also, make sure that if the FSM should ever accidentally (e.g. after startup) enter the state $s_0 = 1 \ \wedge \ s_1 = 1$ that is not defined by the state transition graph, that it gets not stuck there but goes to the state $s_0 = 0 \ \wedge \ s_1 = 0$ with the next clock signal instead. Do show intermediate results that illustrate your approach to solve this tasks.

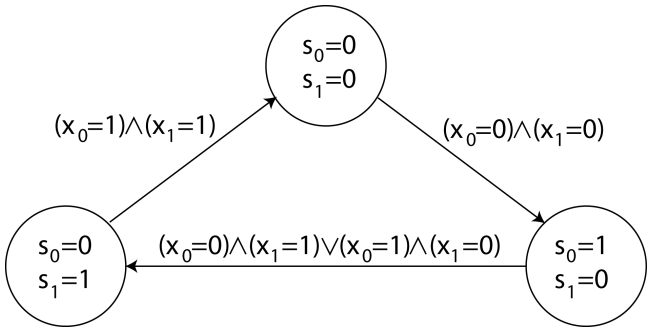

Figure 1: a state transition graph describing a FSM