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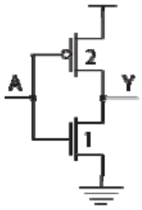
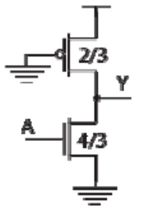
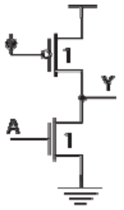
Introduksjon til dynamisk CMOS



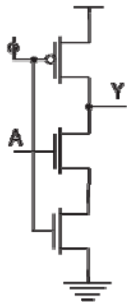
Komplementær



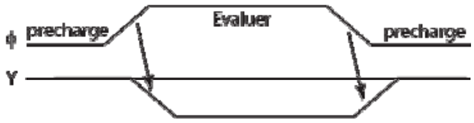
Pseudo nMOS



Dynamisk



”Footed” dynamisk



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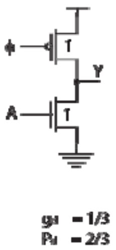
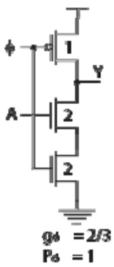
Dynamiske invertere:





Ikke-footed inverter:

$$g_d = \frac{W_n}{\left(1+\frac{\mu_n}{\mu_p}\right)\cdot\left(\frac{1}{W_n}\right)^{-1}} = \frac{W_n}{3W_n} = \frac{1}{3}$$

$$P_d = \frac{1}{W_n}\cdot R\cdot(W_p+W_n)\cdot C = 1R\cdot 2C = 2RC = \frac{2}{3}\tau$$

Footed inverter:

$$g_d = \frac{W_n}{\left(1+\frac{\mu_n}{\mu_p}\right)\cdot\left(\frac{1}{W_n}+\frac{1}{W_n}\right)^{-1}} = \frac{W_n}{3\left(\frac{2}{W_n}\right)^{-1}} = \frac{2}{3}$$

$$P_d = \left(\frac{1}{W_n}+\frac{1}{W_n}\right)\cdot R\cdot(W_p+W_n)\cdot C = \left(\frac{1}{2}+\frac{1}{2}\right)R\cdot(1+2)C = 3RC = 1\tau$$

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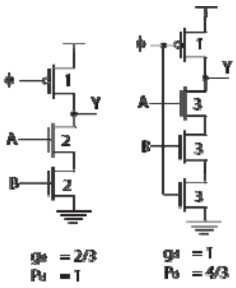
Dynamiske NAND2:



Ikke-footed NAND2:

$$g_d = \frac{W_n}{\left(1+\frac{\mu_n}{\mu_p}\right)\cdot\left(\frac{1}{W_n}+\frac{1}{W_n}\right)^{-1}} = \frac{W_n}{3\left(\frac{2}{W_n}\right)^{-1}} = \frac{2}{3}$$

$$P_d = \left(\frac{1}{W_n}+\frac{1}{W_n}\right)\cdot R\cdot\left(W_p+W_n\right)\cdot C = \left(\frac{1}{2}+\frac{1}{2}\right)R\cdot(1+2)C = 3RC = 1\tau$$

Footed NAND2:

$$g_d = \frac{W_n}{\left(1+\frac{\mu_n}{\mu_p}\right)\cdot\left(\frac{1}{W_n}+\frac{1}{W_n}+\frac{1}{W_n}\right)^{-1}} = \frac{W_n}{3\left(\frac{3}{W_n}\right)^{-1}} = 1$$

$$P_d = \left(\frac{1}{W_n}+\frac{1}{W_n}+\frac{1}{W_n}\right)\cdot R\cdot\left(W_p+W_n\right)\cdot C = \left(\frac{1}{3}+\frac{1}{3}+\frac{1}{3}\right)R\cdot(1+3)C = 4RC = \frac{4}{3}\tau$$

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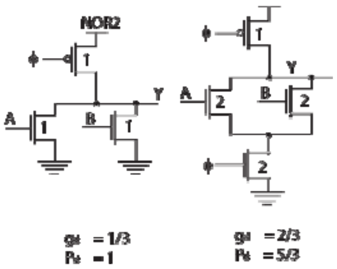
Dynamiske NOR2:



Ikke-footed NOR2:

$$g_d = \frac{W_n}{\left(1+\frac{\mu_n}{\mu_p}\right)\cdot\left(\frac{1}{W_n}\right)^{-1}} = \frac{W_n}{3\left(\frac{1}{W_n}\right)^{-1}} = \frac{1}{3}$$

$$P_d = \left(\frac{1}{W_n}\right)\cdot R\cdot\left(W_p+W_n+W_n\right)\cdot C = \left(\frac{1}{2}+\frac{1}{2}\right)R\cdot(1+1+1)C = 3RC = 1\tau$$

Footed NOR2:

$$g_d = \frac{W_n}{\left(1+\frac{\mu_n}{\mu_p}\right)\cdot\left(\frac{1}{W_n}+\frac{1}{W_n}\right)^{-1}} = \frac{W_n}{3\left(\frac{2}{W_n}\right)^{-1}} = \frac{2}{3}$$

$$P_d = \left(\frac{1}{W_n}+\frac{1}{W_n}\right)\cdot R\cdot\left(W_p+W_n+W_n\right)\cdot C = \left(\frac{1}{2}+\frac{1}{2}\right)R\cdot(1+2+2)C = 5RC = \frac{5}{3}\tau$$

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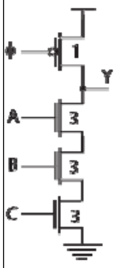
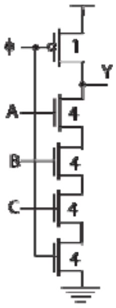
Oppgave 6.27

Tegn transistorskjema for dynamisk footed 3inngangs NAND og NOR porter. Angi bredde p˚a transistorene. Hva blir logisk effort for portene?

Dynamiske NAND3:



$g_d = 1$
$P_d = 4/3$



$g_d = 4/3$
$P_d = 5/3$

Ikke-footed NAND3:

$$g_d = \frac{W_n}{\left(1+\frac{\mu_n}{\mu_p}\right)\cdot\left(\frac{1}{W_n}+\frac{1}{W_n}+\frac{1}{W_n}\right)^{-1}} = \frac{W_n}{3\left(\frac{3}{W_n}\right)^{-1}} = 1$$

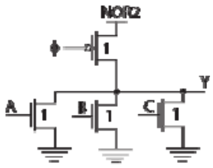
$$P_d = \left(\frac{1}{W_n}+\frac{1}{W_n}+\frac{1}{W_n}\right)\cdot R\cdot\left(W_p+W_n\right)\cdot C = \left(\frac{1}{3}+\frac{1}{3}+\frac{1}{3}\right)R\cdot(1+3)C = 4RC = \frac{4}{3}\tau$$

Footed NAND3:

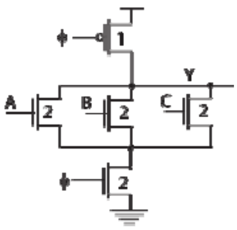
$$g_d = \frac{W_n}{\left(1+\frac{\mu_n}{\mu_p}\right)\cdot\left(\frac{1}{W_n}+\frac{1}{W_n}+\frac{1}{W_n}+\frac{1}{W_n}\right)^{-1}} = \frac{W_n}{3\left(\frac{4}{W_n}\right)^{-1}} = \frac{4}{3}$$

$$P_d = \left(\frac{1}{W_n}+\frac{1}{W_n}+\frac{1}{W_n}+\frac{1}{W_n}\right)\cdot R\cdot\left(W_p+W_n\right)\cdot C = \left(\frac{1}{4}+\frac{1}{4}+\frac{1}{4}+\frac{1}{4}\right)R\cdot(1+4)C = 5RC = \frac{5}{3}\tau$$

Dynamiske NOR3:



$g_d = 1/3$
$P_d = 4/3$



$g_d = 2/3$
$P_d = 7/3$

Ikke-footed NOR3:

$$g_d = \frac{W_n}{\left(1+\frac{\mu_n}{\mu_p}\right)\cdot\left(\frac{1}{W_n}\right)^{-1}} = \frac{W_n}{3\left(\frac{1}{W_n}\right)^{-1}} = \frac{1}{3}$$

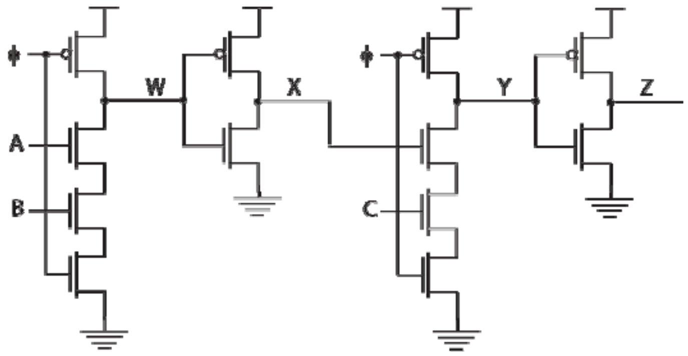
$$P_d = \left(\frac{1}{W_n}\right)\cdot R\cdot\left(W_p+W_n+W_n+W_n\right)\cdot C = \left(\frac{1}{2}+\frac{1}{2}\right)R\cdot(1+1+1+1)C = 4RC = \frac{4}{3}\tau$$

Footed NOR3:

$$g_d = \frac{W_n}{\left(1+\frac{\mu_n}{\mu_p}\right)\cdot\left(\frac{1}{W_n}+\frac{1}{W_n}\right)^{-1}} = \frac{W_n}{3\left(\frac{2}{W_n}\right)^{-1}} = \frac{2}{3}$$

$$P_d = \left(\frac{1}{W_n}+\frac{1}{W_n}\right)\cdot R\cdot\left(W_p+W_n+W_n+W_n\right)\cdot C = \left(\frac{1}{2}+\frac{1}{2}\right)R\cdot(1+2+2+2)C = 7RC = \frac{7}{3}\tau$$

Domino logikk



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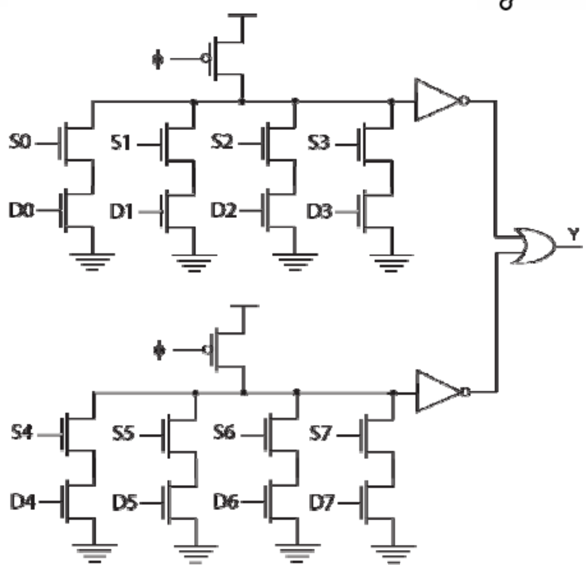
Domino multiplekser:



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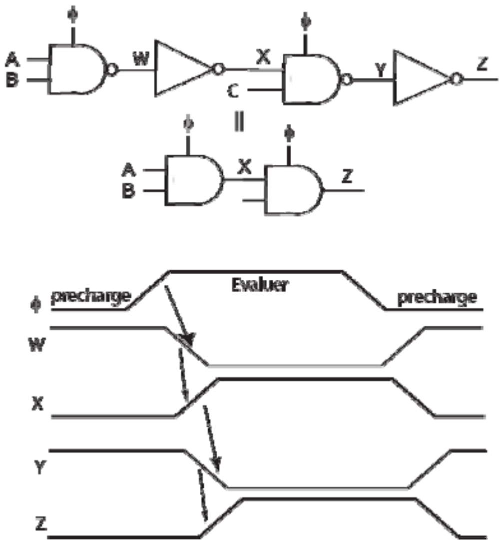
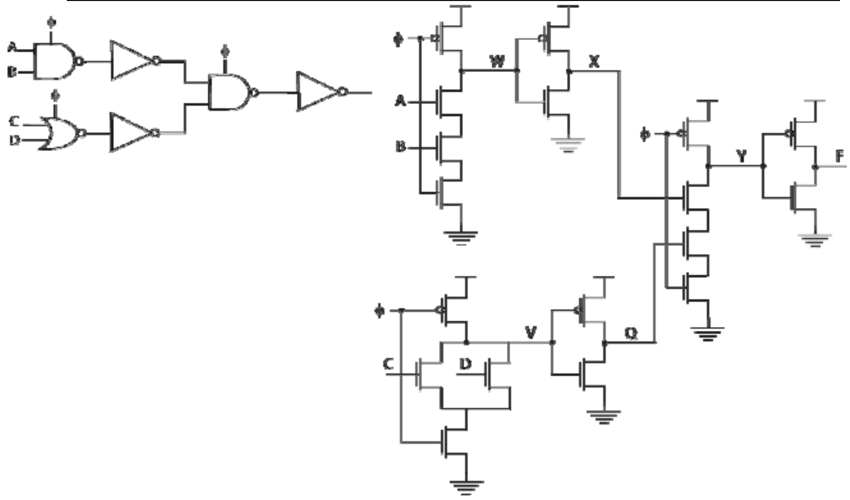
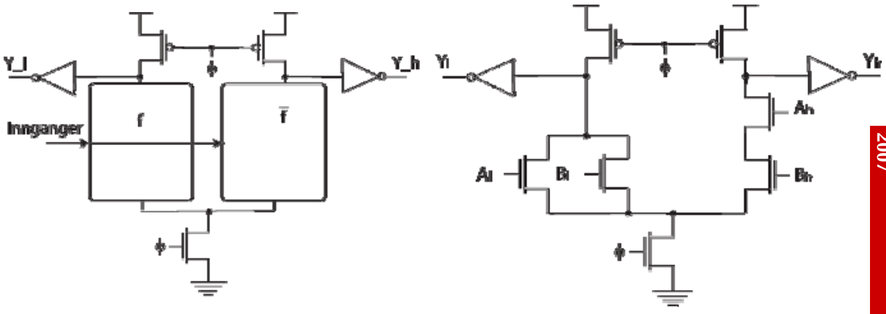


Oppgave B

Tegn transistorskjema for funksjonen $F = A \cdot B \cdot (C + D)$ ved å bruke domino logikk.



Dual-rail domino logikk



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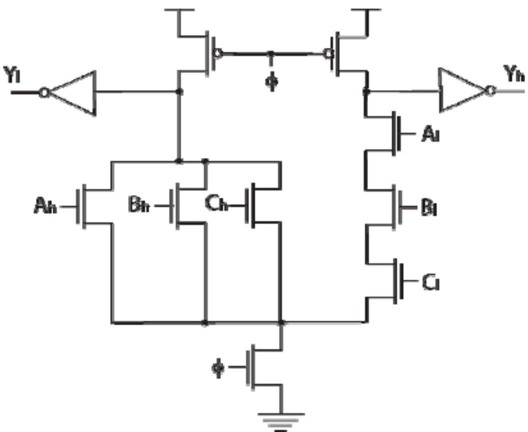
Oppgave 6.28

Tegn transistorskjema for en 3inngangs dual-rail domino OR/NOR port.



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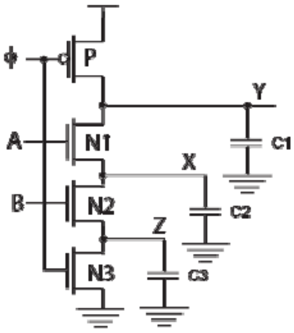
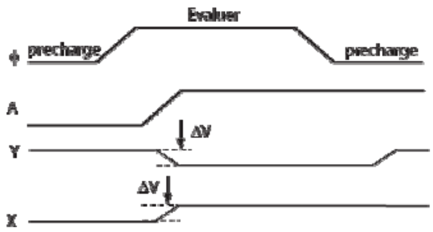
Ladningsdeling





Endring pga. ladningsdeling:

$$\Delta V = \left(1 - \frac{C_1}{C_1 + C_2}\right) \cdot V_{DD}$$

$$V_Y = V_{DD} - \Delta V$$

$$V_X \approx V_Y$$

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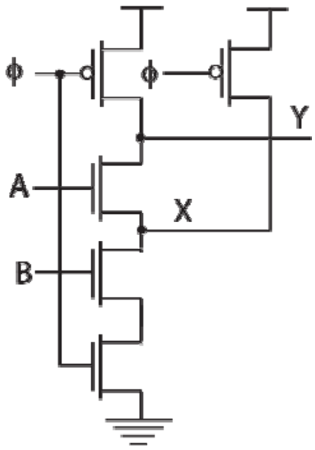
Precharge av interne nodert



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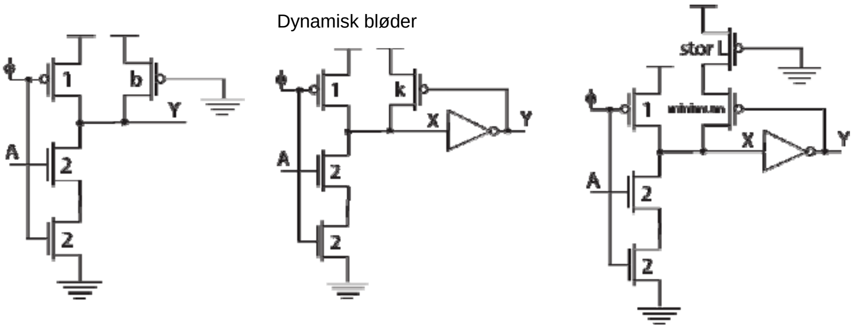
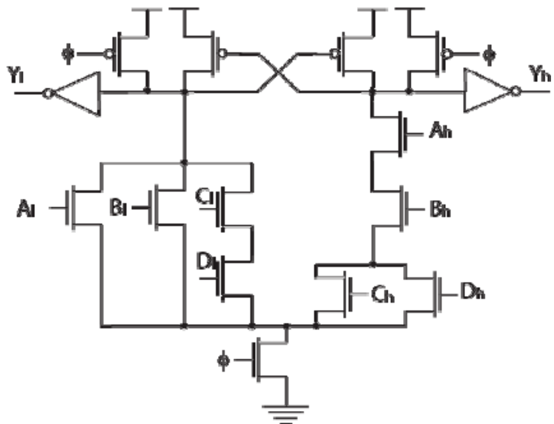
Blødere (keepers)



Oppgave D

Tegn transistorskjema for funksjonen *F* = *A*·*B*·(*C* +*D*) med en differensiell dynamisk port med dynamisk bløder. Diskuter fordeler og ulemper med denne implementasjon i forhold til domino logikk.

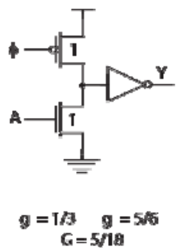


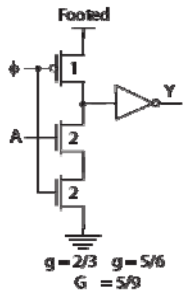
Logisk effort i dynamiske kjeder

Ikke-footed:

$$G_u = \frac{1}{3}\cdot\frac{5}{6} = \frac{5}{18}$$

$$G_d = \frac{2}{3}\cdot\frac{5}{3} = \frac{10}{9}$$





Footed:

$$G_u = \frac{2}{3}\cdot\frac{5}{6} = \frac{5}{9}$$

$$G_d = \frac{4}{3}\cdot\frac{5}{3} = \frac{20}{9}$$

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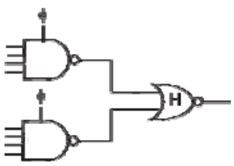
Eksempel:



$$G_u = \frac{5}{3}\cdot\frac{3}{2} = \frac{5}{2}$$

$$P_u = (5C + C)\cdot R + \left(4C + 2\cdot\frac{1}{2}C\right)\cdot R = 11RC = \frac{11}{3}\tau$$

$$N = 2$$

$$f' = F^{\frac{1}{2}} = (G\cdot 1\cdot H)^{\frac{1}{2}} = \sqrt{\frac{5H}{2}}$$

Tidsforsinkelse i kjeden:

$$D = NF^{\frac{1}{N}} + P_u = 2\sqrt{\frac{5H}{2}} + \frac{11}{3}$$

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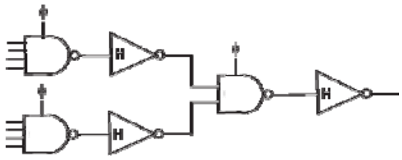
Eksempel:



$$N = 4$$

$$f' = F^{\frac{1}{4}}$$

$$= (G \cdot 1 \cdot H)^{\frac{1}{4}}$$

$$= \left(\frac{125H}{108}\right)^{\frac{1}{4}}$$

$$G_u = \frac{5}{3} \cdot \frac{5}{6} \cdot 1 \cdot \frac{5}{6}$$

$$= \frac{125}{108}$$

$$P_u = (5C + C) \cdot R + \left(2 + \frac{1}{2}\right) C \cdot R + (3C + C) \cdot R + \left(2 + \frac{1}{2}\right) C \cdot R$$

$$= 15RC$$

$$= 5\tau$$

Tidsforsinkelse i kjeden:

$$D = NF^{\frac{1}{N}} + P_u$$

$$= 4 \cdot \left(\frac{125H}{108}\right)^{\frac{1}{4}} + 5$$

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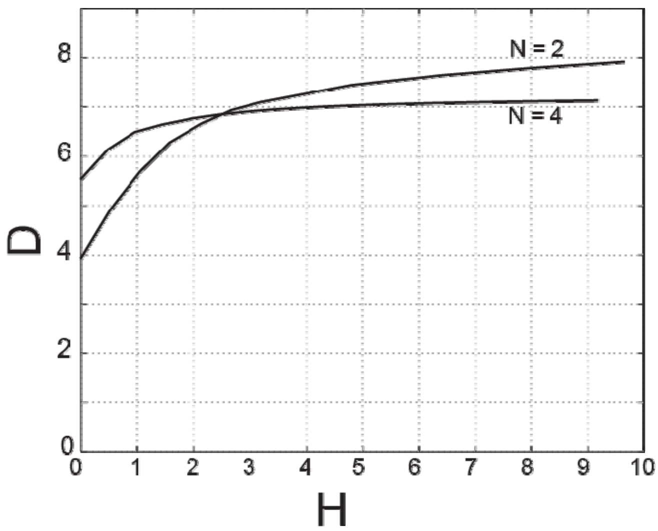

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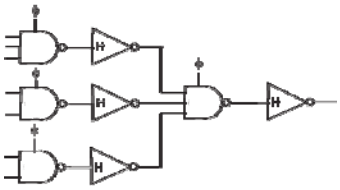
Oppgave E

Finn tidsforsinkelse i den dynamiske kjeden som er vist i Figuren.



$$N = 4$$

$$f' = F^{\frac{1}{4}} = (G \cdot 1 \cdot H)^{\frac{1}{4}} = \left(\frac{100H}{81}\right)^{\frac{1}{4}}$$

$$G_u = \frac{4}{3} \cdot \frac{5}{6} \cdot \frac{4}{3} \cdot \frac{5}{6} = \frac{100}{81}$$

Tidsforsinkelse i kjeden:

$$P_u = 5RC + \left(2 + \frac{1}{2}\right)C \cdot R + 5RC + \left(2 + \frac{1}{2}\right)C \cdot R = 15RC = 5\tau$$

$$D = NF^{\frac{1}{N}} + P_u = 4 \cdot \left(\frac{100H}{81}\right)^{\frac{1}{4}} + 5$$

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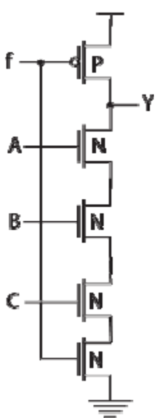
Eksamensoppgave 2005

Hva blir parasittisk tidsforsinkelse for nedtrekket for 3inngangsdynamisk footed NAND porten?



Velger N=4 som gir effektiv motstand i nedtrekket lik R:

$$P_d = R(1+4)C = 5RC = \frac{5}{3}\tau$$

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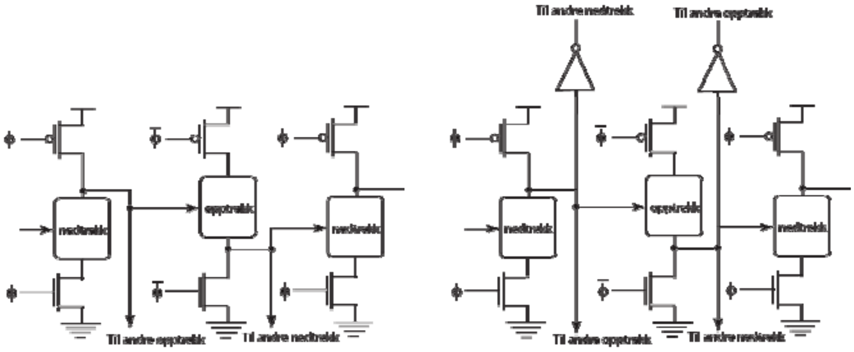
NP (og Zipper domino)



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