

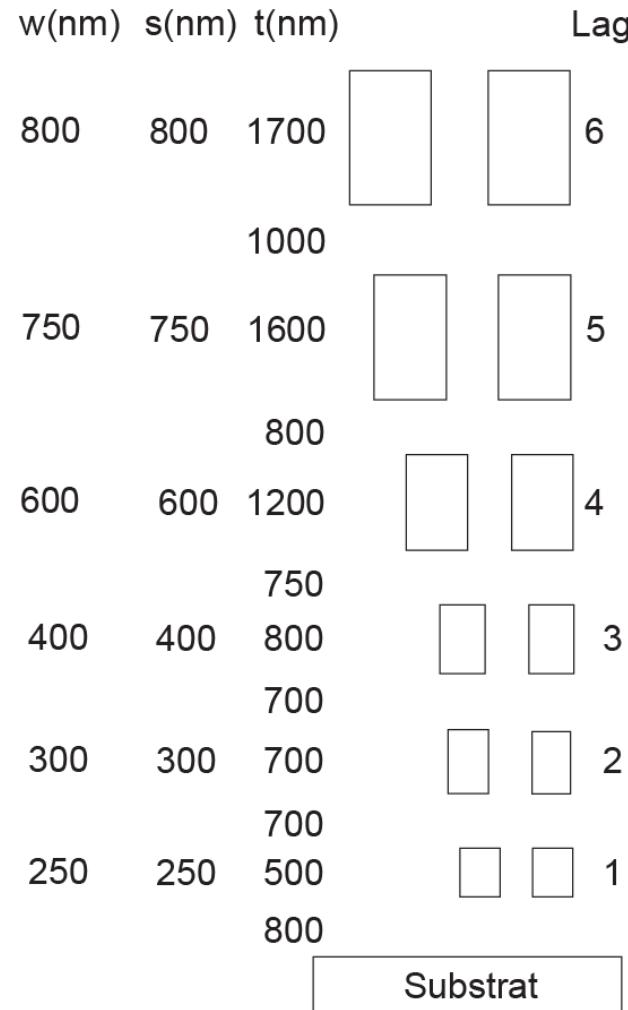


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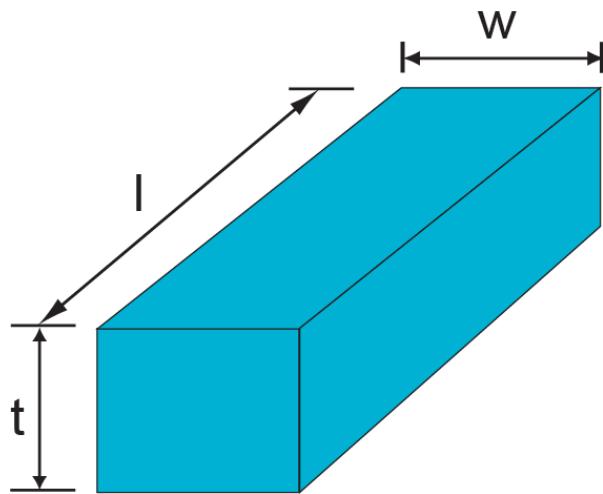
INF3400 Del 13 Teori Interkonnekt



Introduksjon

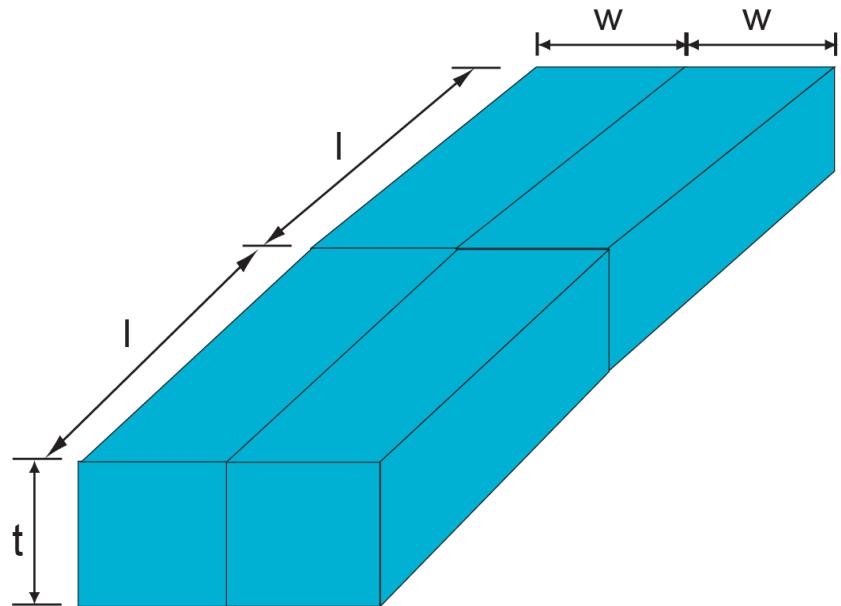


Motstand i interkonnekter



$$R = \frac{\rho}{t} \cdot \frac{l}{w}$$

$$R = R_{square} \frac{l}{w}$$



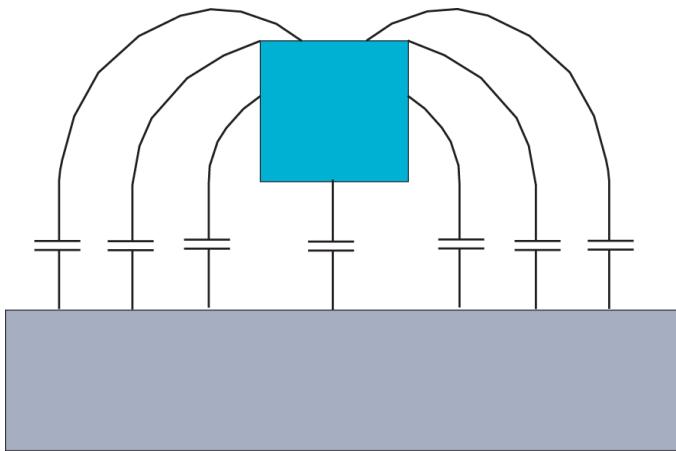
$$R = R_{square} \frac{2l}{2w}$$

$$= R_{square} \frac{l}{w}$$

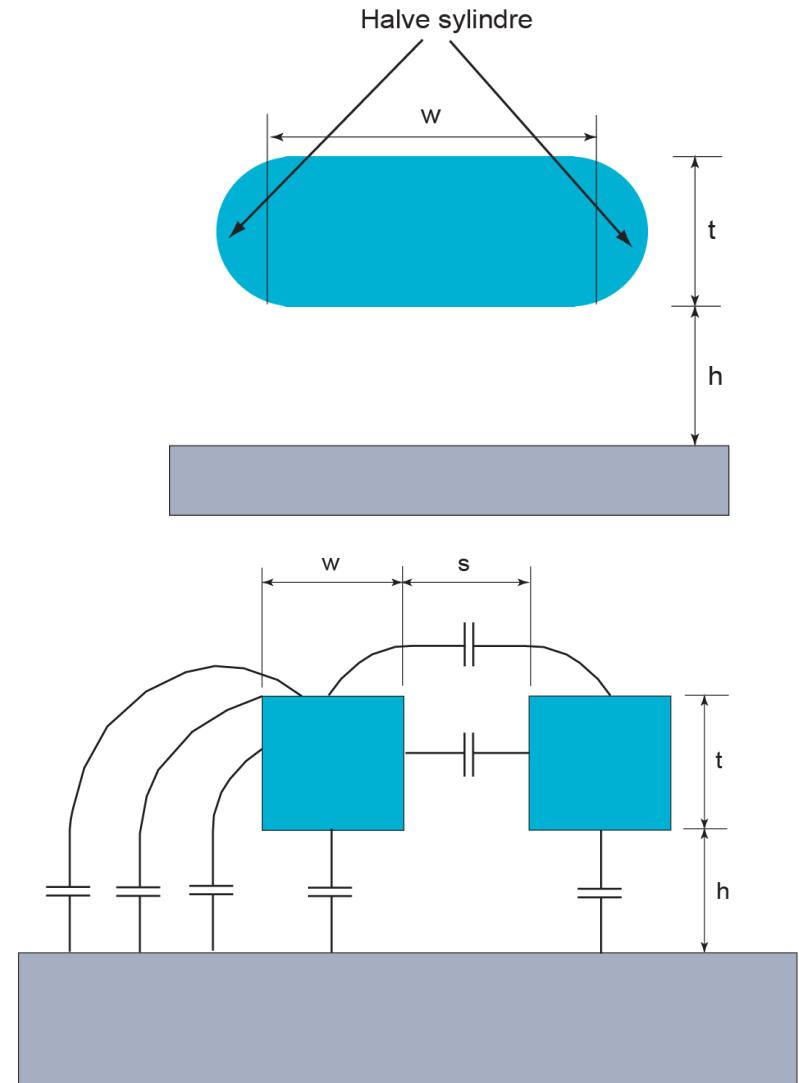
Kapasitans i interkonnekt

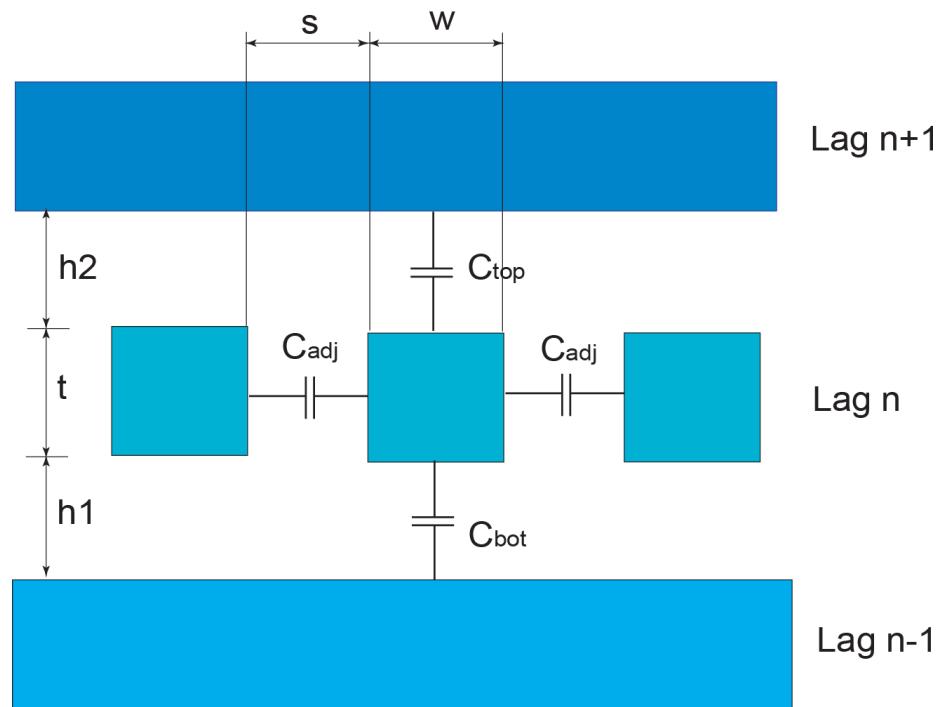
Kapasitans:

$$C = \frac{k\epsilon_0}{d}$$



$$C = \frac{\epsilon_{ox} \cdot w \cdot l}{h}$$

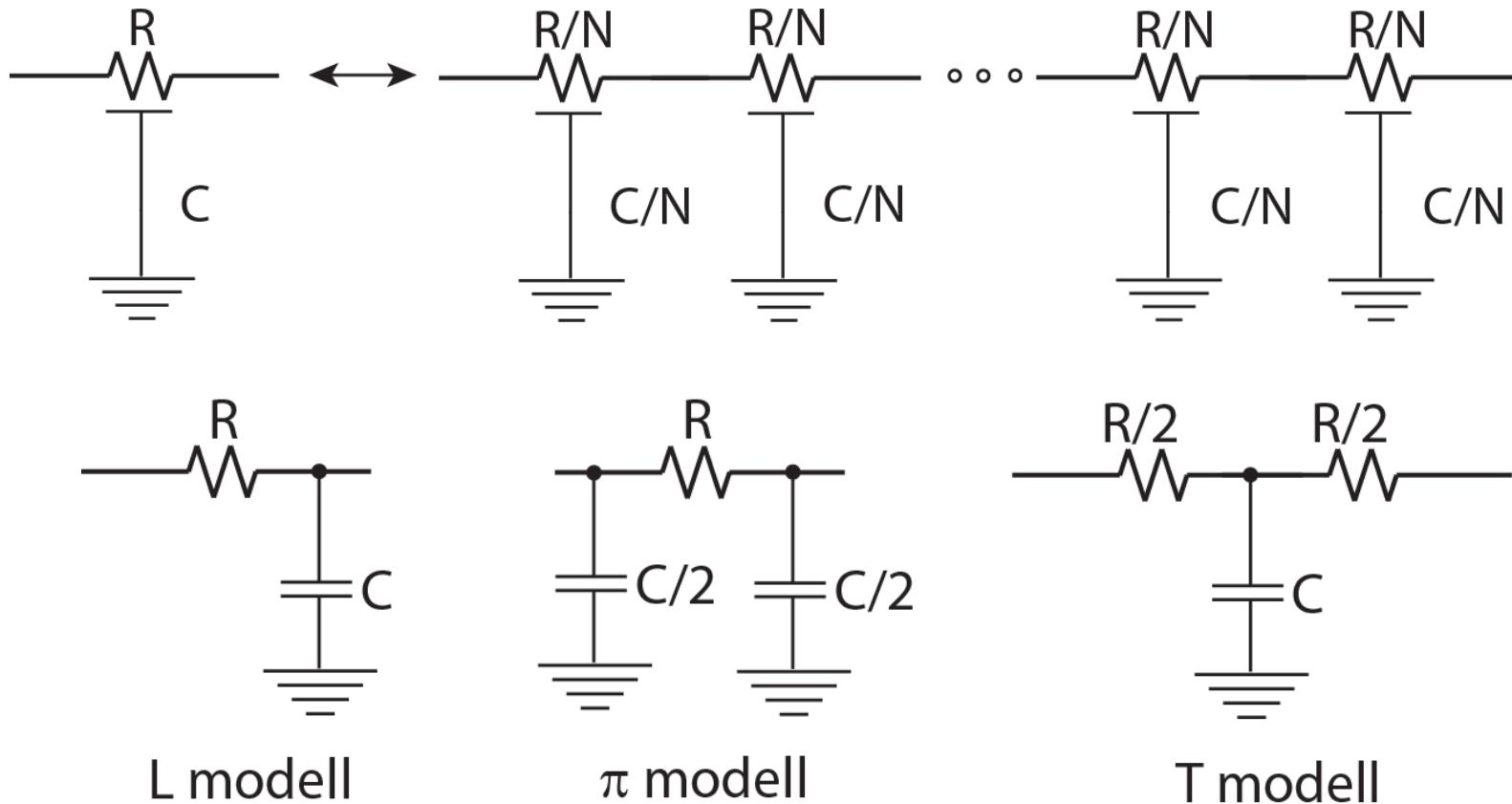




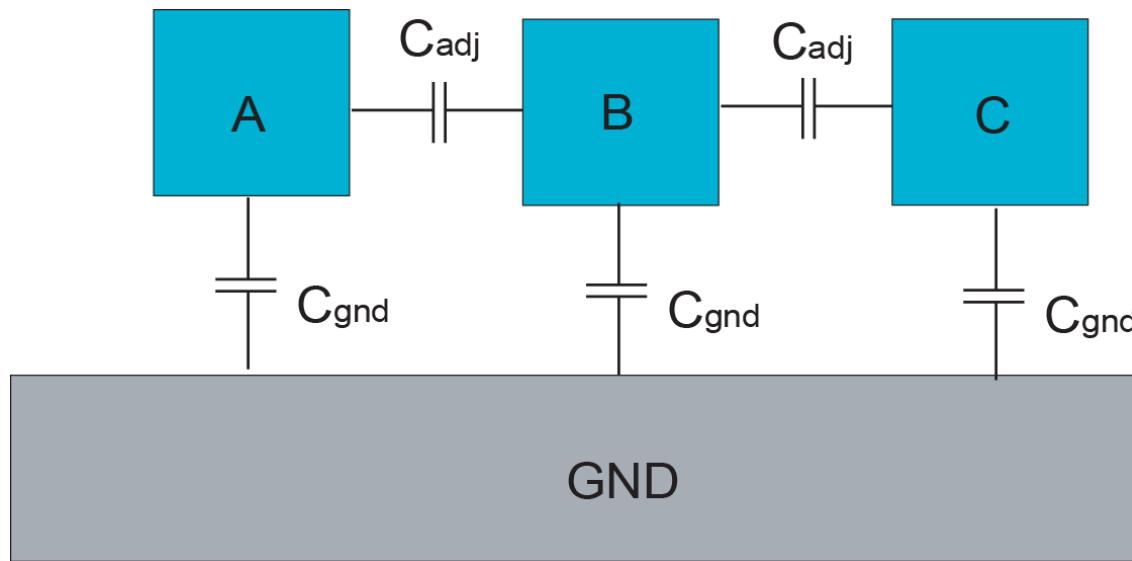
$$C_{gnd} = C_{bot} + C_{top}$$

$$C_{total} = C_{gnd} + C_{adj}$$

Forsinkelse i interkonnekt



Crosstalk



Ladning:

$$Q = C_{adj} \Delta V$$

Crosstalk støy:

$$\Delta V_{victim} = \left(\frac{C_{adj}}{C_{gnd} + C_{adj}} \right) \cdot \Delta V_{aggressor}$$

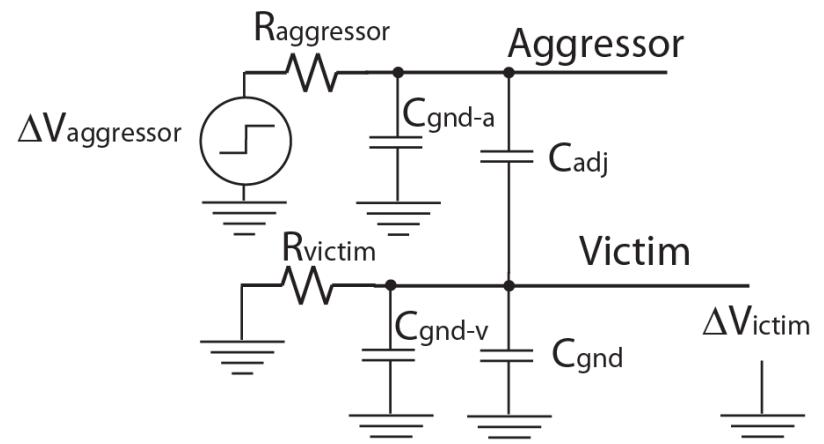
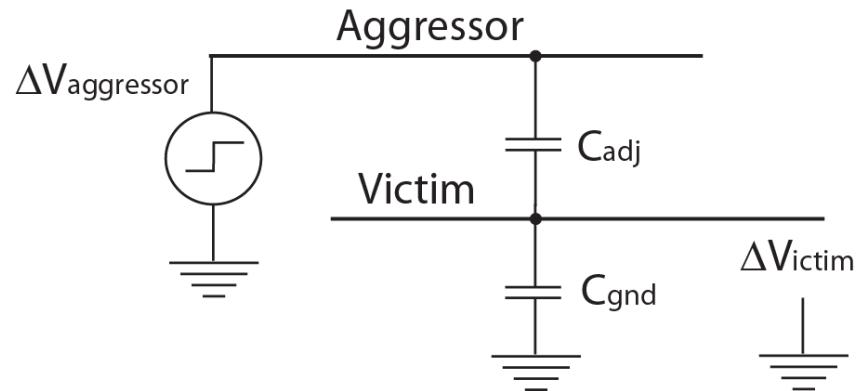
Drevne noder:

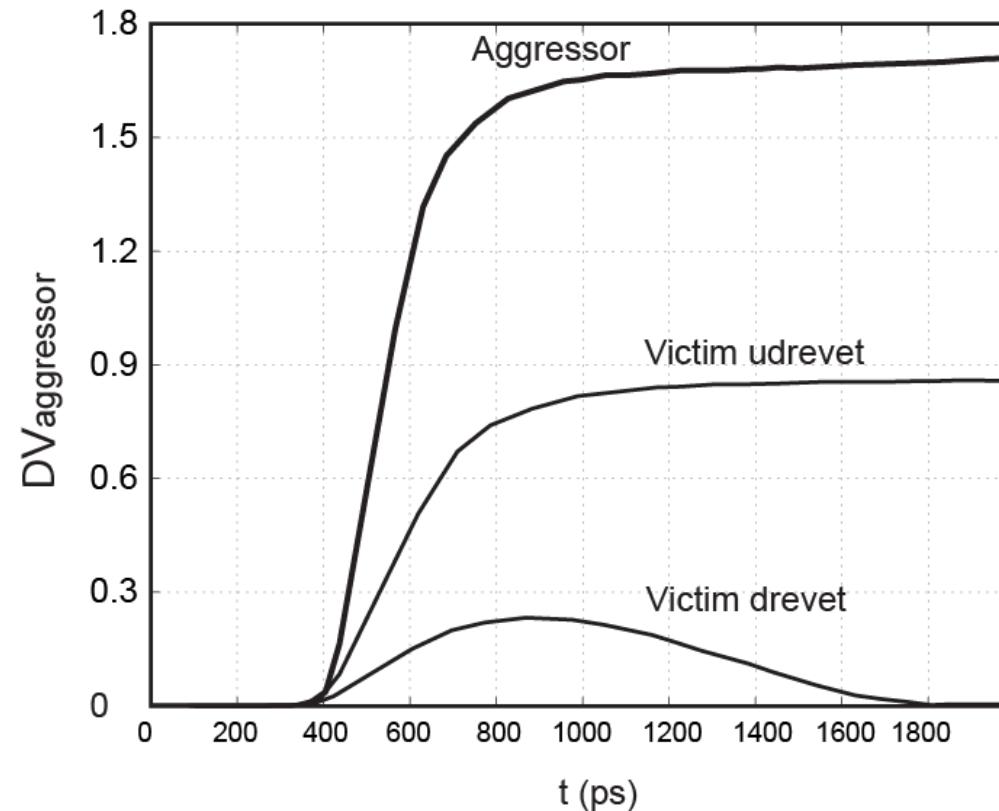
$$\Delta V_{victim} = \left(\frac{C_{adj}}{C_{gnd} + C_{adj}} \right) \cdot \left(\frac{1}{1+k} \right) \cdot \Delta V_{aggressor}$$

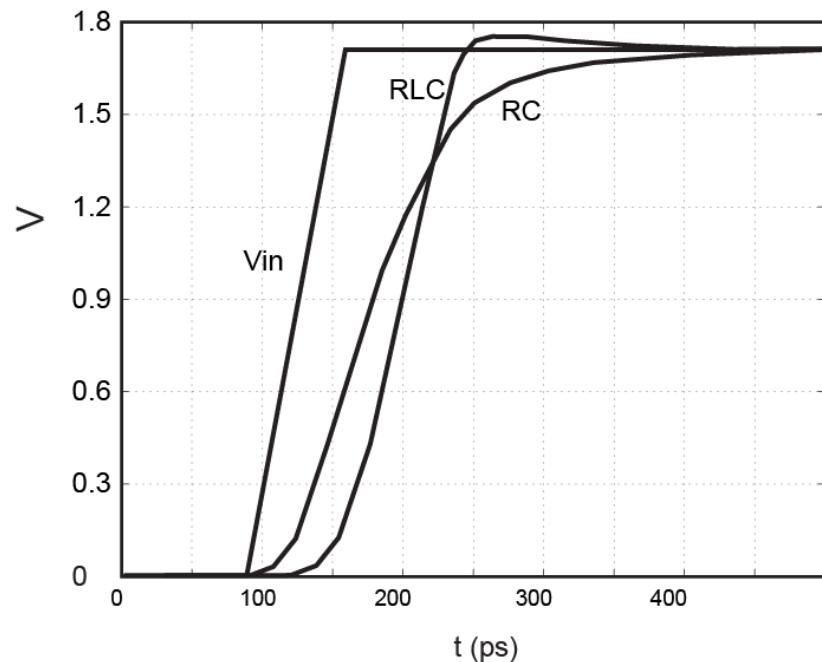
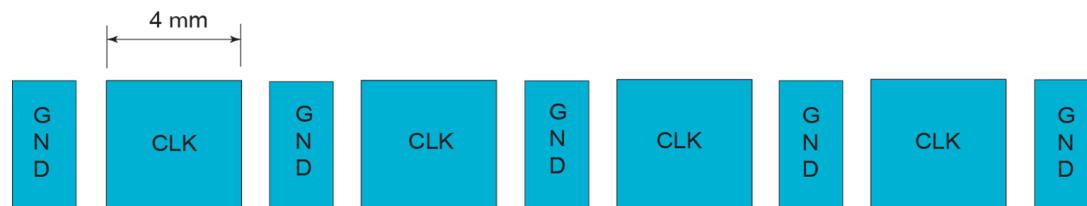
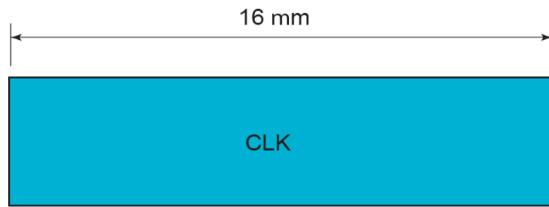
der:

$$k = \frac{\tau_{aggressor}}{\tau_{victim}}$$

$$= \frac{R_{aggressor}}{R_{victim}} \left(\frac{C_{gnd-a} + C_{adj}}{C_{gnd-v} + C_{adj}} \right)$$









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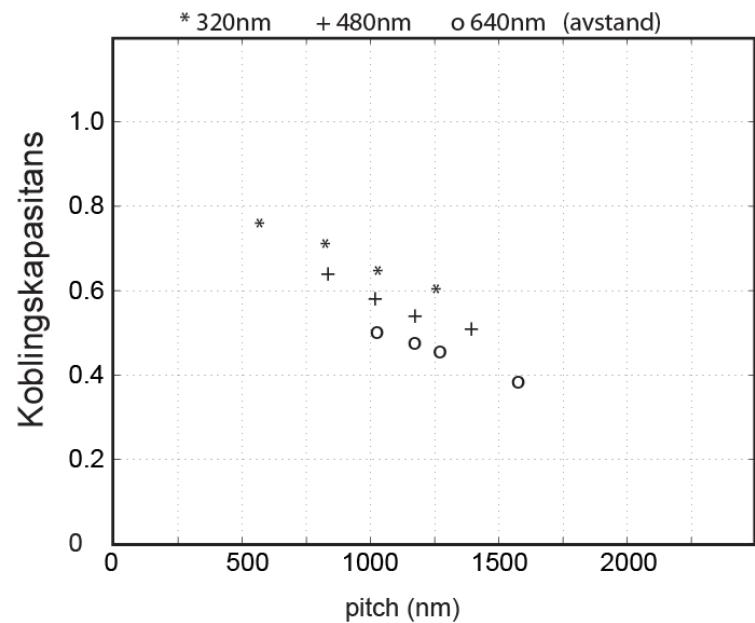
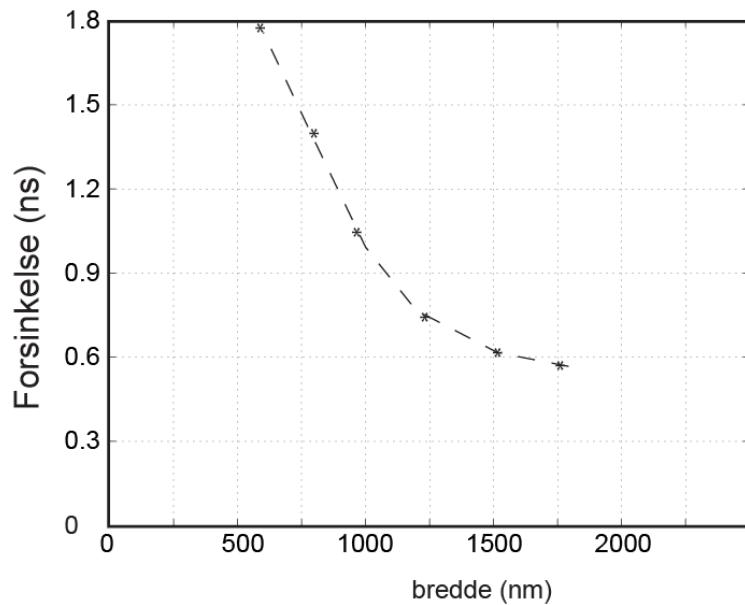
**INF3400 Del 14 Teori
Design av ledere og designmarginer**



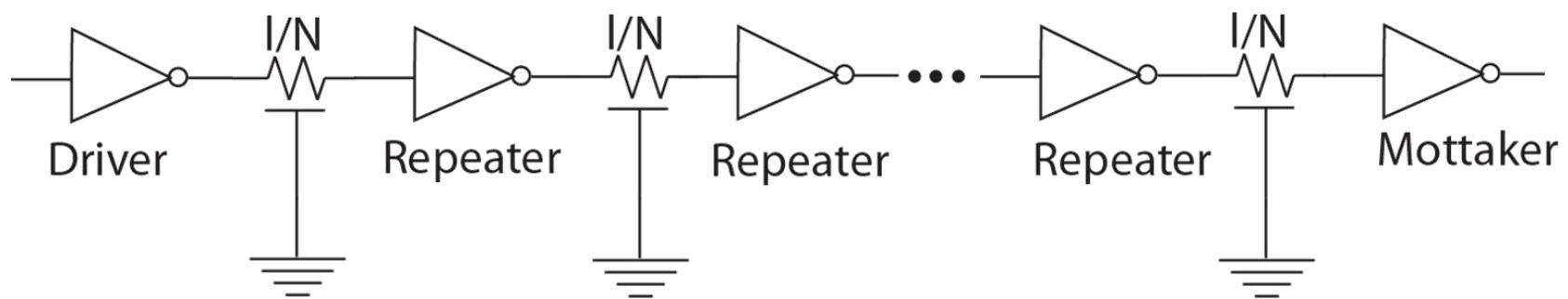
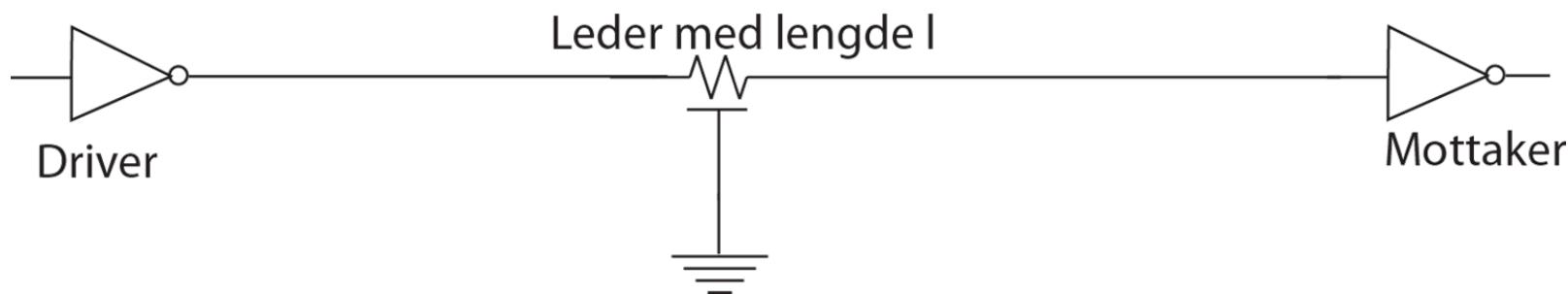
Bredde og avstand for ledere

Pitch:

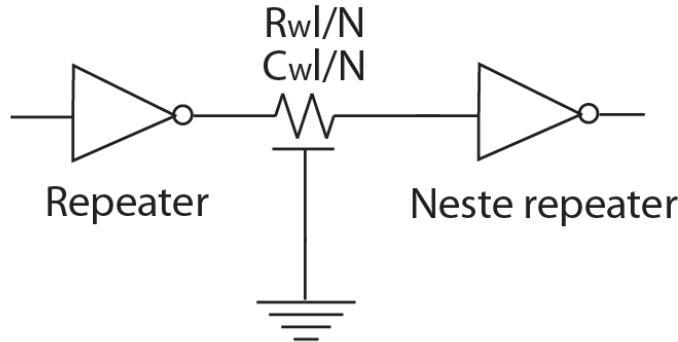
$$pitch = w + s$$



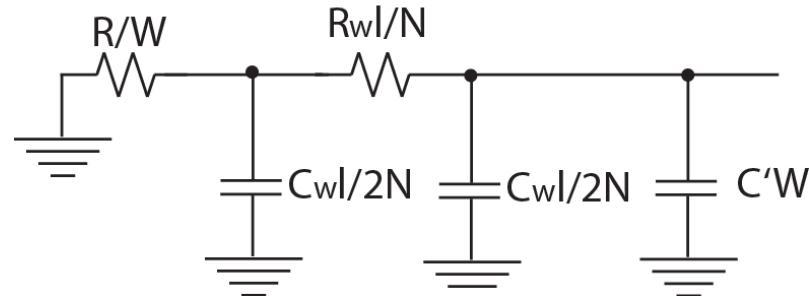
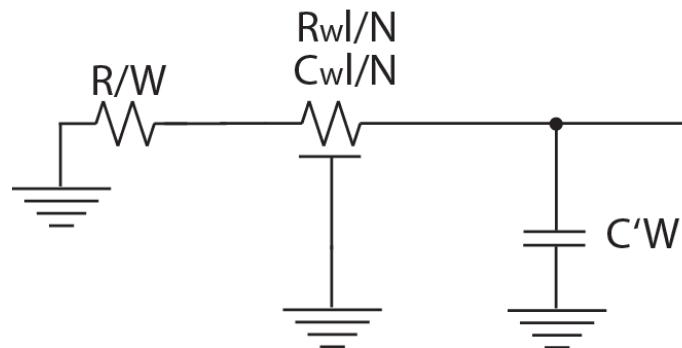
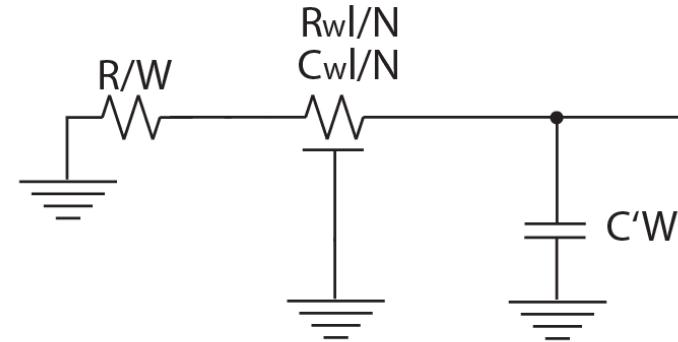
Repetere



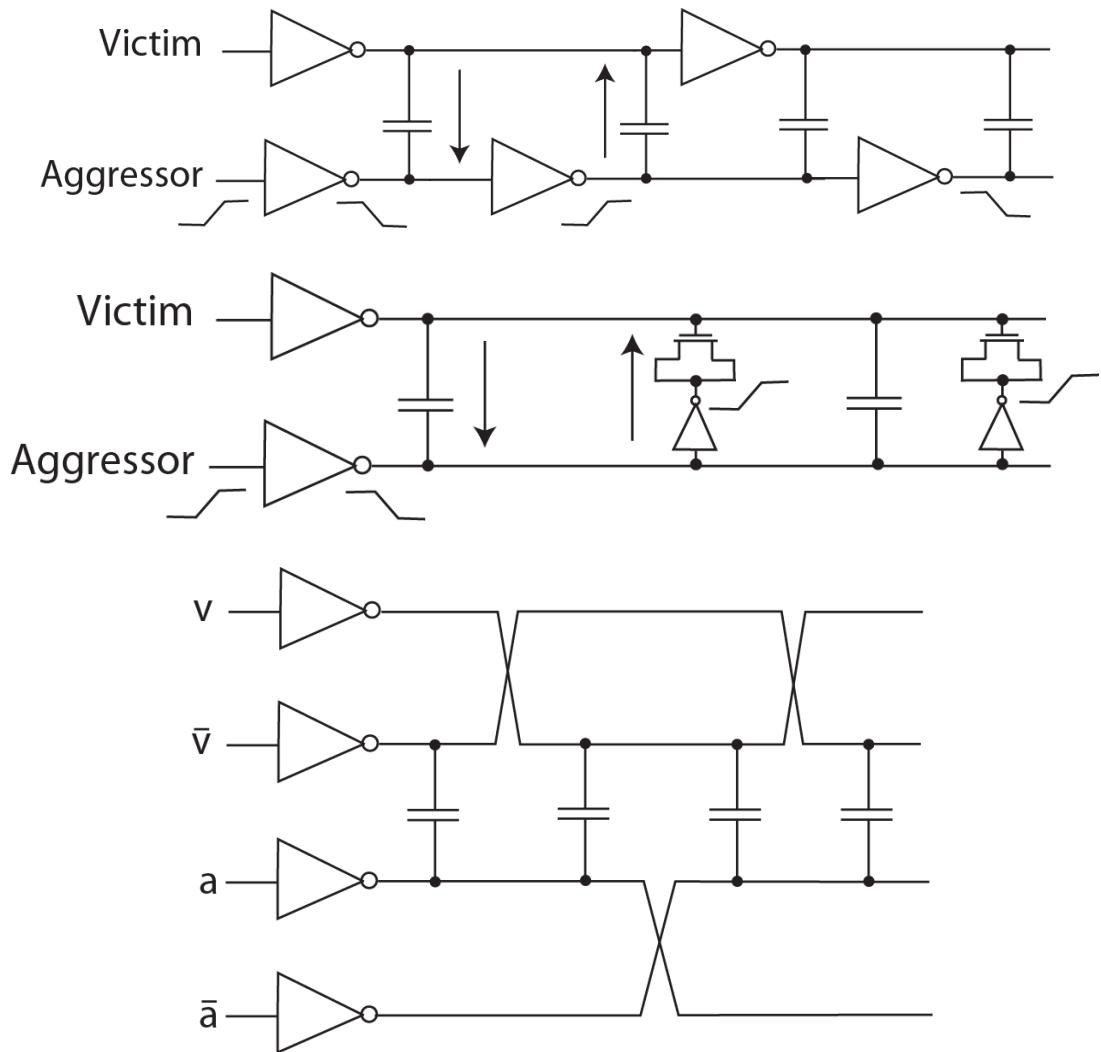
Modell for repeatere:



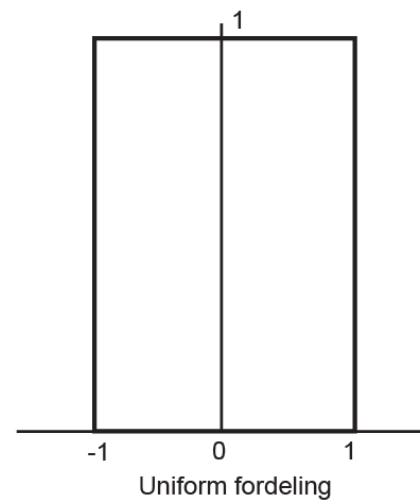
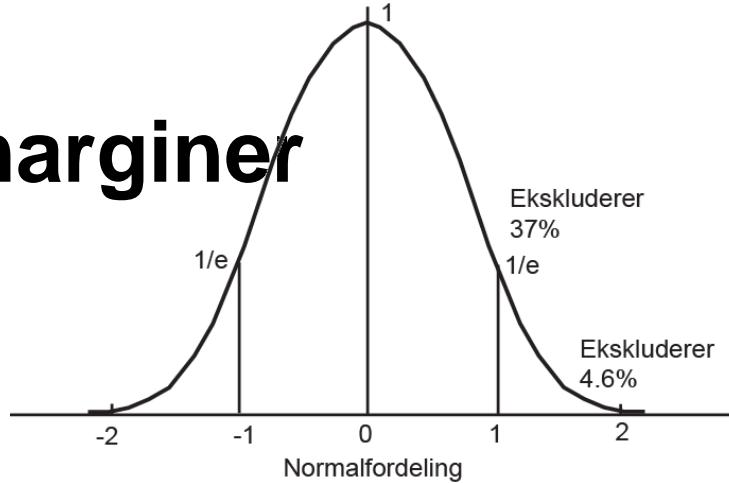
Elmore forsinkelsesmodell:



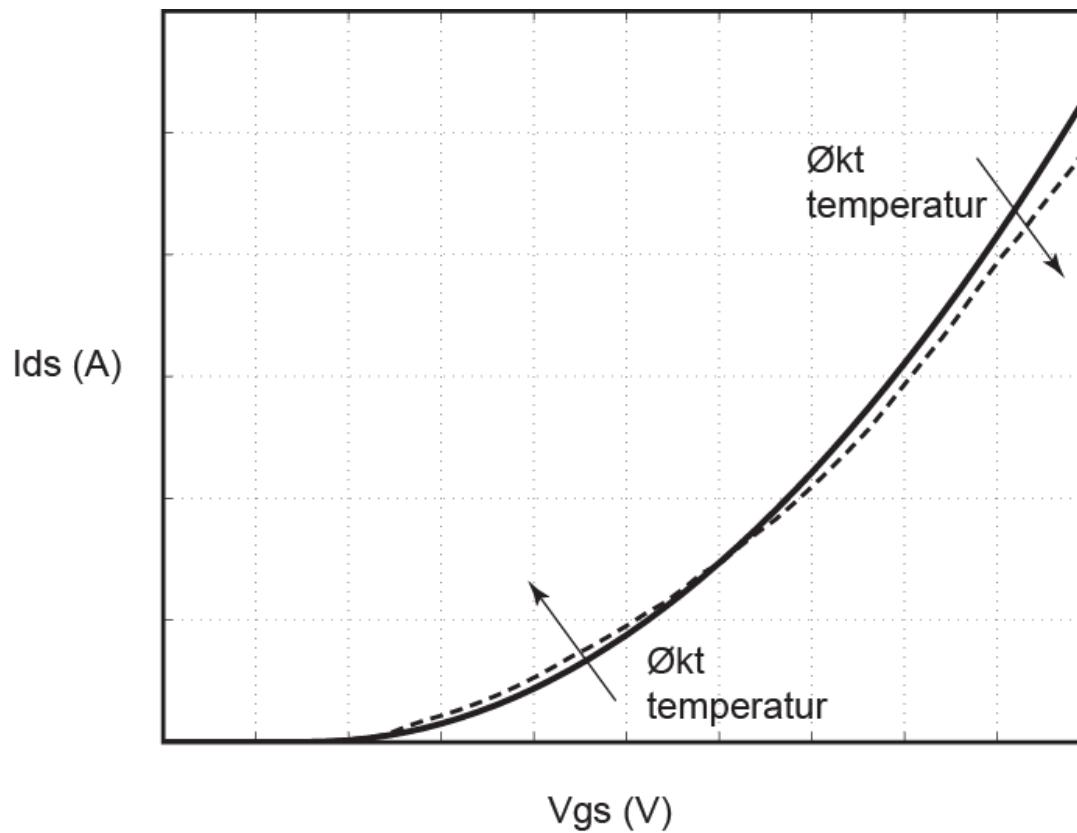
Kontroll av cross talk



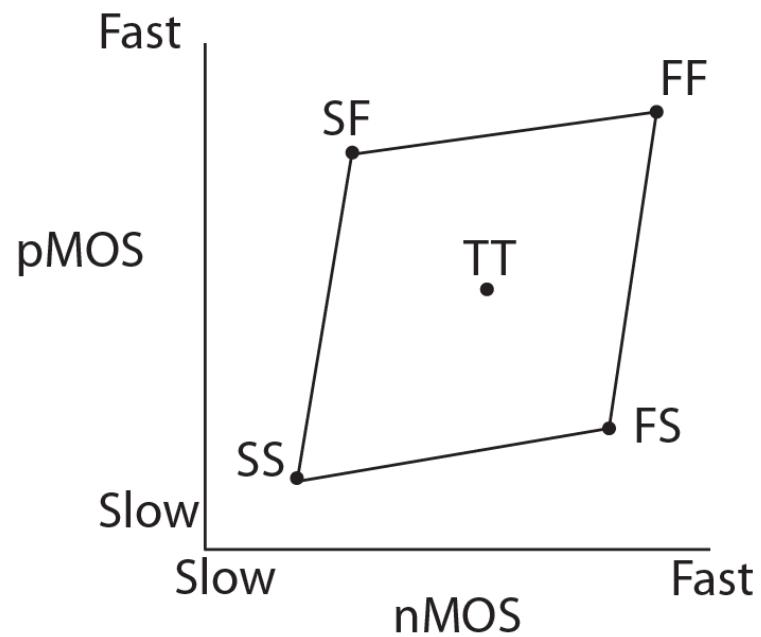
Designmarginer



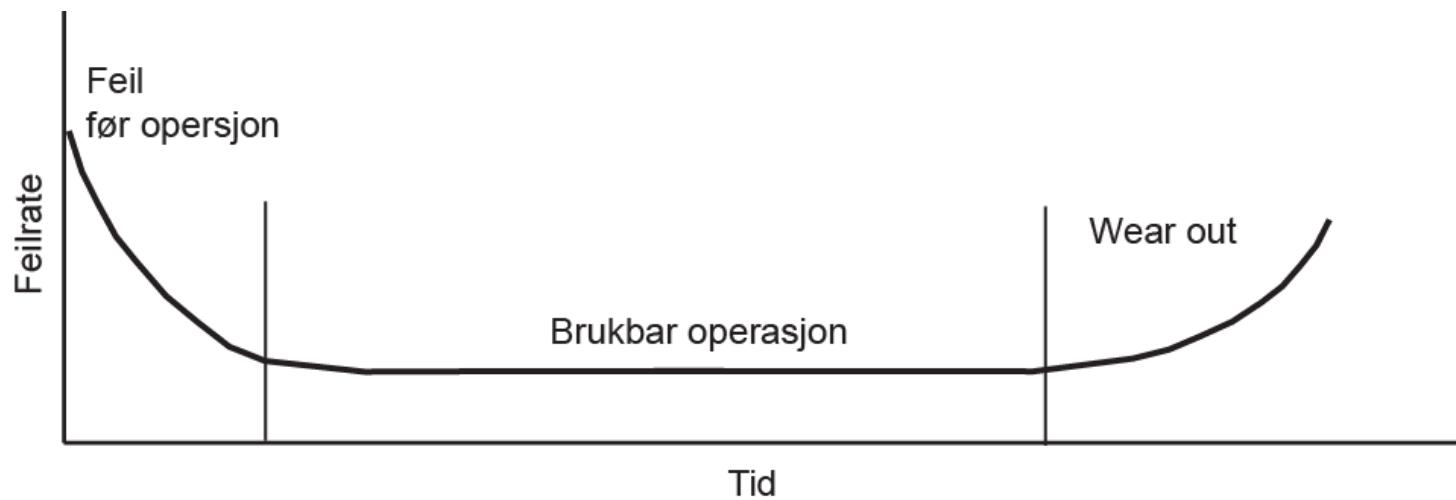
Temperaturavhengighet



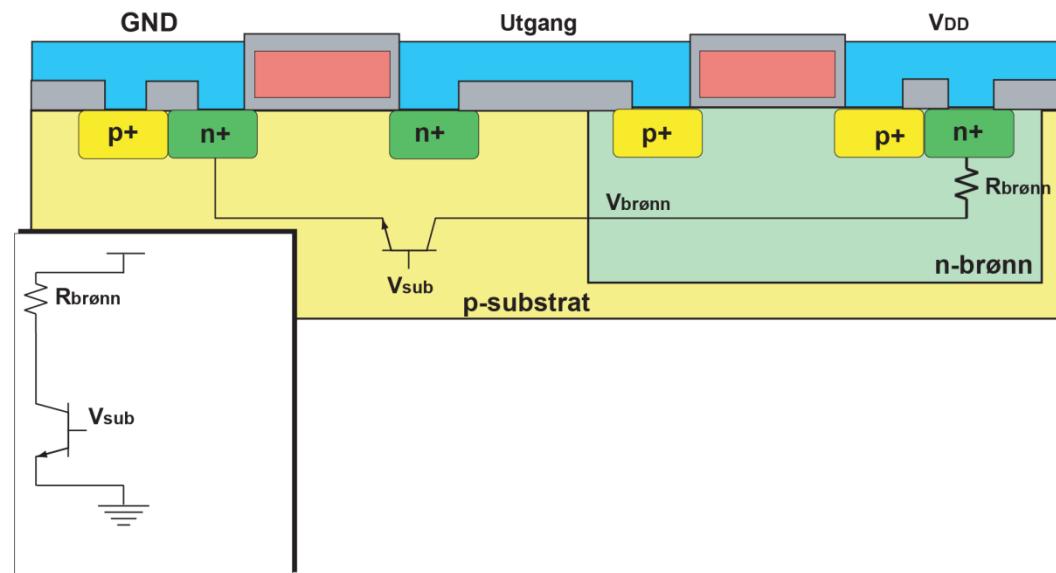
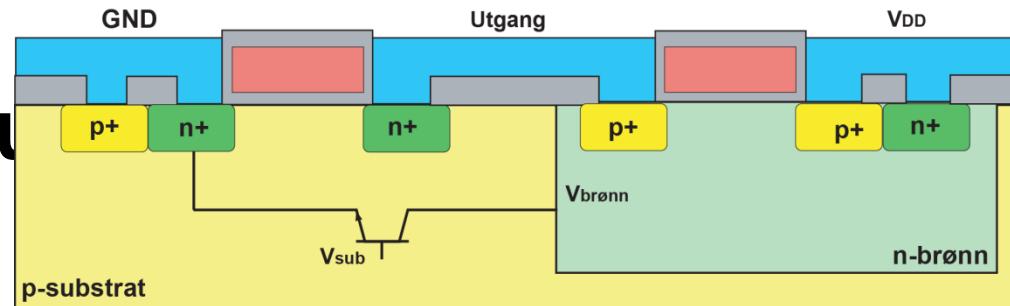
Designhjørner

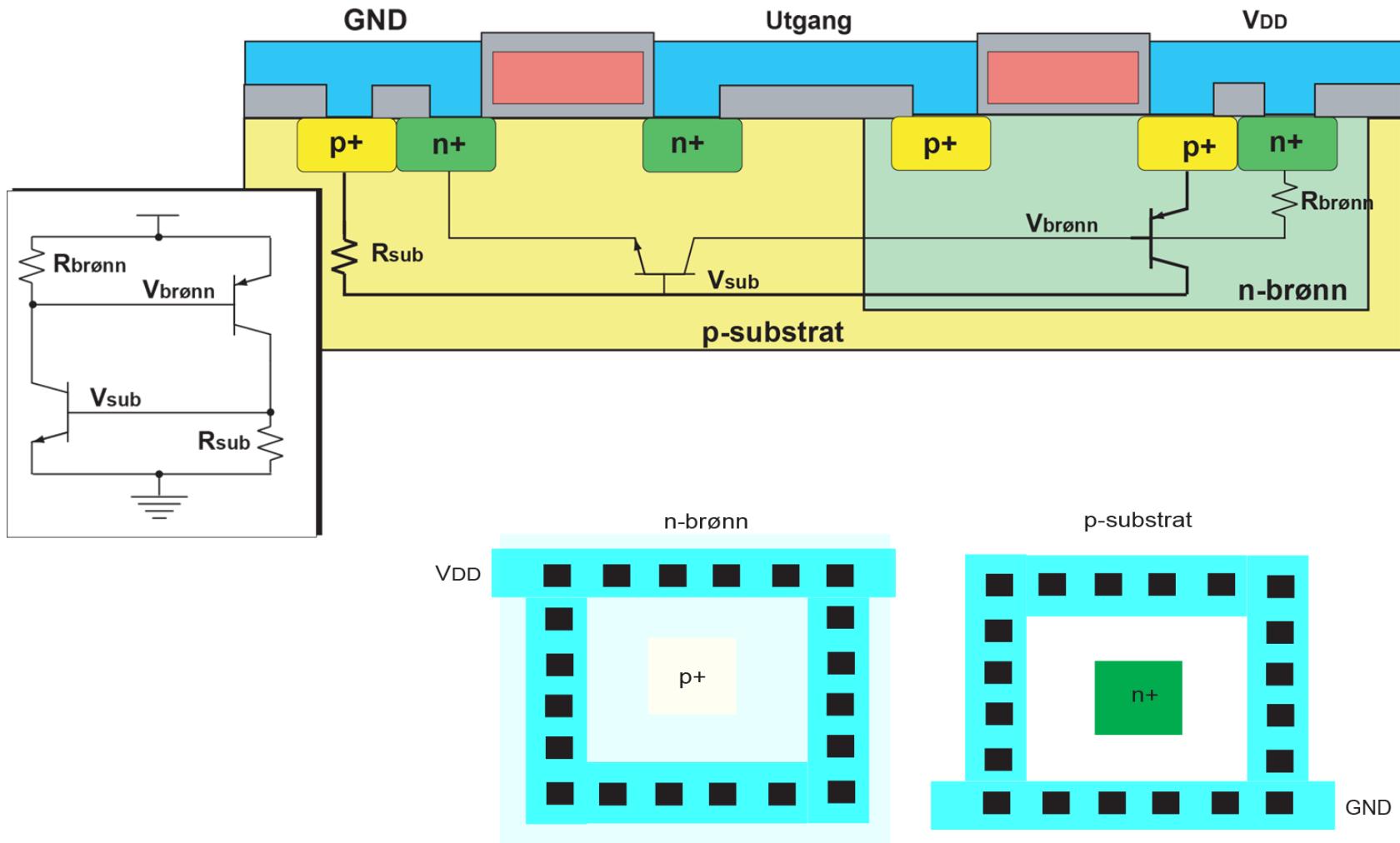


Pålitelighet



Latchup







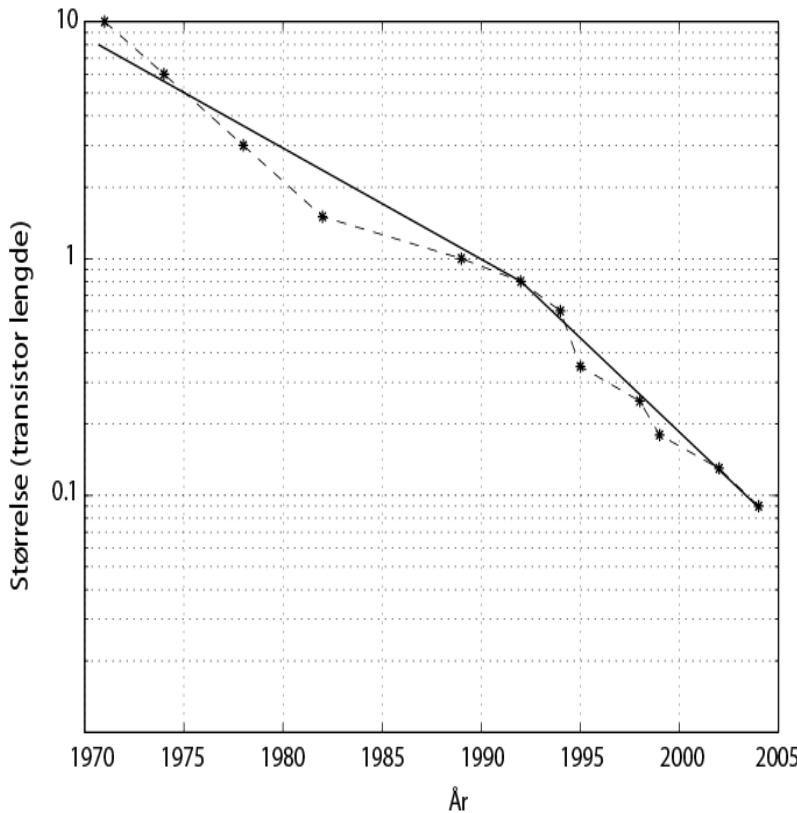
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**INF3400 Del 15 Teori
Avansert CMOS**

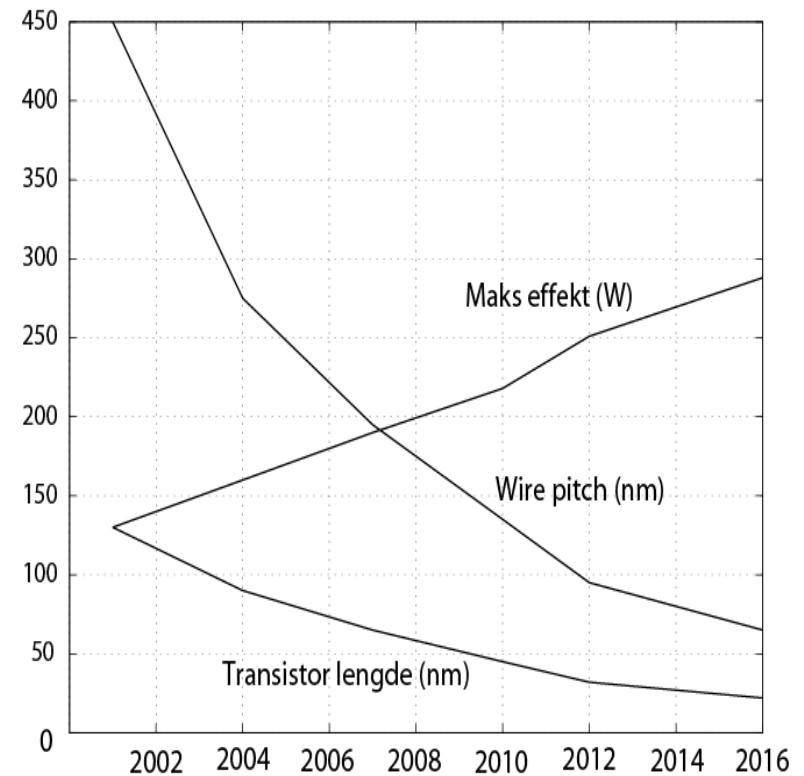


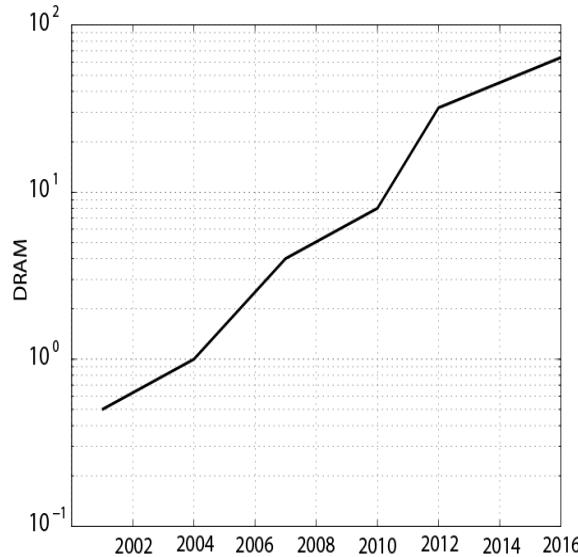
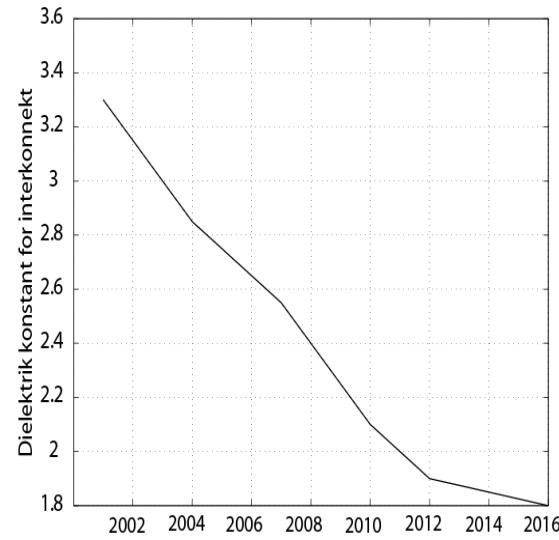
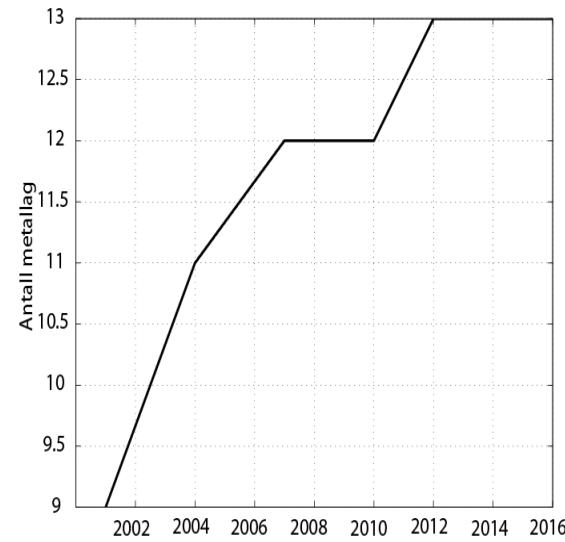
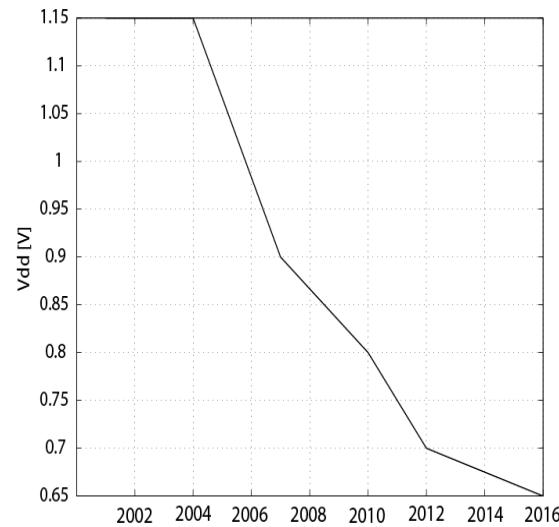
Hvordan er fremtiden for CMOS?

Introduksjonstidspunkt av ulike teknologier:

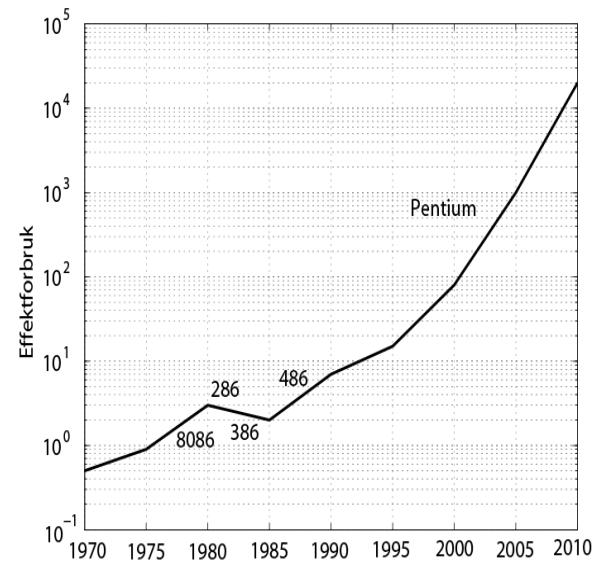
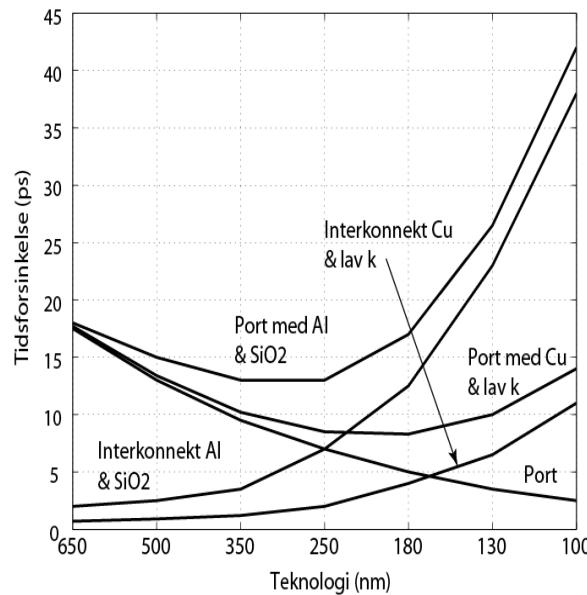
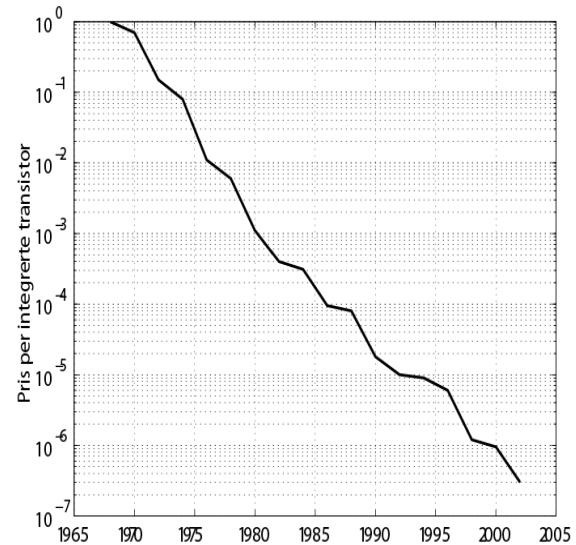
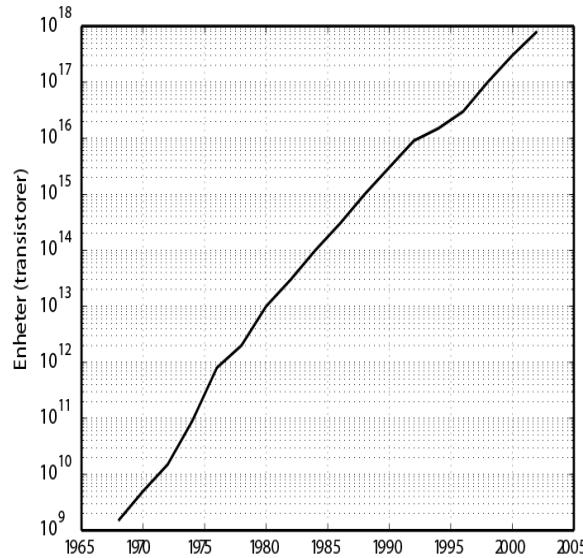


Transistor lengde, wire pitch og maks. effekt:





Designutfordringer

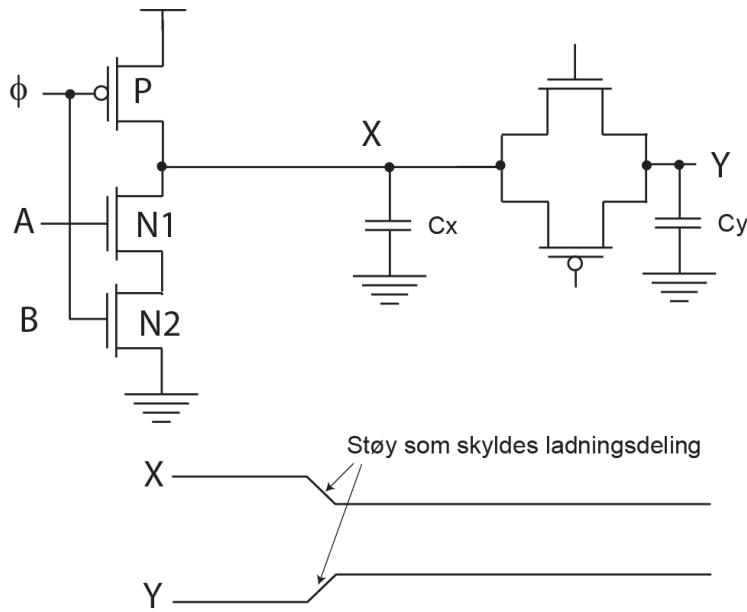


Lekkasje:

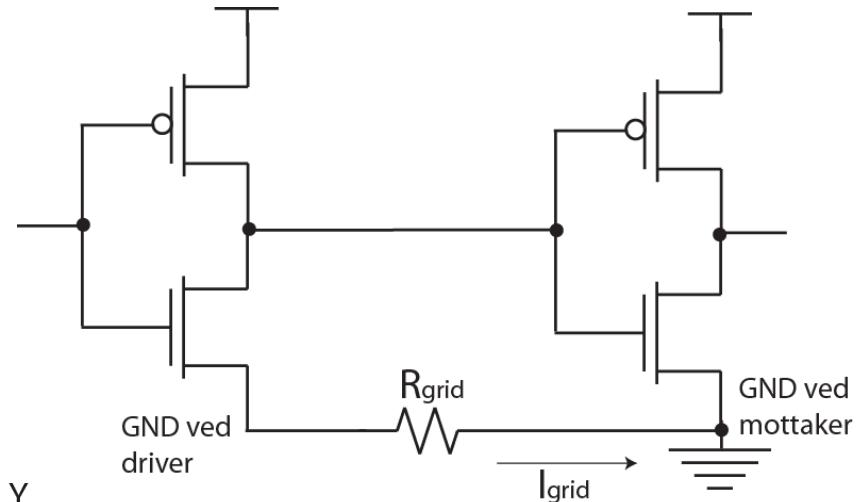
$$t = \frac{C_{node}}{I_{lekkasje}} \cdot \Delta V$$

$$\Delta V = \frac{I_{lekkasje}}{C_{node}} \cdot t$$

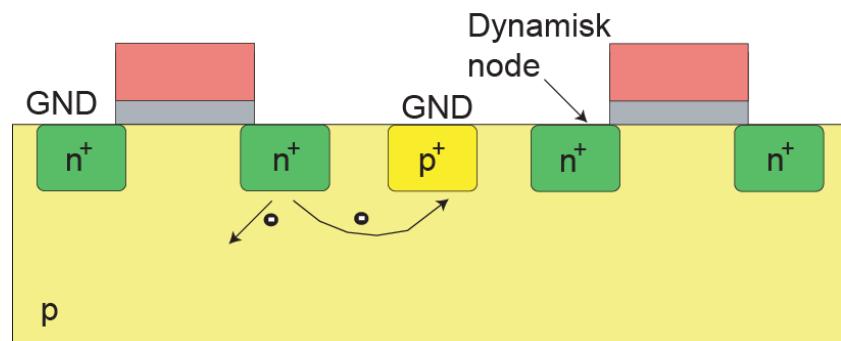
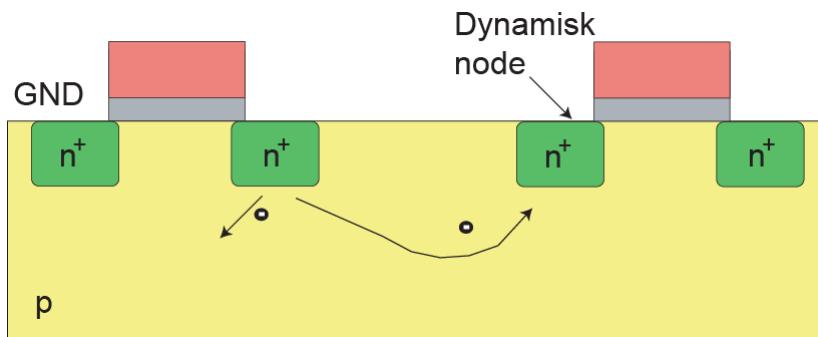
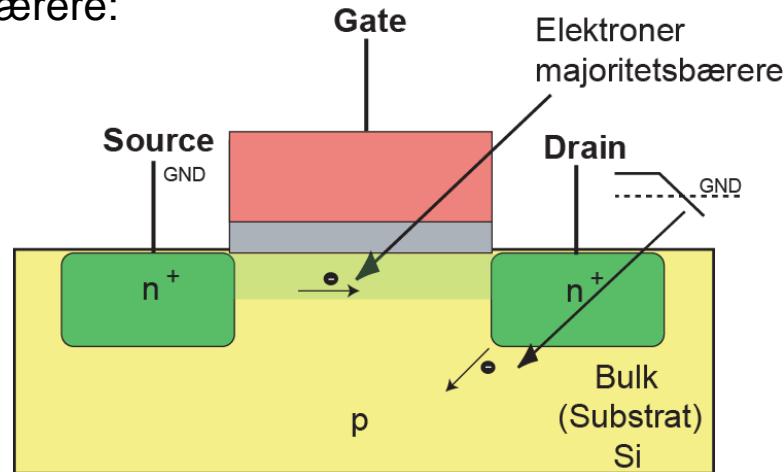
Støy pga ladningsdeling:



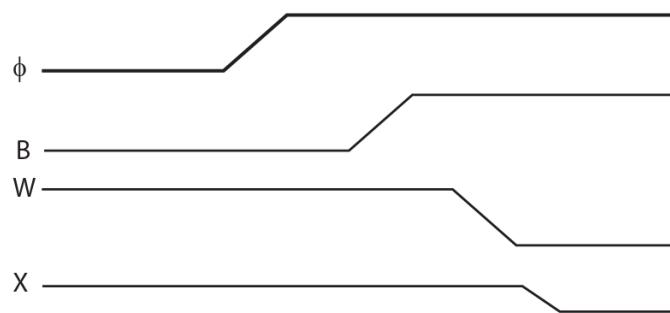
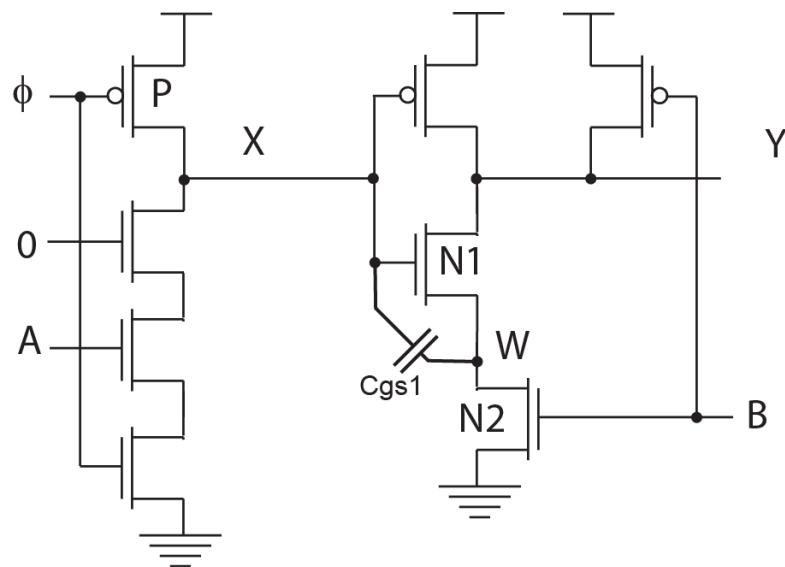
Støy på forsyningsspenningen:



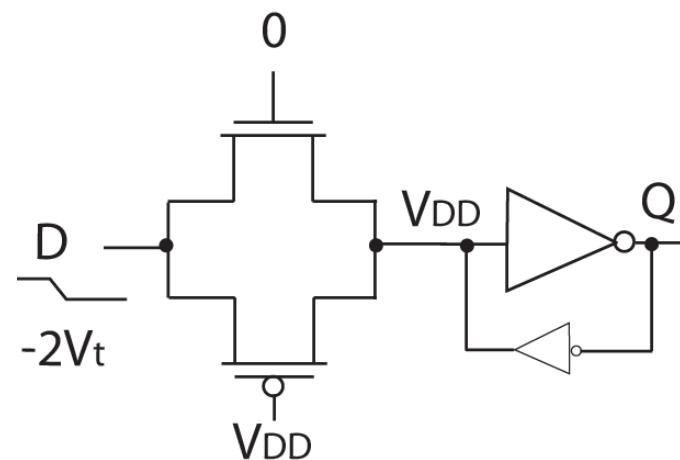
Injeksjon av minoritetsbærere:



Back-gate:



Følsomhet for støy I diffusjon:



Domino logikk:

1. Lekkasje av ladning.
2. Ladningsdeling.
3. Kapasitive koblinger.
4. Back-gate.
5. Injeksjon av minoritetsbærere.
6. Støy på spenningsforsyninger.