UNIVERSITY OF OSLO

Faculty of Mathematics and Natural Sciences

Exam in: INF4420 Projects in Analog / Mixed Signal CMOS
Construction.
Day of exam: Thursday, June the 5th, 2008.
Exam hours: 14:30 – 17:30.
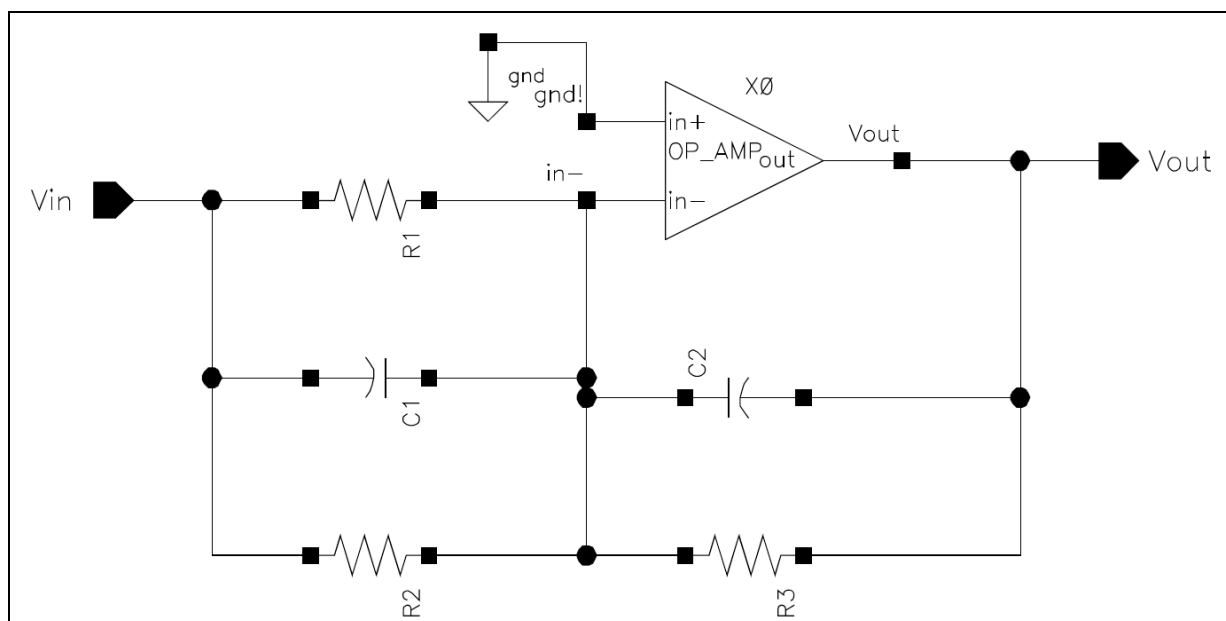**This examination paper consists of 5 page(s).**
Appendices: None.
Permitted materials: Any written material and calculator.

Make sure that your copy of this examination paper
is complete before answering.

1 a) (Weight 10 %)

An active-RC filter is depicted below. Draw the schematics for a Switched Capacitor ("SC") equivalent. Simplify the schematics, if possible.


1 b) (Weight 10 %)

Find a transfer function, $H(z) = Vout(z) / Vin(z)$, for the SC equivalent from problem 1 a).

2 a) (Weight 8 %)

A simplified circuit of a bandgap reference is shown below. Describe briefly which voltages that are generated on the base of the bipolar transistor shown, the output from the PTAT, the output from the

triangular block with "K" in it, and the output from the sum node. You may make a simple drawing to explain the concept. The figure depicts the same circuit as in figure 8.23 In the book by Johns & Martin.
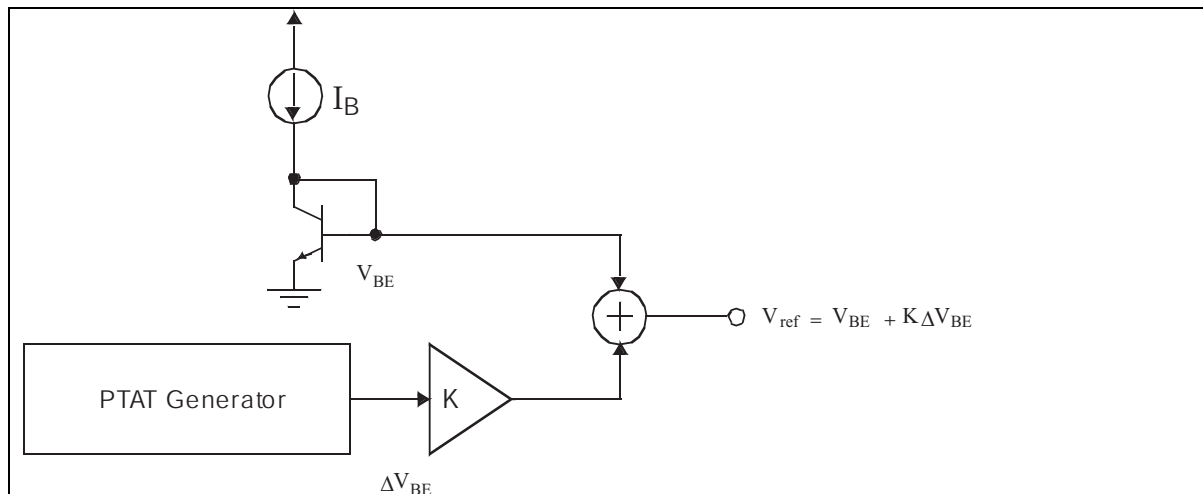
2 b) (Weight 8 %)

Assume that a bandgap reference of the same type shall be used at a temperature of 300 Kelvin. The PTAT depends on two base-emitter junctions, where the two bipolar transistors have emitter areas differing by a factor of 8. Let $V_{BE0\text{-}2} = 0.65$ V, $\Delta V_{BE} = -2$ mV / degree Kelvin, $V_{G0} = 1.18$ V and m = 2.3. The following, fundamental relationship, holds:

$$V_{ref} = V_{BE2} + K\,\Delta V_{BE}$$
$$= V_{G0} + \frac{T}{T_0}(V_{BE0\text{-}2} - V_{G0}) + (m-1)\frac{kT}{q}\ln\left(\frac{T_0}{T}\right) + K\frac{kT}{q}\ln\left(\frac{J_2}{J_1}\right)$$

Calculate K, under the given conditions.

3 a) (Weight 10 %)

A sampled signal is bandlimited to $f_0 = 22$ kHz. What is the sampling frequency, f_s, for an oversampling ratio ("OSR") of 128?
A 1-bit analog-to-digital converter ("ADC") has an inherent 6-dB SNR. Which maximum SNR is acquired by combining it with strict oversampling and an OSR of 128, if no noise shaping is used?
What is the maximum SNR in the similar case exploiting 2nd order noise shaping?
If a 1-bit ADC using 3rd order noise shaping has a maximum SNR of 125 dB for an OSR of 128, what is the expected maximum SNR if the OSR is reduced to 32?

3 b) (Weight 6 %)

Assume that a 1st order noise shaping modulator is considered for use in a battery driven hearing aid, being part of the sound processing signal path. Are you aware of any reasons for increasing the order of the modulator(s), instead?

4 a) (Weight 8 %)

A simple sample-and-hold ("S/H") circuit is shown in the schematics below. It is implemented in a standard 90 nm CMOS technology, having a supply voltage of 1.0 V. The clock signal ("clk") varies between 0 V and 1 V, while a sine wave varying between 0.3 V AND 0.5 V is connected to the input ("Vin"). Make a sketch depicting the two previously mentioned signals as well as the voltage across the hold capacitor ("Chld"), and the output ("Vout").
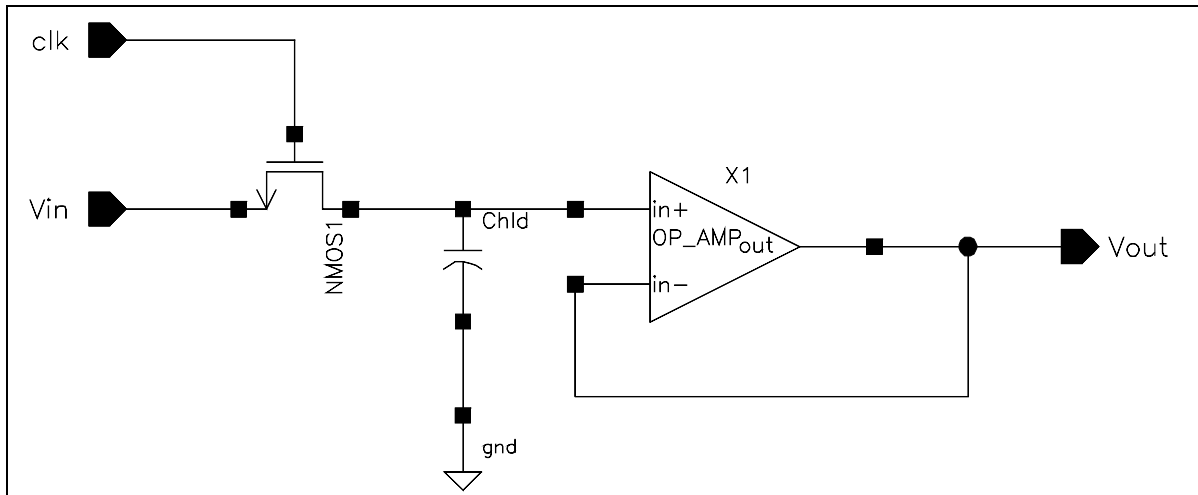

4 b) (Weight 12 %)

Consider the S/H from 4 a) and describe certain problems that may arise if Chld is made very small.

5 **a) (Weight 6 %)**

Assume that you are going to design an ADC (Analog-to-Digital Converter) for use in a sensor-node utilizing energy harvesting (containing no batteries), leading to a very strict budget with respect to average power consumption. This ADC should measure slowly changing physiological parameters for humans, needing a maximum resolution of 8 bits ("Effective Number of Bits" ; ENOB). What is most likely to be the best choice among a FLASH ADC or an integrating ADC? Please explain.
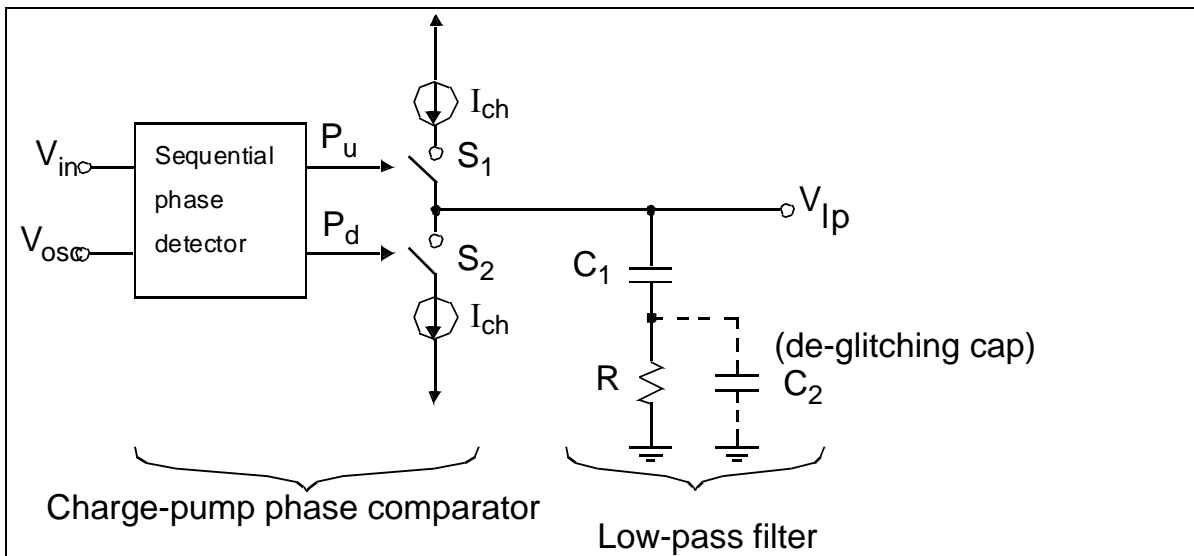
5 b**) (Weight 6 %)**

Sampling in the frequency domain, under two different basic conditions, is depicted below. Could the situation in the lower half of the picture represent a problem ($f_s/2$, f_s, and f is written along the horisontal lines.)? Please explain.

Figure 3.6
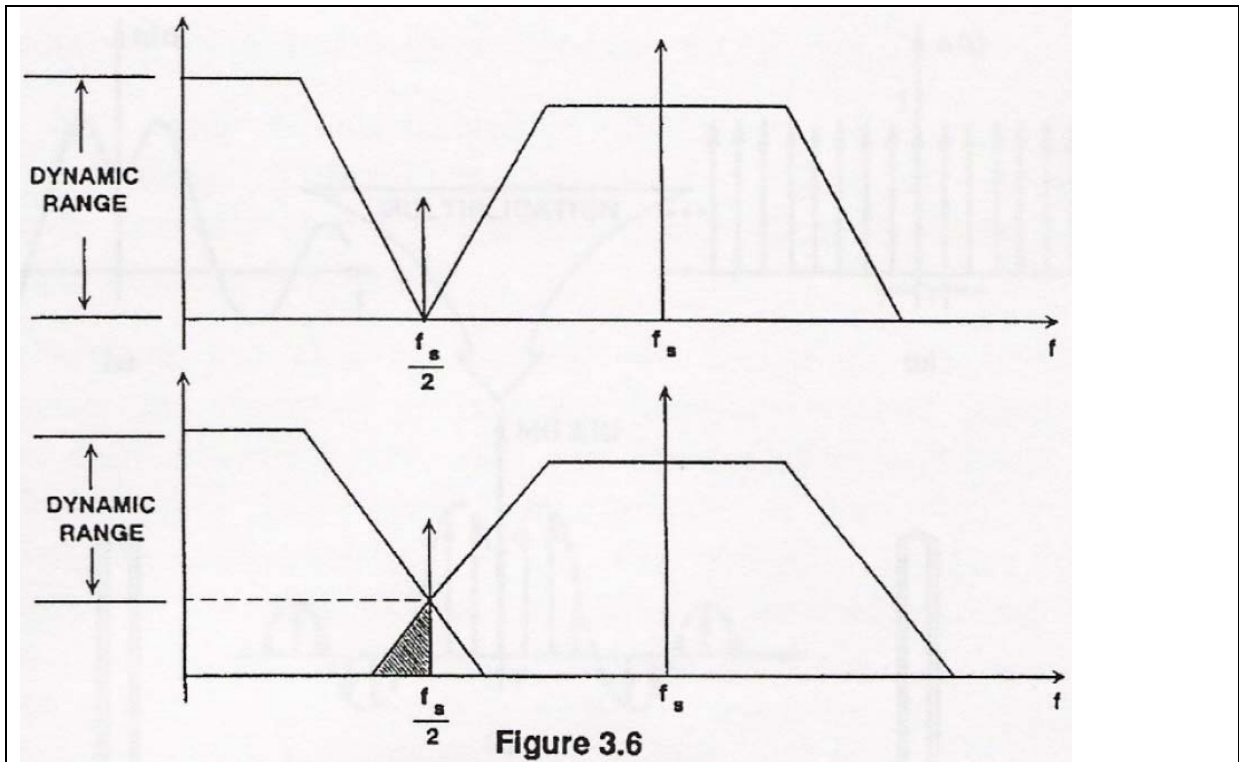
6 a) (Weight 8 %)

A ring oscillator consisting of inverters has it's supply voltage increased from 1.0 V to 1.2 V. What is the resulting expected increase in it's oscillating frequency?
Using fully differential inverters would improve the power supply rejection and lead to a more stable circuit. Can you imagine any negative effects of changing the simple inverter based ring oscillator for a differential solution?

6 b) (Weight 6 %)

How would you choose the Q-factor in a PLL (to obtain a maximally flat group delay) given that the architecture is a charge-pump PLL with a deglitching capacitor in the loop-filter, as shown above? What is most likely the value of C_1 if the "de-glitching" capacitor, C_2, was choosen to be 1 pF?

Good luck!