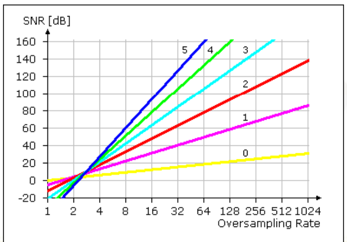
Last time – and today, Tuesday 16th of March:

Last time:
- 13.1 Integrating Converters
- 13.2 Successive-Approx. Converters
- 13.3 Algorithmic (or cyclic) A/D Converters
- 13.4 Flash (or parallel) converters
- 13.5 Two-Step A/D converters
- 13.8 Pipelined A/D Converters
- 13.9 Time-Interleaved A/D Converters

Today – from the following chapters:
- 13.6 Interpolating A/D Converters
- 13.7 Folding A/D Converters
- 14.1 Oversampled converters



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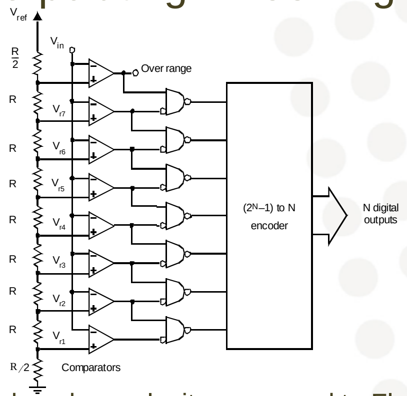
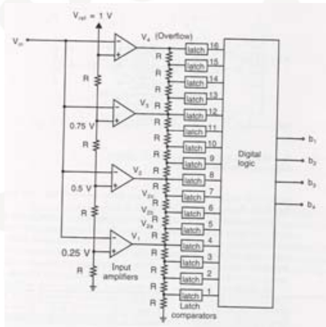
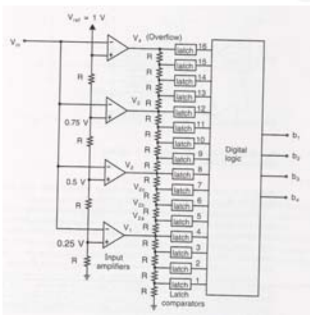
Interpolating ADCs. Rightmost interpol.=4 (1/4)

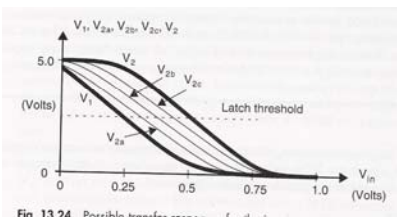




- Reduced complexity compared to Flash ADCs → reduced input capacitance and slightly reduced power.
- In the mathematical subfield of numerical analysis, **interpolation** is a method of constructing new data points within the range of a discrete set of known data points.

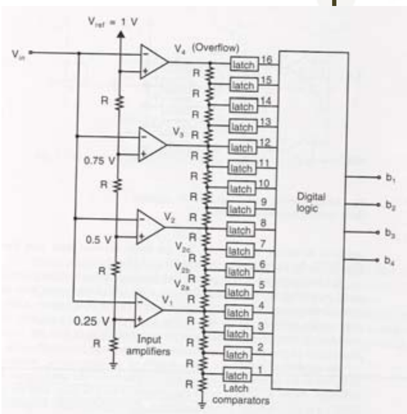
Interpolating ADCs (2/4)

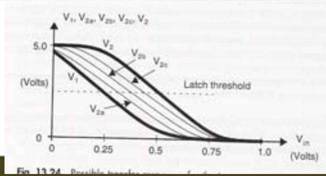




- Uses input amplifiers behaving as linear amplifiers near their threshold voltages, allowed to saturate for moderately large input signals
- Thus "noncritical" latches need only determine the sign of the amplifier outputs

Interpolating ADCs (3/4)





- Amplifier outputs V_1 and V_2 as well as their interpolated values are shown lowermost (fig. 13.24)
- The reference points created from interpolated values (for example V_{2a}, V_{2b}, V_{2c}) have latches potentially triggering in order, for increasing (or decreasing) input.
- For good linearity the interpolated signals need only cross the latch threshold at the correct points

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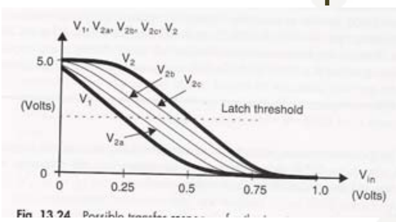
Interpolating ADCs (4/4)



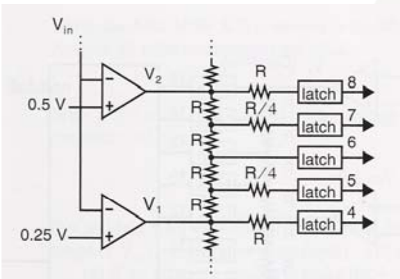


Fig. 13.25 Adding series resistors to equalize delay times to the latch comparators.

- To achieve good linearity V_1 and V_2 need to be linear between their own thresholds. In figure 13.24 this linear region corresponds to $0.25 < V_{in} < 0.5$ (horizontally)
- For fast operation the delays to each of the latches must be made to equal each other as much as possible. In fig. 13.25 this is done using resistors.

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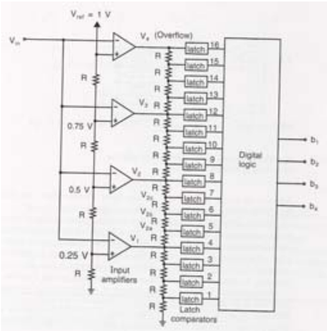
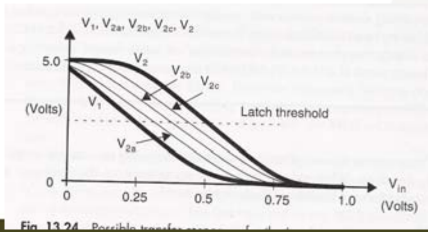
Example, based on Fig. 13.23 (1/2)





- Vin = 0.4 V, gain of -10, logic levels of 0 and 5 volts. →

- V4 = 5 V
- V3 = 5 V
- V2 = 3.5 V
- V1 = 1.0 V

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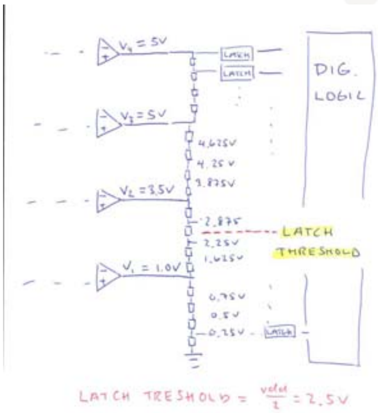
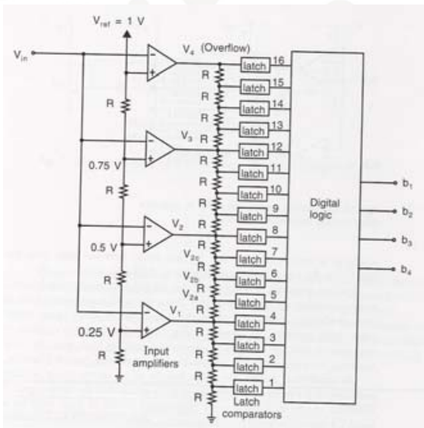
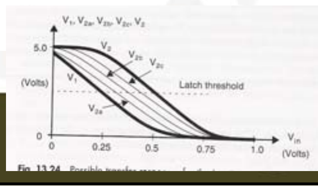
Example – interpolating ADC (2/2)







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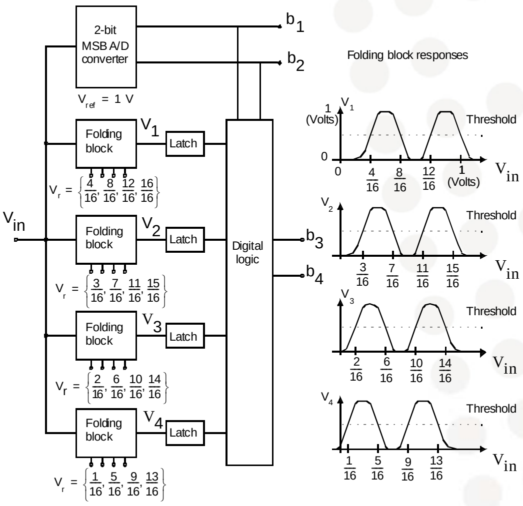
Folding A/D Converters (13.7)



- The number of latches is reduced compared to the interpolating ADC, and even more from FLASH
- The figure shows a 4 bit converter with folding rate of 4
- A group of LSBs are found separately from a group of MSBs.
- The MSB converter determines whether the input signal, V_{in}, is in one of four voltage regions (between 0 and ¼, ¼ and ½ , ½ and ¾ , or ¾ and 1)
- V_1 to V_4 produce a thermometer code for each of the four MSB regions

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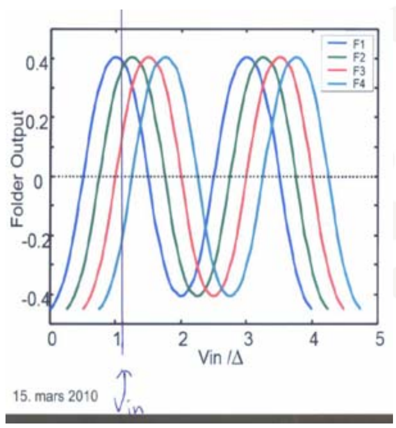
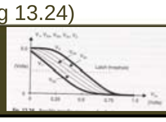
Similar to folding block responses on previous slide..



- Bipolar folder outputs
- Ex: Input 1.05:
- F1 > threshold=0 -> ”1”
- F2 > threshold=0 -> ”1”
- F3 > threshold=0 -> ”1”
- F4 < threshold=0 -> ”0”
- Thermometer code produced for each of the four MSB regions (between 0 and ¼, ¼ and ½ , ½ and ¾ , or ¾ and 1 for previous slide)
- (in certain respects related to interpolation in Fig 13.24)



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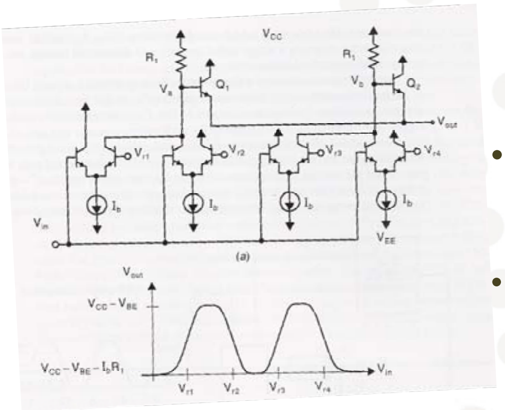
Folding block with a folding rate of four



- Input-output response for the cross-coupled differential pair is shown lowermost
- Vout is low if, and only if, both V_a and V_b are low, otherwise high
- The output from a folding block is at a much higher frequency than the input signal, limiting the practical folding rate.
- Differential solutions in practice

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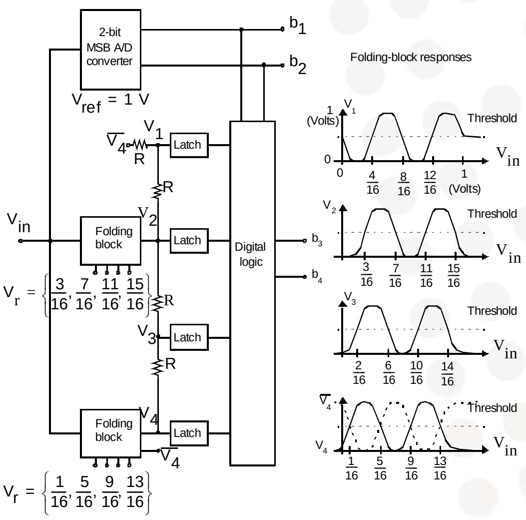
Folding and Interpolating ADC



- By introducing interpolation, the number of folding blocks is reduced
- Input capacitance is reduced (if both folding and interpolating is combined)
- Folding-rate of four and interpolate-by-two
- (Literature references on page 523)

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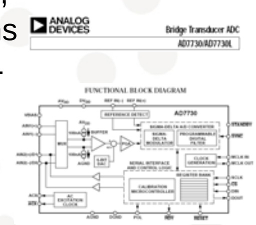
Interpolating and folding and interpolating ADCs

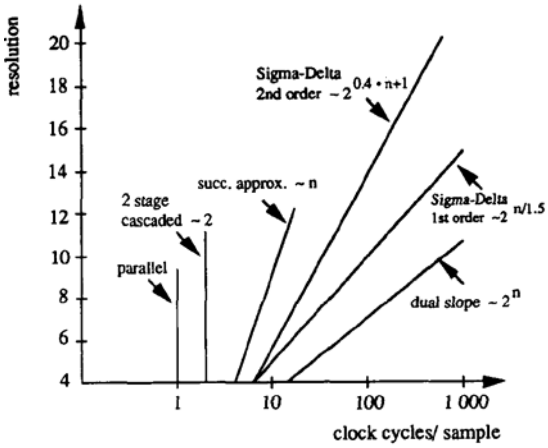
Resolution	Sampling rate	ENOB	Power dissip.	Supply voltage	architecture	reference
8 bit	100 MHz	6.5 bit@5V, 7.1 bit@8V	1.2W@5V	5 or 8 V	interpolating	Steyaert , Roovers, Craninckx, CICC 1993
5 bit	5 GHz	4 bit at 5GHz	113 mW@1V	1 V	interpolating	Wang, Liu, VLSI-DAT '2007
6 bit	200 MHz	5.35 bit	35 mW@3.3V	3.3V	folding and interpolating	Yin, Wang, Liu, ICSICT, 2008
6 bit	200 MHz	5.5 bit	78.8 mW@2.5V	2.5V	folding and interpolating	Silva, Fernandes, ISCAS, 2003

Oversampling converters (chapter 14 in "J & M")

- For high resolution, low-to-medium-speed applications like for example digital audio
- Relaxes requirements placed on analog circuitry, including matching tolerances and amplifier gains
- Simplify requirements placed on the analog anti-aliasing filters for A/D converters and smoothing filters for D/A converters.
- Sample-and-Hold is usually not required on the input
- Extra bits of resolution can be extracted from converters that samples much faster than the Nyquist-rate. Extra resolution can be obtained with lower oversampling rates by exploiting noise shaping



Resolution and clock cycles per sample

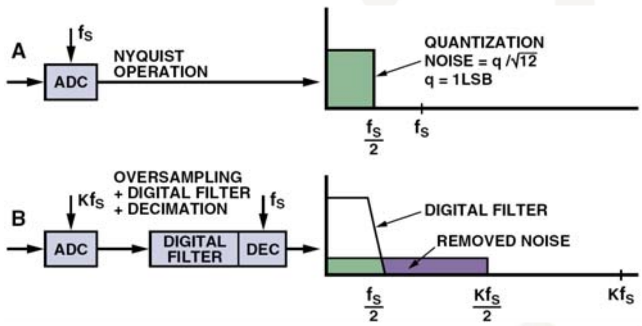


. Dependence of achievable resolution and required clock cycles per sample for various ADC systems.

A Gigasample/Second 5-b ADC with On-Chip Track and Hold Based on an Industrial 1-μm GaAs MESFET E/D Process

Richard Hagelauer, Member, IEEE, Frank Oehler, Günter Rohmer, Josef Sauerer, and Dieter Seitzer, Senior Member, IEEE

Nyquist Sampling and Oversampling



- Figure from [Kest05]
- Straight over-sampling gives an SNR improvement of 3 dB / octave
- fs > $2f_0$ ($2f_0$ = Nyquist Rate
- OSR = $f_s/2f_0$
- SNRmax = 6.02N+1.76+ 10log (OSR)

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Oversampled converters; High resolution and relatively low speed

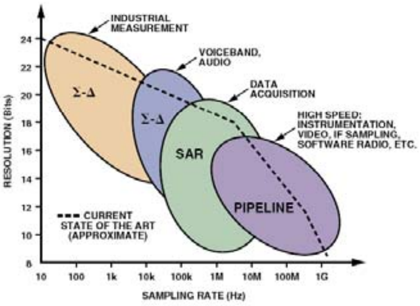

Figure 1. ADC architectures, applications, resolution, and sampling rates.

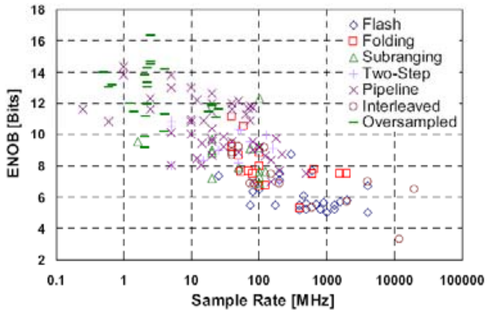

Fig. 2. ADC sample rate vs. ENOB from 1987 to 2005.

Which ADC Architecture Is Right for Your Application?

By Walt Kester [walt.kester@analog.com]

IEEE 2005 CUSTOM INTEGRATED CIRCUITS CONFERENCE

Scaling of Analog-to-Digital Converters into Ultra-Deep-Submicron CMOS

Y. Chiu[1], B. Nikolić[2], and P. R. Gray[2]

[1] Electrical and Computer Engineering, University of Illinois at Urbana-Champaign
[2] Electrical Engineering and Computer Sciences, University of California at Berkeley

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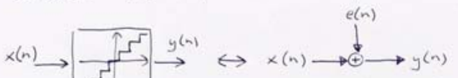
QUANTIZATION NOISE (p. 532-533 in "J & M")

The quantization noise is the difference between the input and output values.



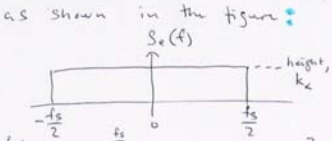
$e(n) = y(n) - x(n)$

This model is exact under the assumption that the quantization error is strongly related to the input signal ("J & M" p. 532). The model becomes approximate when assumptions are made about the statistical properties of e(n), such as e(n) being an independent white-noise signal. This model leads to a simpler understanding of ΣΔ and with some exceptions is usually reasonably accurate.

- If x(n) is very active, e(n) can be approximated as an independent random number uniformly distributed between $\pm \frac{\Delta}{2}$, where Δ equals the difference between two adjacent quantization levels.

Thus, the quantization noise power equals $\frac{\Delta^2}{12}$ (Sec. 11.3) and is independent of the sampling frequency, f_s

The spectral density of e(n), $S_e(f)$ is white (constant over freq.) and all its power within $\pm f_s/2$, as shown in the figure:



$$\int_{-f_s/2}^{f_s/2} S_e^2(f)\,df = \int_{-\frac{f_s}{2}}^{\frac{f_s}{2}} k_x^2\,df = (k_x)^2 f_s = \frac{\Delta^2}{12}$$

$$\Updownarrow$$

$$k_x = \frac{\Delta}{\sqrt{12}}\sqrt{\frac{1}{f_s}}$$

The spectral density height is calculated by noting that the total noise power is $\Delta^2/12$ and with a two-sided def. of power equals the area under $S_e(f)$ within $+/- f_s/2$

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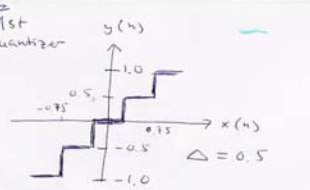
14.1 Output and quantization errors for two quantizers

$x(n) = \{0.01, 0.31, -0.11, 0.80, 0.52, -0.70\}$

1st quantizer ?



$\Delta = 0.5$

Quantizer 1:

$y_1(n) = \{0.0, 0.5, 0, 1.0, 0.5, -0.5\}$

Quantizer 2:

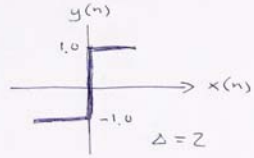
$y_2(n) = \{1.0, 1.0, -1.0, 1.0, 1.0, -1.0\}$

$e(n) = y(n) - x(n)$

$e_1(n) = \{-0.01, 0.19, -0.11, -0.30, -0.02, 0.20\}$

$e_2(n) = \{0.99, 0.69, -0.89, 0.20, 0.48, -0.30\}$

Quantizer II:



$\Delta = 2$

Expected power and power density height?

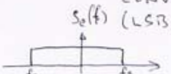
e(n) is approximated as an independent random number uniformly distributed between $\pm\frac{\Delta}{2}$, where Δ equals the difference between two adjacent quantization levels.

$$P_e = \frac{\Delta^2}{12}$$

quant 1: $\frac{\Delta^2}{12}[W] = \frac{(0.5)^2}{12}[W] = 0.0208\bar{3}\ [W]$

quant 2: $\frac{\Delta^2}{12}[W] = \frac{2^2}{12}[W] = 0.3\bar{3}\ [W]$

"OVERSAMPLING IS BASED ON THE ASSUMPTION THAT AN ADC'S TOTAL QUANTIZATION NOISE POWER (VARIANCE) IS THE SQUARED VALUE OF THE CONVERTER'S LEAST SIGNIFICANT BIT (LSB) VOLTAGE DIVIDED BY 12" (LYONS'05)

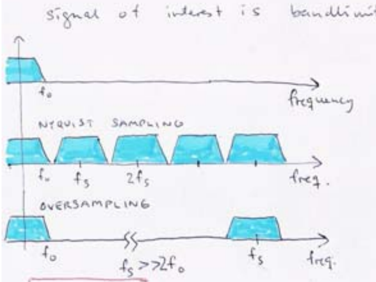


$S_{eI}^2(f) = \frac{0.0208\bar{3}}{2\pi}\left[\frac{W}{rad/Sample}\right] = 0.00331\ \frac{W}{rad/Sample}$

$S_{eII}^2(f) = \frac{0.333}{2\pi}\left[\frac{W}{rad/Sample}\right] = 0.053\ \frac{W}{rad/Sample}$

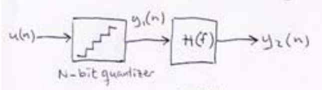
OVERSAMPLING ADVANTAGE p. 535

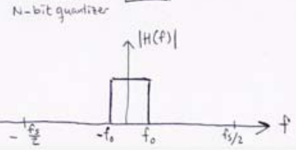
signal of interest is bandlimited to f_0



$$OSR \equiv \frac{f_s}{2f_0}$$

After quantization, $y_1(n)$ is filtered by $H(f)$ to create $y_2(n)$ that eliminates quantization noise (together with any other signals) greater than f_0.





If the input is sinusoidal, its maximum peak value without clipping is $2^N(\Delta/2)$. For this wave the signal power, P_s, has a power equal to $P_s = \left(\frac{\Delta 2^N}{2}\frac{1}{\sqrt{2}}\right)^2 = \frac{\Delta^2 2^{2N}}{8}$

The power of the input signal within $y_2(n)$ remains the same as before since we assumed the signal's frequency content is below f_0.

HOWEVER, THE QUANTIZATION NOISE POWER IS REDUCED TO

$$P_e = \int_{-f_s/2}^{f_s/2} S_e^2(f)\,|H(f)|^2\,df = \int_{-f_0}^{f_0} k_x^2\,df$$

$$= \frac{2f_0}{f_s}\cdot\frac{\Delta^2}{12} = \frac{\Delta^2}{12}\left[\frac{1}{OSR}\right]$$

THEREFORE, DOUBLING OSR DECREASES THE QUANTIZATION NOISE POWER BY ONE-HALF, OR EQUIVALENTLY, 3 dB (or equiv. 0.5 bits)

$$SNR_{MAX} = 10\log\left(\frac{P_s}{P_e}\right) = 10\log\left(\frac{3}{2}2^{2N}\right) + 10\log(OSR)$$

$$= \underbrace{6.02N + 1.76}_{\text{due to N-bit quantizer}} + \underbrace{10\log(OSR)}_{\text{due to oversampling}}\ [dB]$$

$$SNR_{max} = 10 \log\left(\frac{P_s}{P_e}\right) \quad \wedge \quad P_s = \frac{\Delta^2 2^{2N}}{8} \quad \wedge \quad P_e = \frac{\Delta^2}{12}\frac{1}{OSR}$$

$$SNR_{max} = 10 \log\left[\frac{\frac{\Delta^2 2^{2N}}{8}}{\frac{\Delta^2}{12}\cdot\frac{1}{OSR}}\right] = 10 \log\left[\frac{\frac{\Delta^2 \cdot 2^{2N}}{2\cdot 2\cdot 2}}{\frac{\Delta^2}{2\cdot 2\cdot 3}\cdot\frac{1}{OSR}}\right] = 10 \log \frac{3}{2} 2^{2N} \cdot OSR$$

$$= 10 \log \frac{3}{2}\cdot 2^{2N} + 10 \log OSR$$

$$= 10 \log \frac{3}{2} + 10 \log 2^{2N} + 10 \log OSR$$

$$= 10 \log 2^{2N} + 1.76 + 10 \log OSR$$

$$= 10 \cdot 2N \cdot \log 2 + 1.76 + 10 \log OSR$$

$$= 10 \cdot 2 \cdot N \cdot 0.301 + 1.76 + 10 \log OSR$$

$$= 6.02 N + 1.76 + 10 \log (OSR) \quad [dB]$$

$\log_b(c^p) = p\log_b(c$

$\log(xy) = \log x + \log y$

(14.13) pp. 536 i J&M.

16. mars 2010 21

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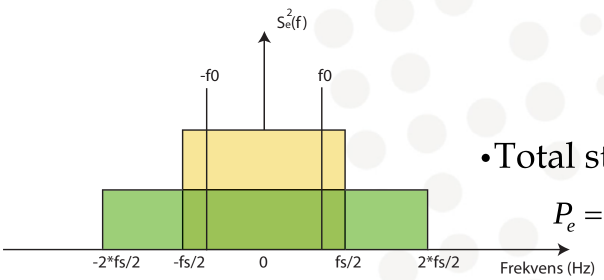
Oversampling (without noise shaping)



•Total støy er gitt av:

$$P_e = \int_{-f_0}^{f_0} S_e^2(f)df = \frac{\Delta^2}{12}\cdot\frac{1}{OSR}$$

- Doubling of the sampling frequency increases the dynamic range by 3 dB = 0.5 bit.
- To get a high SNR a very high fs is needed → high power consumption.
- Oversampling usually combined with noise shaping and higher order modulators, for higher increase in dynamic range per octave ("OSR")

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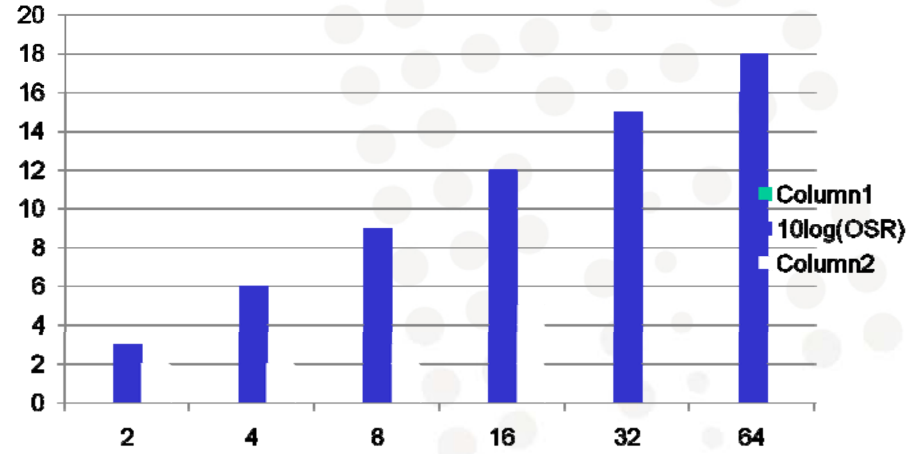
SNRmax = 6.02N+1.76+10log(OSR) [dB]
SNR improvement 0.5 bits / octave



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Ex. 14.3

EXAMPLE 14.3

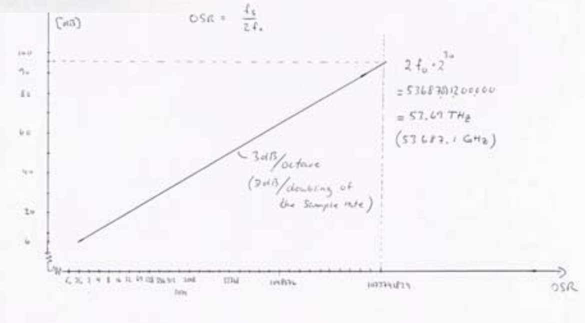
Given that a 1-bit A/D converter has a 6-dB SNR, what sample rate is required using oversampling (no noise shaping) to obtain a 96-dB SNR (i.e., 16 bits) if $f_0 = 25$ kHz ? (Note that the input into the A/D converter has to be very active for the white-noise quantization model to be valid—a difficult arrangement when using a 1-bit quantizer with oversampling without noise shaping).

Solution

Oversampling (without noise shaping) gives 3 dB/octave where 1 octave implies doubling the sampling rate. We require 90 dB divided by 3 dB/octave, or 30 octaves. Thus, the required sampling rate, f_s, is

$$f_s = 2^{30} \times 2f_0 \cong 54{,}000 \text{ GHz !}$$

This example shows why noise shaping is needed to improve the SNR faster than 3 dB/octave, since 54,000 GHz is highly impractical.



Advantages of 1-bit A/D converters (p.537 in ”J&M”)

- Oversampling improves signal-to-noise ratio, but not linearity
- Ex.: 12-bit converter with oversampling needs component accuracy to match better than 16-bit accuracy if a 16-bit linear converter is desired

- Advantage of 1-bit D/A is that it is inherently linear. Two points define a straight line, so no laser trimming or calibration is required
- Many audio converters presently use 1-bit converters for realizing 16- to 18-bit linear converters (with noise shaping).

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Problems with some 1-bit converters ((?))

Why 1-Bit Sigma-Delta Conversion is Unsuitable for High-Quality Applications

by

Stanley P. Lipshitz and John Vanderkooy
Audio Research Group, University of Waterloo
Waterloo, Ontario N2L 3G1, Canada

ABSTRACT
Single-stage, 1-bit sigma-delta converters are in principle imperfectible. We prove this fact. The reason, simply stated, is that, when properly dithered, they are in constant overload. Prevention of overload allows only partial dithering to be performed. The consequence is that distortion, limit cycles, instability, and noise modulation can never be totally avoided. We demonstrate these effects, and using coherent averaging techniques, are able to display the consequent profusion of nonlinear artefacts which are usually hidden in the noise floor. Recording, editing, storage, or conversion systems using single-stage, 1-bit sigma-delta modulators, are thus inimical to audio of the highest quality. In contrast, multi-bit sigma-delta converters, which output linear PCM code, are in principle infinitely perfectible. (Here, multi-bit refers to at least two bits in the converter.) They can be properly dithered so as to guarantee the absence of all distortion, limit cycles, and noise modulation. The audio industry is misguided if it adopts 1-bit sigma-delta conversion as the basis for any high-quality processing, archiving, or distribution format to replace multi-bit, linear PCM.

Audio Engineering Society
Convention Paper 5395
Presented at the 110th Convention
2001 May 12–15 Amsterdam, The Netherlands

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Oversampling with noise shaping (14.2)

- Oversampling combined with noise shaping can give much more dramatic improvement in dynamic range each time the sampling frequency is doubled.
- The sigma delta modulator converts the analog signal into a noise-shaped low-resolution digital signal.
- The decimator converts to a high resolution digital signal

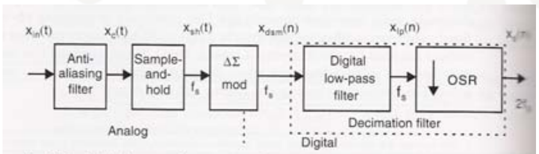

Fig. 14.5 Block diagram of an oversampling A/D converter.

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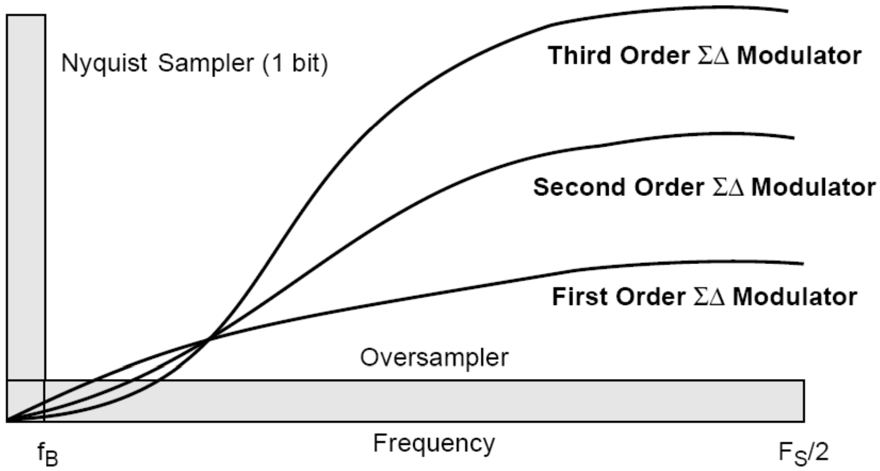
Multi-order sigma delta noise shapers (Sangil Park, Motorola)



Note: Higher order Noise Shaper has less baseband noise

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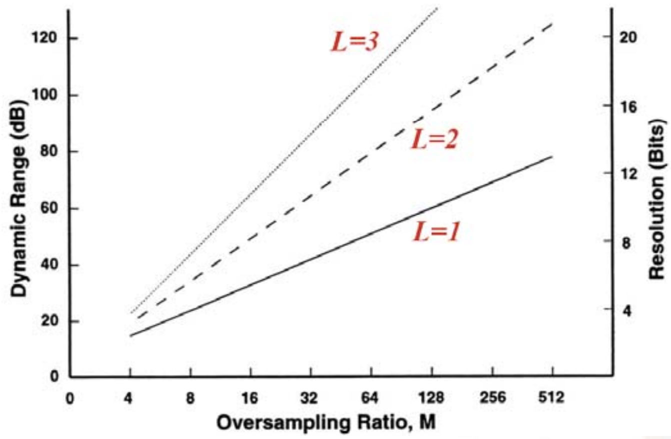
OSR, modulator order and Dynamic Range



- 2 X increase in M → (6L+3)dB or (L+0.5) bit increase in DR.
  L: sigma-delta order
  Oversampling and noise shaping

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Ex. 14.5

- Given that a 1-bit A/D converter has a 6 dB SNR, which sample rate is required to obtain a 96-dB SNR (or 16 bits) if f_0 = 25 kHz for straight oversampling as well as first-and second-order noise shaping?

- Oversampling with no noise shaping: From ex. 14.3 we know that straight oversampling requires a sampling rate of 54 THz.
- (6.02N+1.76+10 log (OSR) = 96
  <->
  6 + 10 log OSR = 96)
  <-> 10 log OSR = 90

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Ex. 14.5

$$SNR_{max} = 6.02N + 1.76 - 5.17 + 30\log(OSR) \quad (14.2$$

We see here that doubling the OSR gives an SNR improvement for a first-order modulator of 9 dB or, equivalently, a gain of 1.5 bits/octave. This result should be compared to the 0.5 bits/octave when oversampling with no noise shaping.

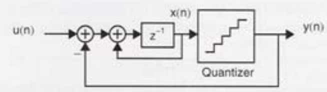

Fig. 14.7 A first-order noise-shaped interpolative modulator.

- Oversampling with 1st order noise shaping:
- 6 - 5.17 + 30 log(OSR) = 96 $\qquad$ $OSR = f_s / 2f_0$
- 30log (OSR) = 96 – 6 + 5.17 = 95.17

A doubling of the OSR gives an SNR improvement of 9 dB / octave for a 1st order modulator;

95.17 / 9 = 10.57 $\qquad 2^{10.56}$ x 2*25 kHz = 75.48 MHz

OR: log(OSR)=95.17/30 = 3.17 → OSR = 1509.6

1509.6 * (2*25kHz) = 75.48 MHz

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Ex. 14.5

$$SNR_{max} = 6.02N + 1.76 - 12.9 + 50\log(OSR) \quad (14.3$$

We see here that doubling the OSR improves the SNR for a second-order modulator by 15 dB or, equivalently, a gain of 2.5 bits/octave.
The realization of the second-order modulator using switched-capacitor techniques is straightforward and is left as an exercise for the interested reader.

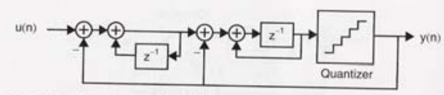

Fig. 14.10 Second-order ΔΣ modulator.

- Oversampling with 2nd order noise shaping:
- 6 – 12.9 + 50 log(OSR) = 96 $\qquad$ $OSR = fs / 2f_0$
- 50 log (OSR) = 96 – 6 + 12.9 = 102.9

A doubling of the OSR gives an SNR improvement of 15 dB / octave for a 2nd order modulator;

102.9 / 15 = 6.86 $\qquad 2^{6.86}$ x 2*25 kHz = 5.81 MHz

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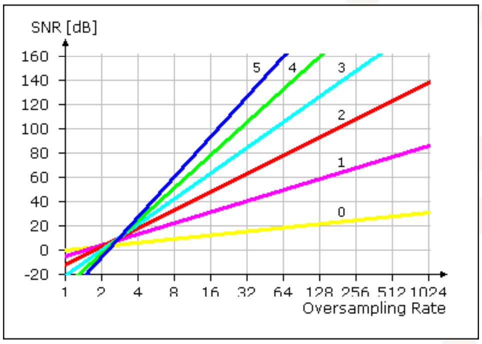
Ex. 14.5 ”point”:



- 2 X increase in M → (6L+3)dB or (L+0.5) bit increase in DR.
- L: sigma-delta order
- 6 db Quantizer, for 96 dB SNR:
- Plain oversampling: f_s=54 GHz
- 1st order : f_s=75.48 MHz
- 2nd order: f_s= 5.81 MHz

- Exam problem (INF4420) below

3 a) (Weight 10 %)

A sampled signal is bandlimited to f_0 = 22 kHz.What is the sampling frequency, f_s, for an oversampling ratio (“OSR”) of 128?
A 1-bit analog-to-digital converter (“ADC”) has an inherent 6-dB SNR. Which maximum SNR is acquired by combining it with strict oversampling and an OSR of 128, if no noise shaping is used?
What is the maximum SNR in the similar case exploiting 2nd order noise shaping?
If a 1-bit ADC using 3rd order noise shaping has a maximum SNR of 125 dB for an OSR of 128, what is the expected maximum SNR if the OSR is reduced to 32?

16. mars 2010

Sigma Delta converters,ISSCC 2008

- ISSCC- Foremost global forum
- ”CT”: continous time

ΔΣ DATA CONVERTERS
Chair: Zhongyuan Chang, IDT Technology, Shanghai, China
Associate Chair: Yiannos Manoli, University of Freiburg, Freiburg, Germany

27.1 A 108dB-SNR 1.1mW Oversampling DAC with a Three-Level DEM Technique **9:30 AM**

K. Nguyen, A. Bandyopadhyay, B. Adams, K. Sweetland, P. Baginski
Analog Devices, Wilmington, MA

A multi-bit audio DAC in a 0.18μm CMOS process uses a three-level DEM scheme and an ISI-free output stage to achieve 108dB SNR while consuming a total of 1.1mW per channel from a 1.8V supply.

27.2 A 0.7V 36μW 85dB-DR Audio ΔΣ Modulator Using a Class-C Inverter **9:00 AM**

Y. Chae, I. Lee, G. Han
Yonsei University, Seoul, Korea

An audio ΔΣ modulator is realized in a standard 0.18μm CMOS process, exploiting the possibility of substituting a class-C inverter for an OTA. The measurement results from the fabricated chip demonstrate 81dB SNDR, 84dB SNR, and 85dB DR for a 20kHz signal bandwidth. The chip consumes 36μW from a 0.7V supply.

27.3 An Inverter-Based Hybrid ΔΣ Modulator **9:30 AM**

R. Veldhoven, R. Rutten, L. Breems
NXP Semiconductors, Eindhoven, Netherlands

A hybrid ΔΣ modulator with 1st-order analog filter, 5b quantizer, 2nd-order digital filter, 1b quantizer, and 1b DAC is presented. The active circuitry is implemented solely with inverter circuits and standard digital cells. The 65nm CMOS modulator achieves a peak SNR of 77dB in 200kHz. Power consumption is 950μW at 1.2V and the area is 0.03mm².

Break 10:00 AM

27.4 A Noise-Coupled Time-Interleaved ΔΣ ADC with 4.2MHz BW, -98dB THD, and 79dB SNDR **10:15 AM**

K. Lee[1], J. Chae[1], M. Aniya[2], K. Hamashita[2], K. Takasuka[2], S. Takeuchi[2], G. Temes[1]
[1]Oregon State University, Corvallis, OR
[2]Asahi Kasei, Atsugi, Japan

A two-channel time-interleaved noise-coupled ΔΣ ADC is realized in 0.18μm CMOS technology. Time interleaving doubles the effective clock rate while noise coupling raises the effective order of the noise-shaping loops, implements dithering, and also prevents tone generation in all loops. Using a 1.5V supply, the device achieved SFDR>100dB, THD = -98dB, and an SNDR of 79dB in a 4.2MHz signal band.

27.5 A 28mW Spectrum-Sensing Reconfigurable 20MHz 72dB-SNR 70dB-SNDR DT ΔΣ ADC for 802.11n/WiMax Receivers **10:45 AM**

P. Malla[1,2], H. Lakdawala[1], K. Kornegay[3], K. Soumyanath[1]
[1]Intel, Hillsboro, OR
[2]Cornell University, Ithaca, NY
[3]Georgia Institute of Technology, Atlanta, GA

A reconfigurable MASH 2-2 ΔΣ ADC, fabricated in 90nm CMOS, has an OSR of 10.5 and uses a 1.2V supply. It achieves SNRs of 72, 62, 60, and 54dB with a 20MHz BW while consuming 28, 20, 15, and 12mW, respectively. The configuration and, therefore, power are determined by signal and blocker power. SNRs of 73, 77, and 78dB are achieved for BWs of 10, 5, 2.5MHz, respectively.

27.6 A 100mW 10MHz-BW CT ΔΣ Modulator with 87dB DR and -91dBc IMD **11:15 AM**

W. Yang, W. Schofield, H. Shibata, S. Korrapati, A. Shaikh, N. Abaskharoun, D. Ribner
Analog Devices, Wilmington, MA

A 5th-order CT ΔΣ modulator with a hybrid feedback-feedforward topology and 9-level quantization is implemented in a 0.18μm CMOS process. When clocked at 640MHz, the modulator achieves 87dB DR, 82dB peak SNDR, and -91dBc IMD over a 10MHz BW. The modulator occupies 0.7mm² and consumes 100mW from a 1.8V supply.

27.7 A 65nm CMOS CT ΔΣ Modulator with 81dB DR and 8MHz BW Auto-Tuned by Pulse Injection **11:45 AM**

Y-S. Shu[1], B-S. Song[1], K. Bacrania[2]
[1]University of California, San Diego, CA
[2]Conexant Systems, Palm Bay, FL

Active filters for CT ΔΣ modulators are calibrated by injecting a binary pulse dither and nulling it with an LMS algorithm. A 3rd-order 4b prototype in 65nm CMOS occupies 0.5mm² and consumes 50mW at 1.3V. At 256MS/s (OSR=16), the DR is 81dB with a 2.4V_{pp} full-scale range. SNR and SNDR at -1dBFS are 76 and 70dB, respectively.

27.8 A CT ΔΣ ADC for Voice Coding with 92dB DR in 45nm CMOS **12:00 PM**

L. Doerrer, F. Kuttner, A. Santner, C. Kropf, T. Puaschitz, T. Hartig
Infineon, Villach, Austria

A 2nd-order CT multi-bit (4b) ΔΣ ADC for voice coding is implemented in a 45nm CMOS process. The input operational amplifier is chopped to eliminate flicker noise and offset. The quantizer, a power-efficient 3-comparator tracking ADC with a capacitive voltage reference DAC, is suitable for low-voltage designs and high clock rates. Over a bandwidth of 20kHz, the DR is 86dB. The ADC consumes 1.2mW from a 1.1V supply when clocked at 12MHz.

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The International Solid-State Circuits Conference is the foremost global forum for presentation of advances in solid-state circuits and systems-on-a-chip. The Conference offers a unique opportunity for engineers working at the cutting edge of IC design and application to maintain technical currency and to network with leading experts.

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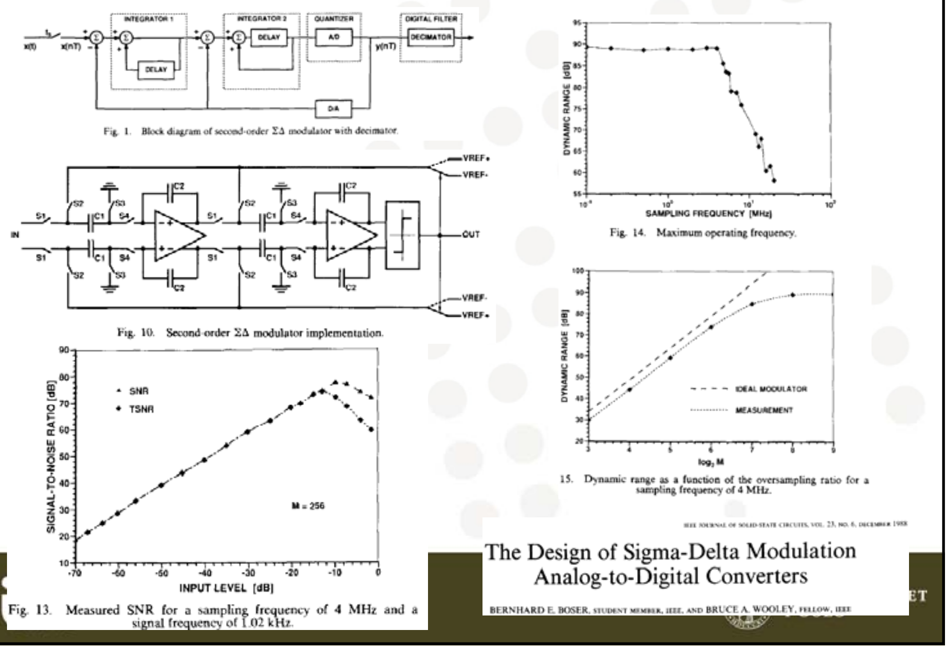
2nd order sigma delta modulator



Additional litterature

- Stanley P. Lipshitz, John Vanderkooy: Why 1-bit Sigma Delta Conversion is Unsuitable for High Quality Applications , Journal of the audio engineering society, 2001.
- Y. Chiu, B. Nicolic, P. R. Gray: Scaling of Analog-to-Digital Converters into Ultra-Deep-Submicron CMOS, Proceedings of Custom Integrated Circuits Conference, 2005.
- Richard Hagelauer, Frank Oehler, Gunther Rohmer, Josef Sauerer, Dieter Seitzer: A GigaSample/Second 5-b ADC with On-Chip Track-And-Hold Based on an Industrial 1 um GaAs MESFET E/D Process, IEEE Journal of Solid-State Circuits ("JSSC"), October 1992.
- Walt Kester: Which ADC Architecture is right for your application?, Analog Dialogue, Analog Devices, 2005.
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- B. E. Boser, B. A. Wooley: "The design of sigma delta modulation analog to digital converters, IEEE JSSC, 1988.
- John P. Bentley: Principles of Measurement Systems, 2nd ed., Bentley, 1989.
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  EE247 Analog Digital Interface Integrated Circuits, Fall 07;http://inst.eecs.berkeley.edu/~ee247/fa07/

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Next Time, 23/3-10:

- More from Chapter 14; Oversampling Converters (14.2, 14.3, 14.4, 14.5, 14.7)
- Beginning of chapter 16; Phase-Locked Loops (16.1)

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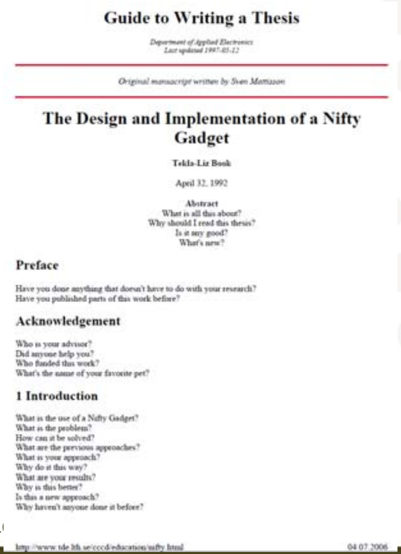
Guide to writing a thesis / report: The Design and implementation of a Nifty Gadget (page 1 and 2)



Guide to Writing a Thesis

Department of Applied Electronics
Last updated 1997-05-12

Original manuscript written by Sven Mattisson

The Design and Implementation of a Nifty Gadget

Tekla-Liz Book

April 32, 1992

Abstract
What is all this about?
Why should I read this thesis?
Is it any good?
What's new?

Preface

Have you done anything that doesn't have to do with your research?
Have you published parts of this work before?

Acknowledgement

Who is your advisor?
Did anyone help you?
Who funded this work?
What's the name of your favorite pet?

1 Introduction

What is the use of a Nifty Gadget?
What is the problem?
How can it be solved?
What are the previous approaches?
What is your approach?
Why do it this way?
What are your results?
Why is this better?
Is this a new approach?
Why haven't anyone done it before?

http://www.tde.lth.se/cccd/education/nifty.html 04.07.2006

or
Why do you reiterate previous work?
What is your contribution to the field of Nifty Gadgets?

2 Theoretical background

What is the required background knowledge?
Where can I find it?

2.1 Various approaches to Nifty Gadgets

What is the relevant prior work?
Where can I find it?
Why should it be done differently?
Has anyone attempted your approach previously?
Where is that work reported?

2.2 Nifty Gadgets my way

What is the outline of your way?
Have you published it before?

3 My implementation of a Nifty Gadget

Can you describe your implementation in detail?
Why did you use this technology?
How does the theory relate to your implementation?
What are your underlying assumptions?
What did you neglect and what simplifications have you made?
What tools and methods did you use?
Why use these tools and methods?

4 Nifty Gadget results

Did you actually build it?
How can you test it?
How did you test it?
Why did you test it this way?
Are the results satisfactory?
Why should you (not) test it more?
What compensations had to be made to interpret the results?
Why did you succeed/fail?

5 Discussion

Are your results satisfactory?
Can they be improved?
Is there a need for improvement?

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”Nifty Gadget” page 3 and 4

Are other approaches worth trying out?
Will some restriction be lifted?
Will you save the world with your Nifty Gadget?

6 References

What is the background reading list?
Where is the related work?
Where is the prior work?
Where can I find important material?

Appendix A

Can you outline fatilary calculus or whatever complicated theory or results you are using that will obscure the text?

Appendix B

A thesis should discuss the following topics:

- **Introduction**

  Presentation of the problem or phenomenon to be addressed, the situation where the problem or phenomenon occurs, and references to earlier relevant research.

  Common errors
  Problem is not properly specified or formulated; insufficient references to earlier work.

- **Purpose**

  What can be gained by more knowledge about the problem or phenomenon.

  Common errors
  The purpose is not mentioned, not connected to earlier research, or not in line with what the actual contents of the thesis.

- **Problem/Hypothesis**

  Questions that need to be answered to reach the goal and/or hypothesis formulated be means of underlying theories.

  Common errors
  Missing problem description; deficiencies in the connections between questions; badly formulated hypothesis.

- **Method**

  Choice of an adequate method with respect to the purpose and problem/hypothesis.

  Common errors
  An inappropriate method is used, for example due to lack of knowledge about different methods; erroneous use of chosen method.

- **Result**

  Answers to the forwarded questions by means of the achieved results.

  Common errors
  The results are not properly connected to the problem; blurry presentation; the results are inter-mixed with discussion.

- **Discussion**

  Discussion of the accuracy and relevance of the results; comparison with other researchers results.

  Common errors
  Too far reaching conclusions; guesswork not supported by the data; introduction of a new problem and a discussion around this.

- **Conclusion**

  Consequences of the achieved results, for example for new research, theory and applications.

  Common errors
  The conclusions are too far reaching with respect to the achieved results; the conclusions do not correspond with the purpose.

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